M-3-5-B1: Design and implement the following using, (i) logisim (do not use inbuilt adder, subtractor, mux, dmux, etc. other than logic gates) (ii) Verilog (gate modelling, dataflow modelling and behavioral modelling) (**Note:** File naming should be done as, 16CO226-L5.circ (for logisim), 16CO226-VG5.v (for gate modelling), 16CO226-VD5.v (for dataflow modelling), 16CO226-VB5.v (for behavioral modelling), 16CO226-V5.v (input/data file along-with $monitor for input and output) and 16CO226-V5.vcd (for waveform))

(i) Serial-in Serial-out (SISO) right shift register

(ii) 4-bit bidirectional shift register

(iii) Parallel-in Parallel-out (PIPO) shift register

(iv) Parallel-in Serial-out (PISO) shift register

Q. No.	Reg. No.
(i)	16CO101 -16CO112
(ii)	16CO113 - 16CO123
(iii)	16CO124 - 16CO134
(iv)	16CO135 - 16CO145