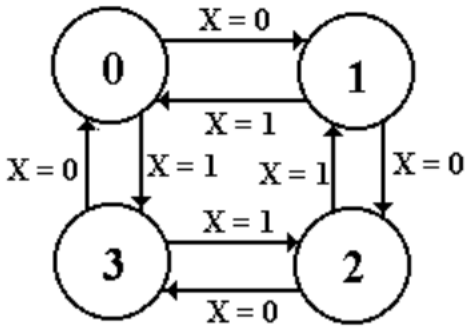
M-3-3-B1: Design and implement the following using, (i) logisim (do not use inbuilt adder, subtractor, mux, dmux, etc. other than logic gates) (ii) Verilog (gate modelling, dataflow modelling and behavioral modelling) (**Note:** File naming should be done as, 16CO226-L3.circ (for logisim), 16CO226-VG3.v (for gate modelling), 16CO226-VD3.v (for dataflow modelling), 16CO226-VB3.v (for behavioral modelling), 16CO226-V3.v (input/data file along-with $monitor for input and output) and 16CO226-V3.vcd (for waveform))

(i) Convert JK to SR flip-flop

(ii) Master Slave flip-flop using NAND gates

(iii) D flip-flop with AND and NOR gates

(iv) Given the state diagram draw its corresponding circuit diagram



Q. No.	Reg. No.
(i)	16CO101 - 16CO112
(ii)	16CO113 - 16CO123
(iii)	16CO124 - 16CO134
(iv)	16CO135 - 16CO145