M-3-1-B1: Design and implement the following using, (i) logisim (do not use inbuilt adder, subtractor, mux, dmux, etc. other than logic gates) (ii) Verilog (gate modelling, dataflow modelling and behavioral modelling) (**Note:** File naming should be done as, 16CO226-L1.circ (for logisim), 16CO226-VG1.v (for gate modelling), 16CO226-VD1.v (for dataflow modelling), 16CO226-VB1.v (for behavioral modelling), 16CO226-V1.v (input/data file along-with $monitor for input and output) and 16CO226-V1.vcd (for waveform))

(i) 4-bit look-ahead carry adder

(ii) 4-bit BCD adder (look-ahead carry adder)

(iii) 9's complement of BCD 4 digit

(iv) Excess-3 **<->** BCD using BCD-to-decimal decoder

Q. No.	Reg. No.
(i)	16CO101-16CO112
(ii)	16CO113-16CO123
(iii)	16CO124-16CO134
(iv)	16CO135-16CO145