

Sheet: NORTH

QVDDIO

>RXI_LCLK_P TXO_LCLK_PD
 >RXI_LCLK_N TXO_LCLK_ND
 >RXI_FRAME_P TXO_FRAME_PD
 >RXI_FRAME_N TXO_FRAME_ND
 >RXO_RD_WAIT_P TXI_RD_WAIT_PD
 >RXO_RD_WAIT_N TXI_RD_WAIT_ND
 >RXO_WR_WAIT_P TXI_WR_WAIT_PD
 >RXO_WR_WAIT_N TXI_WR_WAIT_ND

>RXI_DATA_P[0..7] TXO_DATA_P[0..7]
 >RXI_DATA_N[0..7] TXO_DATA_N[0..7]

File: paracard-elink.sch

Sheet: SOUTH

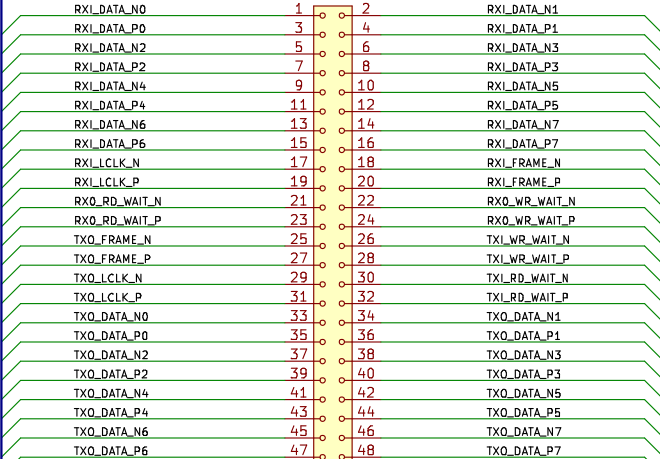
QVDDIO

>RXI_LCLK_P TXO_LCLK_PD
 >RXI_LCLK_N TXO_LCLK_ND
 >RXI_FRAME_P TXO_FRAME_PD
 >RXI_FRAME_N TXO_FRAME_ND
 >RXO_RD_WAIT_P TXI_RD_WAIT_PD
 >RXO_RD_WAIT_N TXI_RD_WAIT_ND
 >RXO_WR_WAIT_P TXI_WR_WAIT_PD
 >RXO_WR_WAIT_N TXI_WR_WAIT_ND

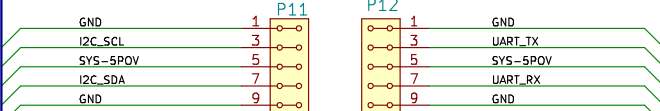
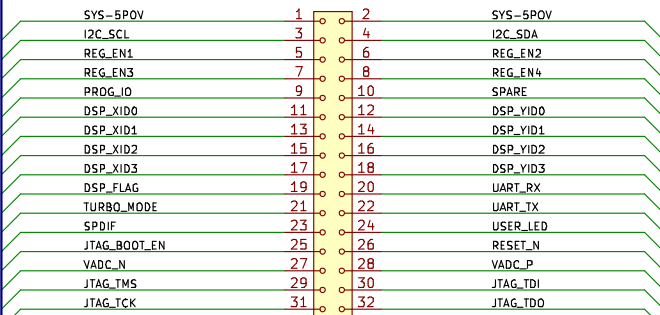
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 >RXI_DATA_N[0..7] TXO_DATA_N[0..7]

File: paracard-elink.sch

HEADER_2x24



P8 HEADER_2x16



Sheet: GPIO

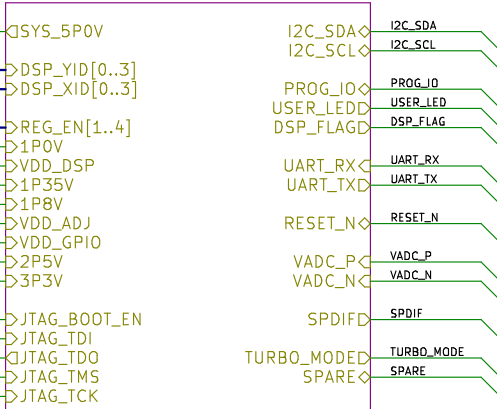
QVGPIO

GPIO_N[0..23]
 GPIO_P[0..23]

GPIO[0..47]

File: paracard-gpio.sch

Sheet: POWER

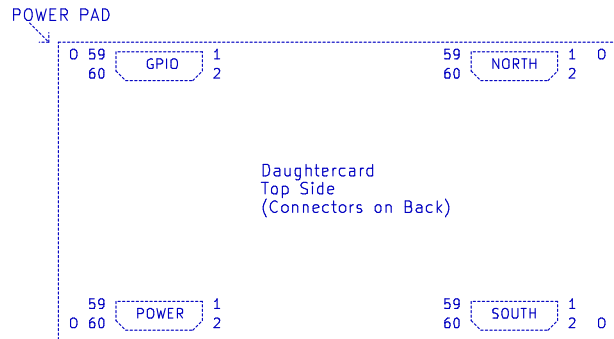
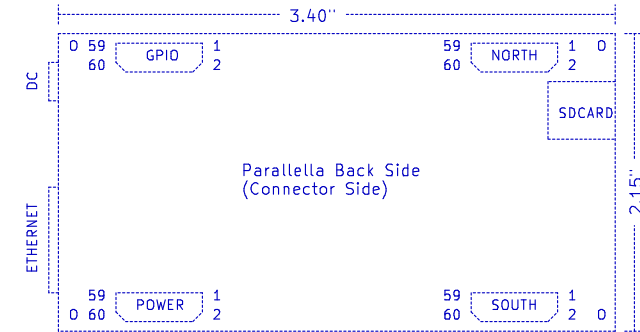
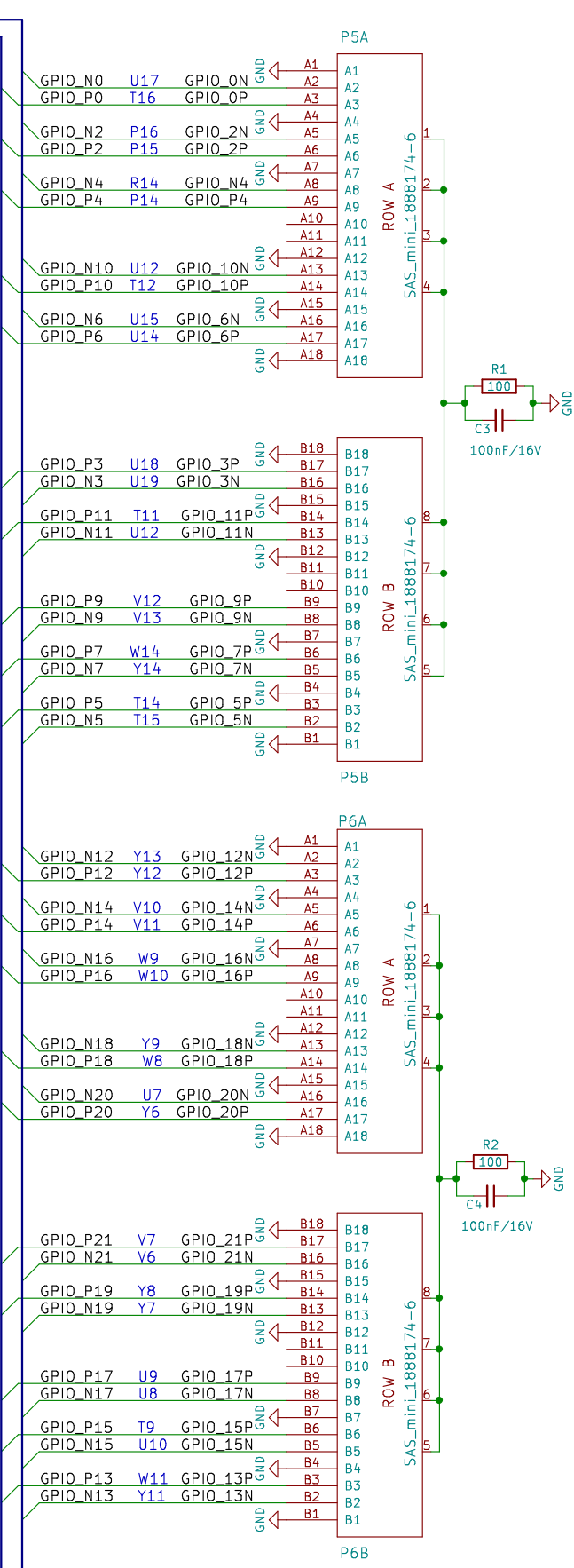
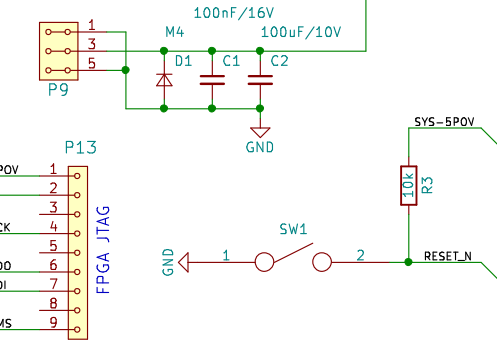


File: paracard-power.sch

Sheet: MountingHoles

QSYS_5POV

File: paracard-mtg.sch



"Paracard" Daughtercard template for Adapteva Parallella-1. This schematic and associated PCB design may be used as a starting point for Parallella-1 daughtercard design.

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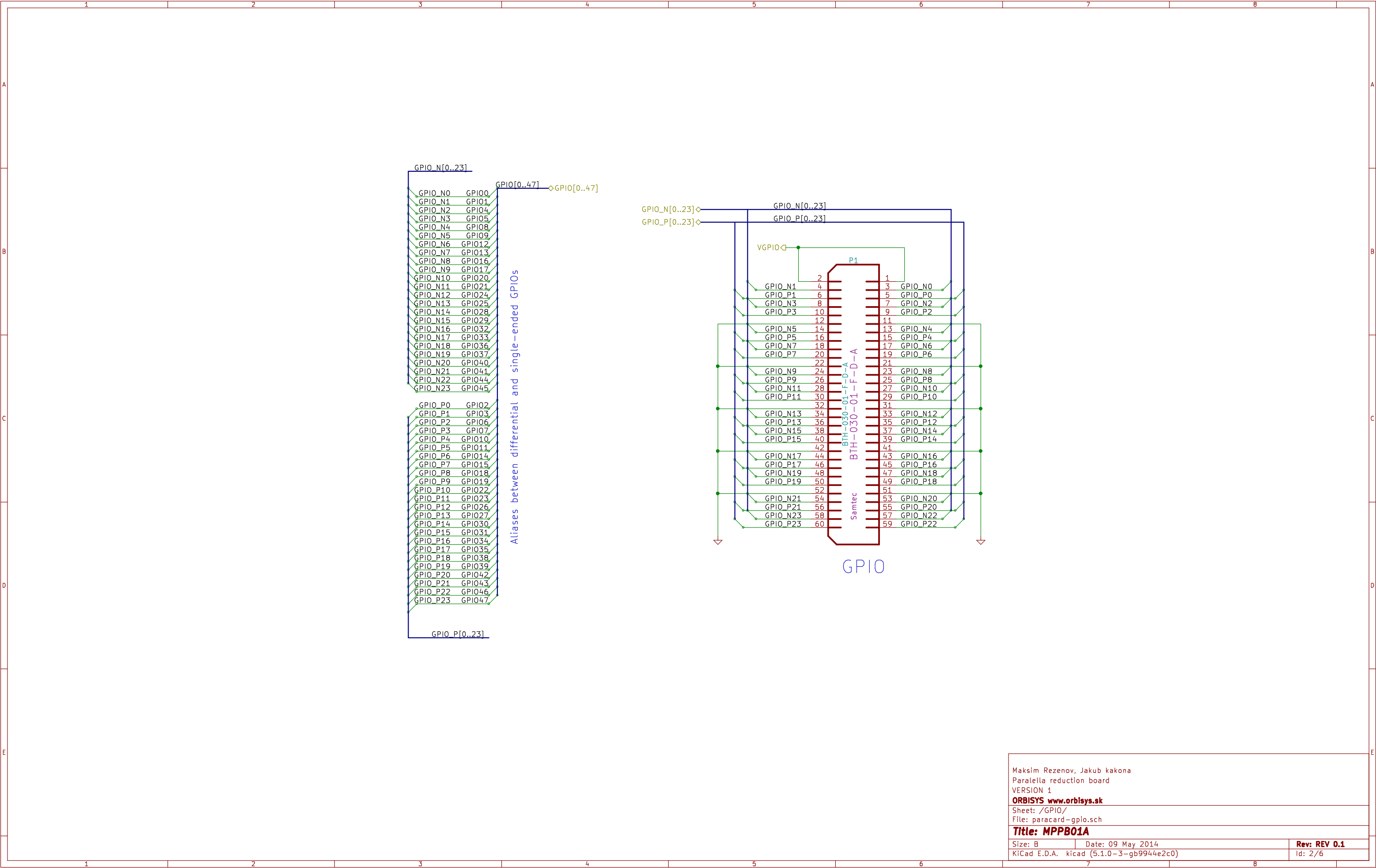
Maksim Rezenov, Jakub kakona
 Parallella reduction board
 VERSION 1
ORBISYS www.orbisisys.sk

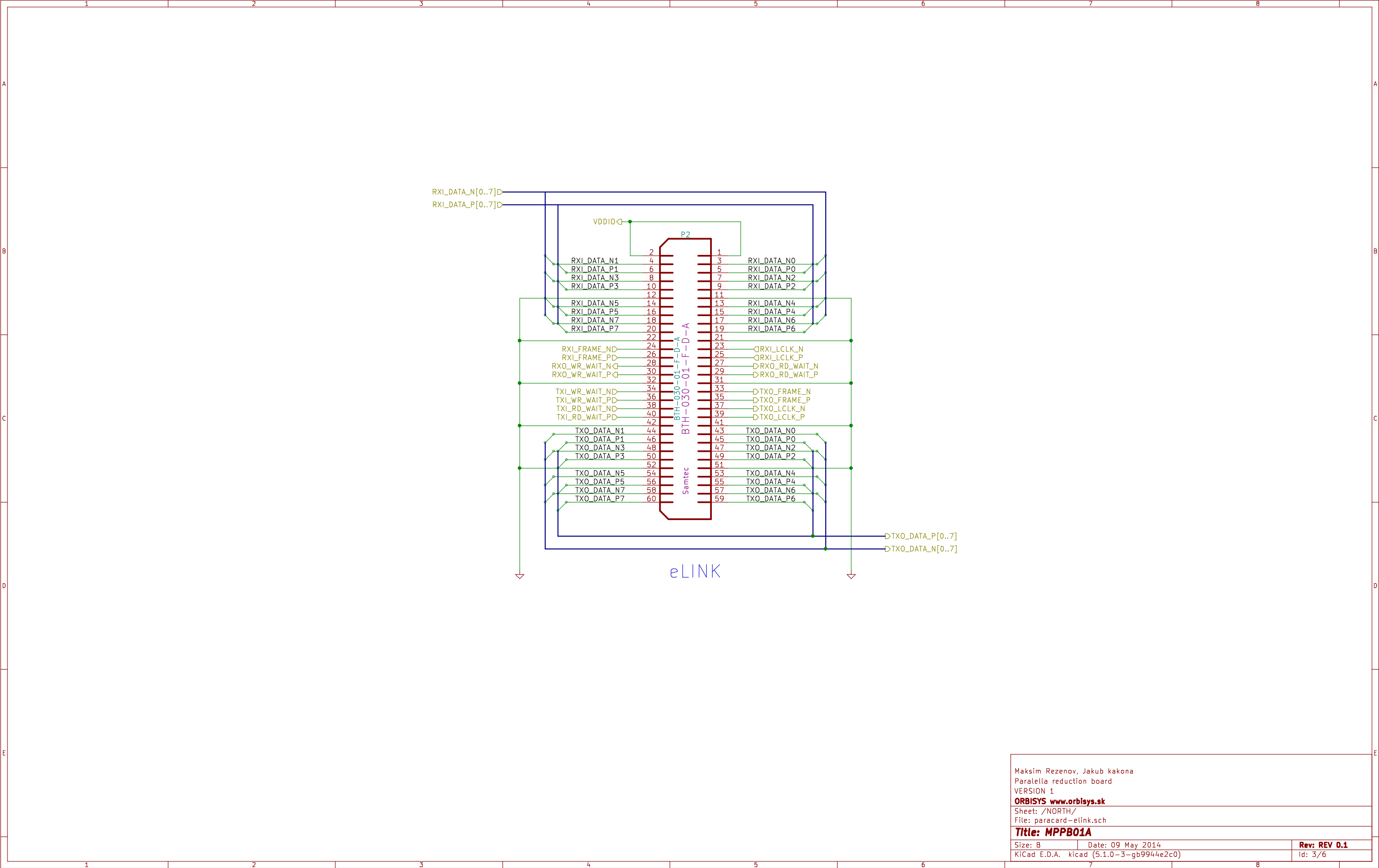
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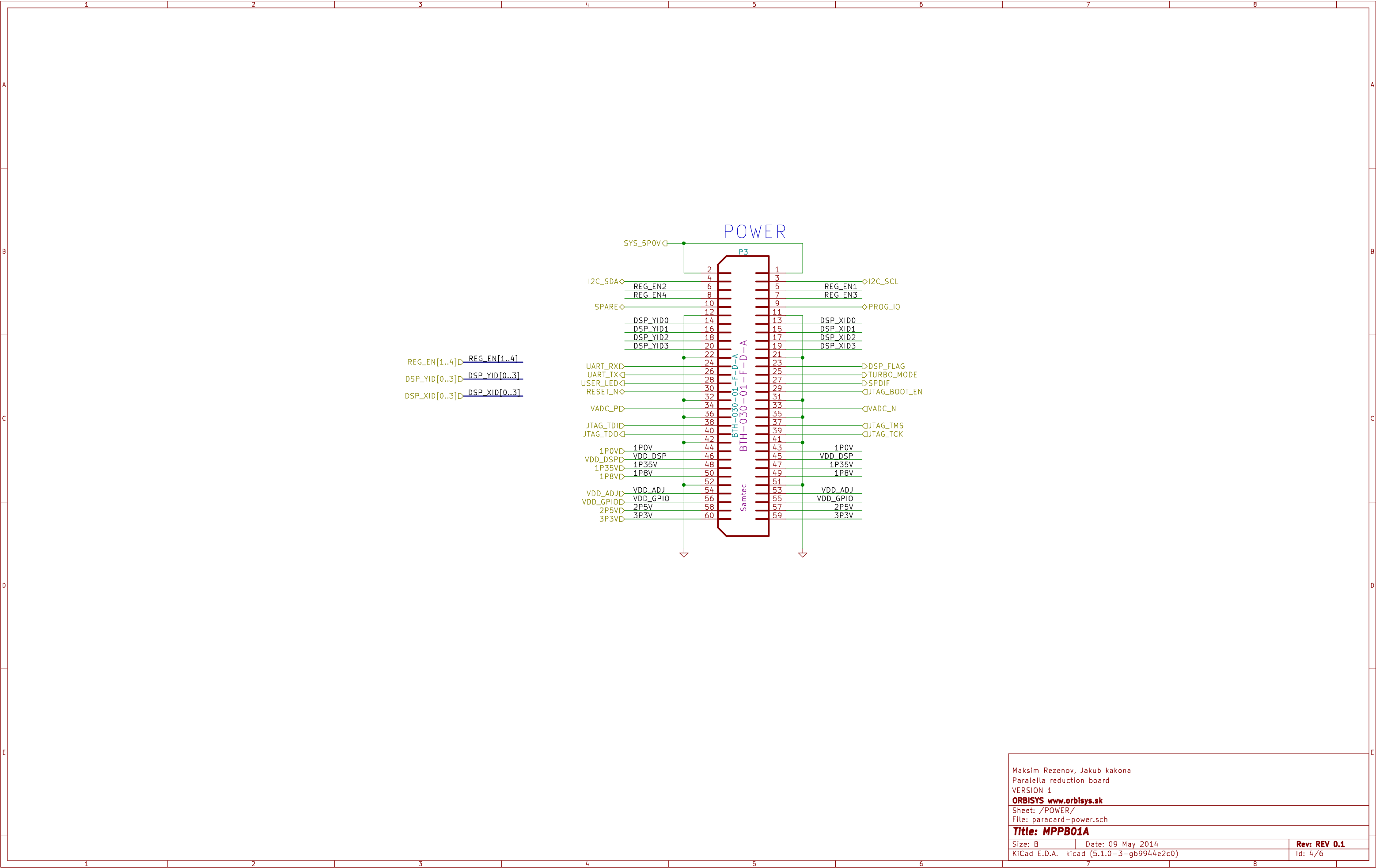
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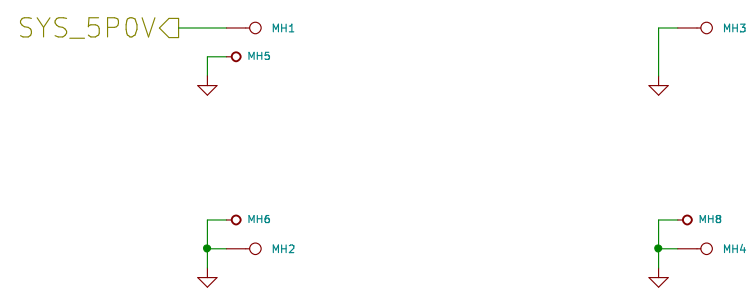
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Rev: **REV 0.1**
 Id: 1/6









Maksim Rezenov, Jakub kakona
 Paralella reduction board
 VERSION 1
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 Sheet: /MountingHoles/
 File: paracard-mtg.sch

Title: MPPB01A

Size: B	Date: 09 May 2014
KiCad E.D.A. kicad (5.1.0-3-gb9944e2c0)	

Rev: REV 0.1
Id: 5/6

