

NORTH

QVDDIO

DRXLCLK_P	TXO_LCLK_PD
DRXLCLK_N	TXO_LCLK_ND
DRXLFRAME_P	TXO_FRAME_PD
DRXLFRAME_N	TXO_FRAME_ND
QRXO_RD_WAIT_P	TXL_RD_WAIT_PD
QRXO_RD_WAIT_N	TXL_RD_WAIT_ND
QRXO_WR_WAIT_P	TXL_WR_WAIT_PD
QRXO_WR_WAIT_N	TXL_WR_WAIT_ND

DRXL_DATA_P[0..7] TXO_DATA_P[0..7]
DRXL_DATA_N[0..7] TXO_DATA_N[0..7]

File: paracard-elink.kicad_sch

SOUTH

QVDDIO

DRXLCLK_P	TXO_LCLK_PD
DRXLCLK_N	TXO_LCLK_ND
DRXLFRAME_P	TXO_FRAME_PD
DRXLFRAME_N	TXO_FRAME_ND
QRXO_RD_WAIT_P	TXL_RD_WAIT_PD
QRXO_RD_WAIT_N	TXL_RD_WAIT_ND
QRXO_WR_WAIT_P	TXL_WR_WAIT_PD
QRXO_WR_WAIT_N	TXL_WR_WAIT_ND

DRXL_DATA_P[0..7] TXO_DATA_P[0..7]
DRXL_DATA_N[0..7] TXO_DATA_N[0..7]

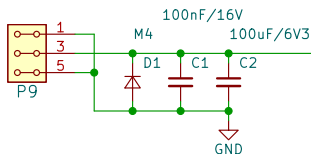
File: paracard-elink.kicad_sch

MountingHoles

PWR_FLAG <SYS-5P0V

QSYS_5P0V

File: paracard-mtg.kicad_sch



GPIO

QVGPIO

GPIO_N[0..23]
GPIO_P[0..23]
GPIO[0..47]

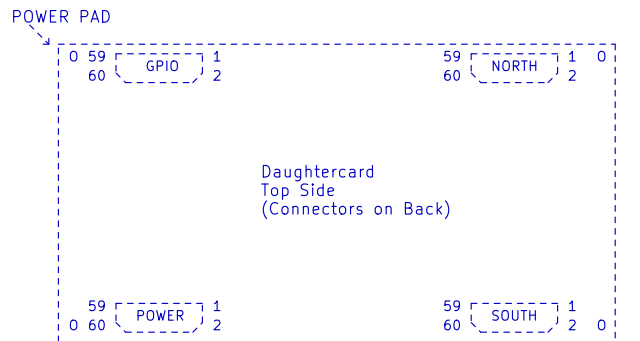
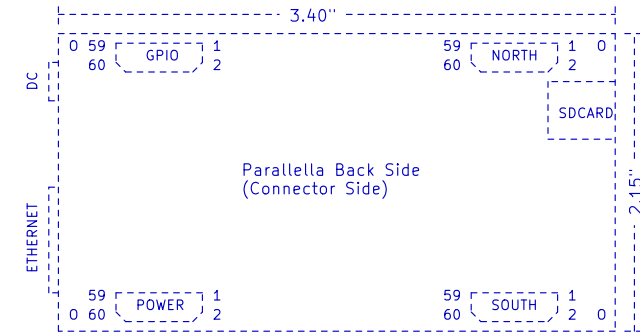
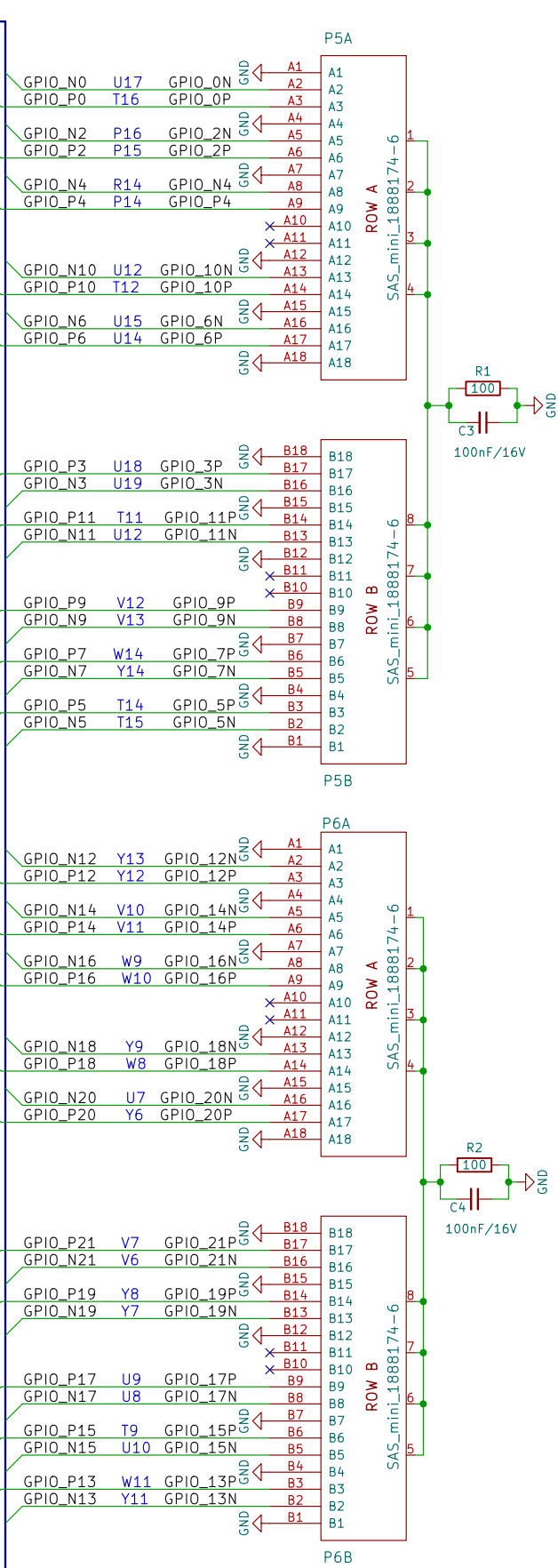
File: paracard-gpio.kicad_sch

POWER

SYS-5P0V	QSYS_5P0V	I2C_SDA	I2C_SDA
DSP_YID[0..3]	DSP_YID[0..3]	I2C_SCL	I2C_SCL
DSP_XID[0..3]	DSP_XID[0..3]	PROG_IO	PROG_IO
REG_EN[1..4]	REG_EN[1..4]	USER_LED	USER_LED
1P0V	>1P0V	DSP_FLAG	DSP_FLAG
VDD_DSP	>VDD_DSP	UART_RX	UART_RX
1P35V	>1P35V	UART_TX	UART_TX
1P8V	>1P8V	RESET_N	RESET_N
VDD_ADJ	>VDD_ADJ	VADC_P	VADC_P
VDD_GPIO	>VDD_GPIO	VADC_N	VADC_N
2P5V	>2P5V	SPDIF	SPDIF
3P3V	>3P3V	TURBO_MODE	TURBO_MODE
JTAG_BOOT_EN	JTAG_BOOT_EN	SPARE	SPARE
JTAG_TDI	JTAG_TDI		
JTAG_TDO	JTAG_TDO		
JTAG_TMS	JTAG_TMS		
JTAG_TCK	JTAG_TCK		

File: paracard-power.kicad_sch

GPIO_N[0..23]
GPIO_P[0..23]



P6A and P6B Mini-SAS connectors are available only with Zynq XC7Z020. Therefore could be used only with Parallela Embedded (P1602).

COMMENTO

Parallel MLAB interface board

Title: MPPB01B

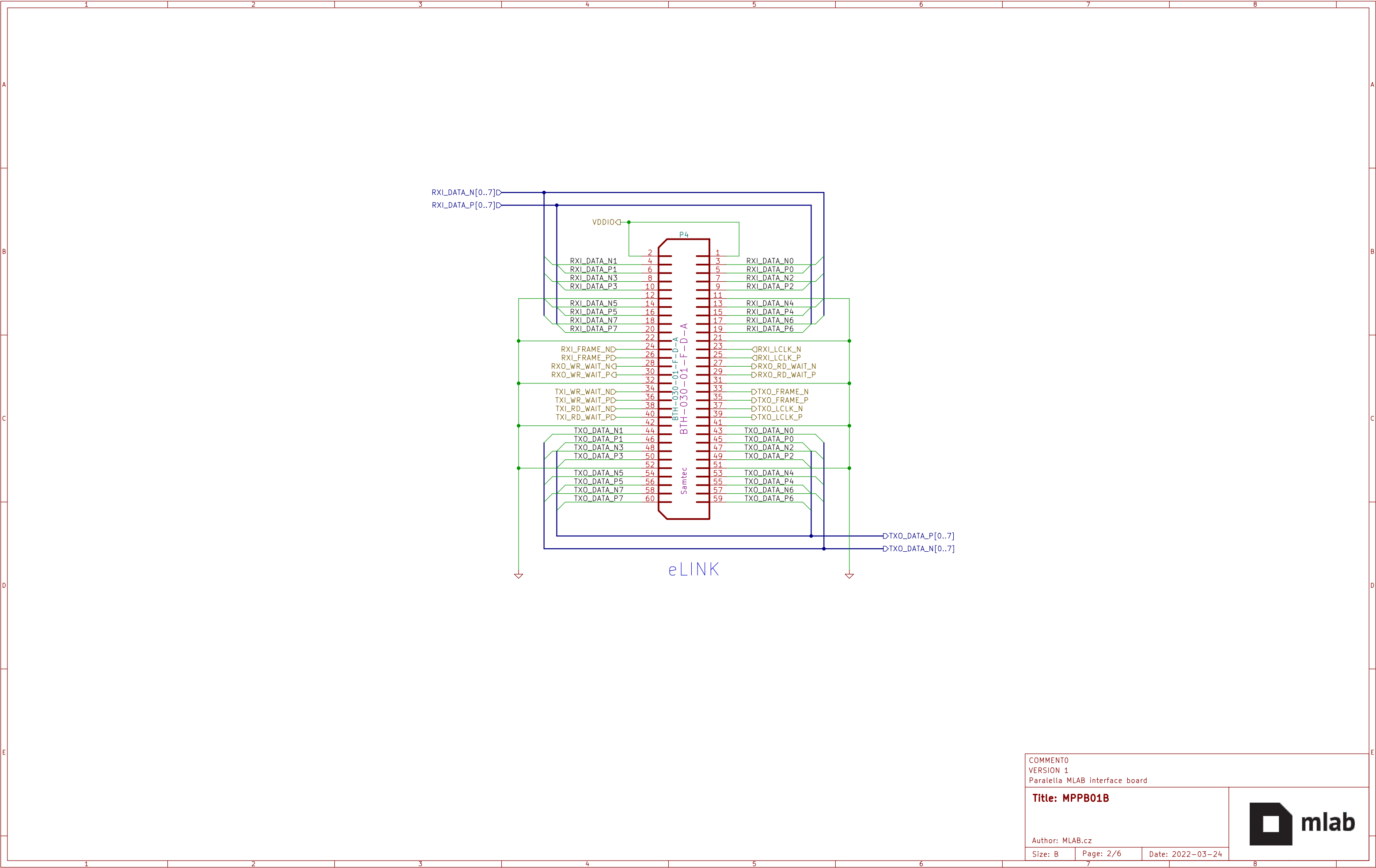
Author: MLAB.cz

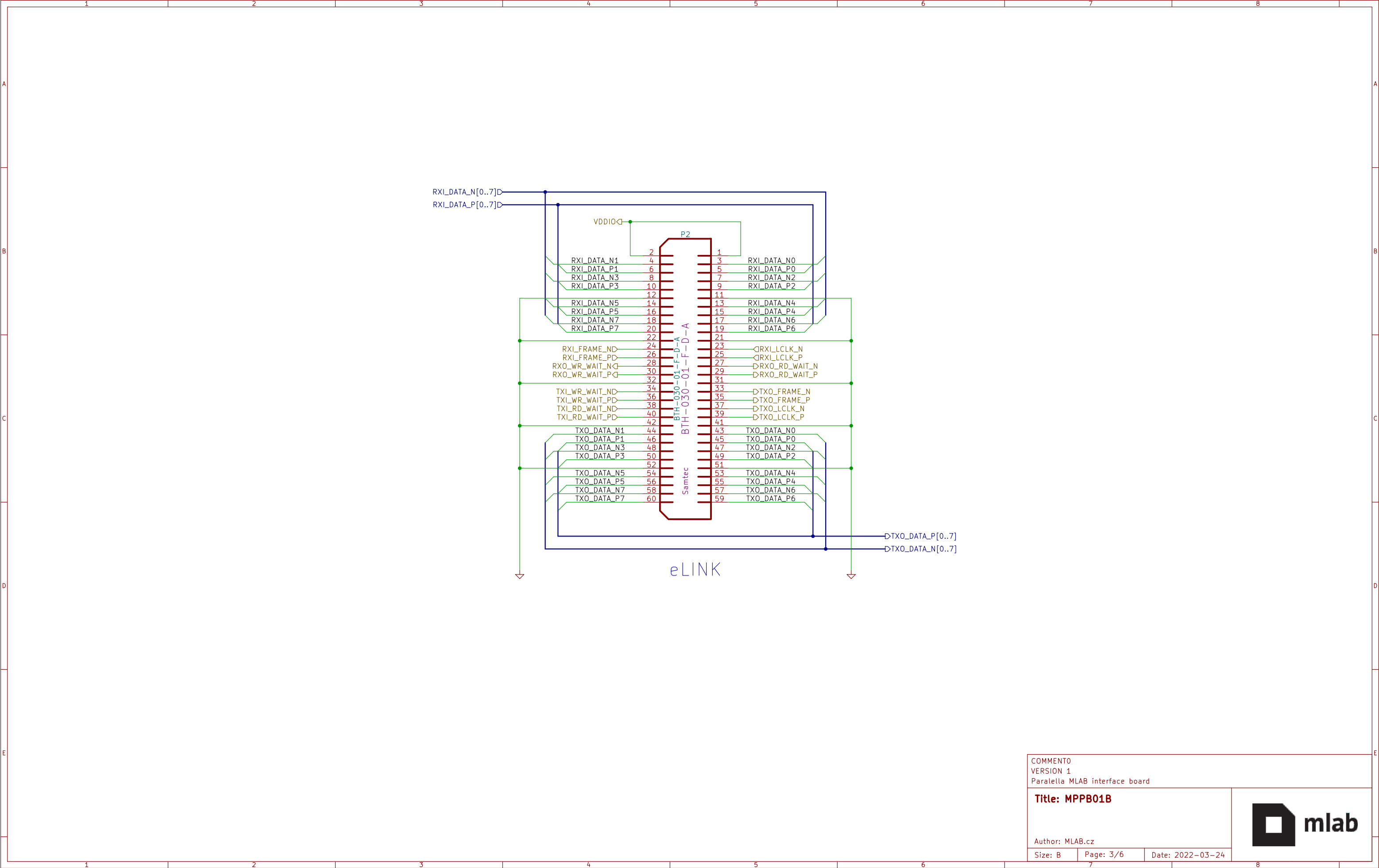
Size: B

Page: 1/6

Date: 2022-03-24







COMMENTO
VERSION 1
Paralella MLAB interface board

Title: MPPB01B

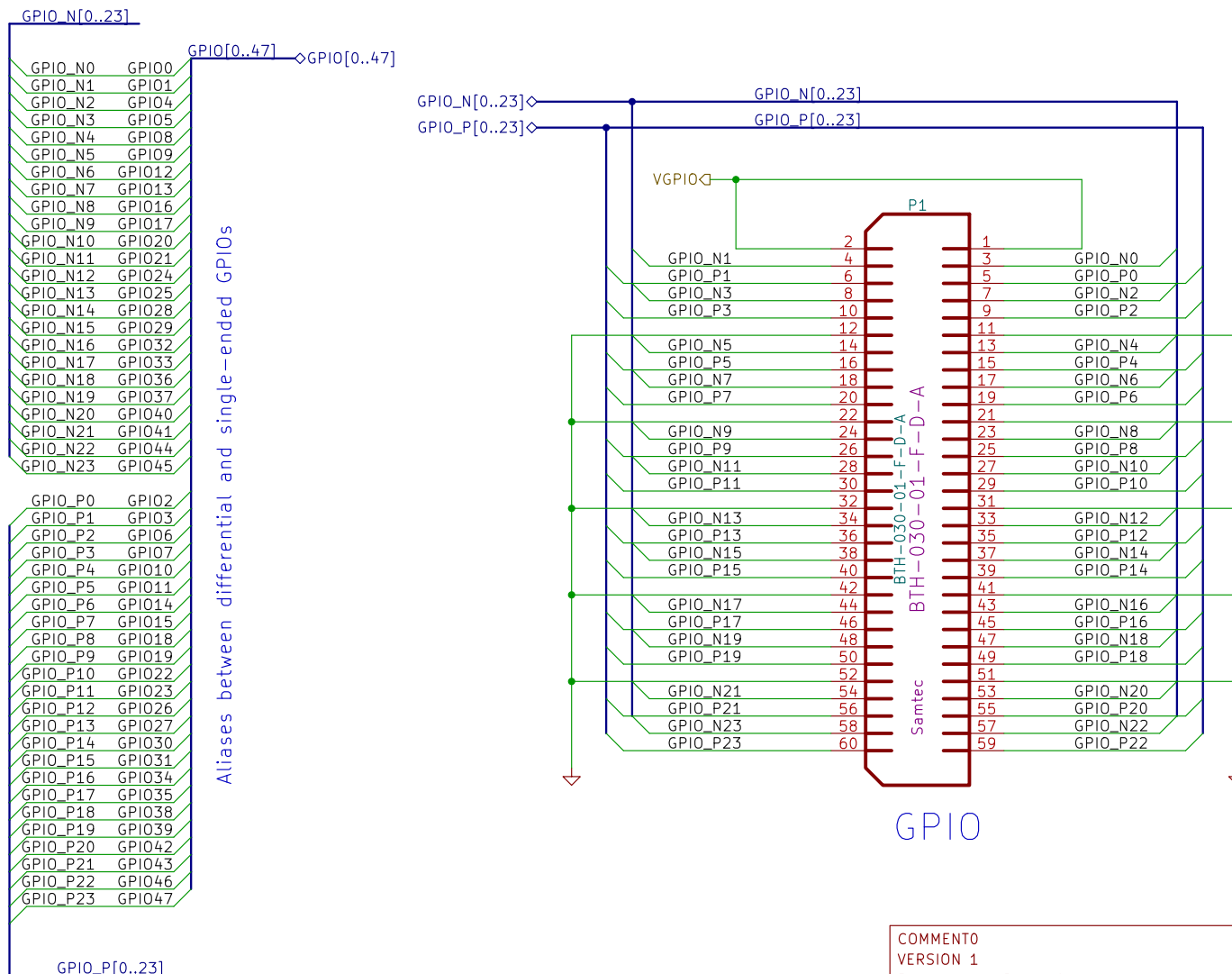
Author: MLAB.cz

Size: B

Page: 3/6

Date: 2022-03-24





COMMENTO
VERSION 1
Paralella MLAB interface board

Title: MPPB01B

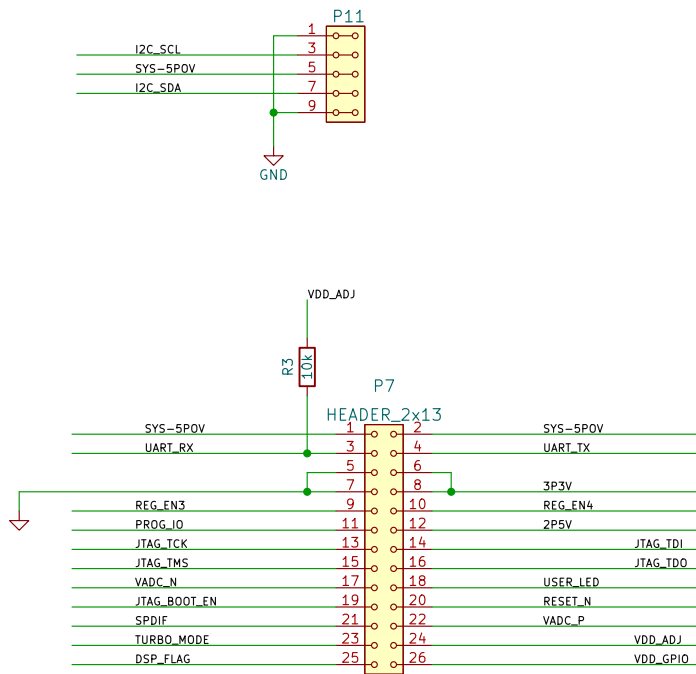
Author: MLAB.cz

Size: A4

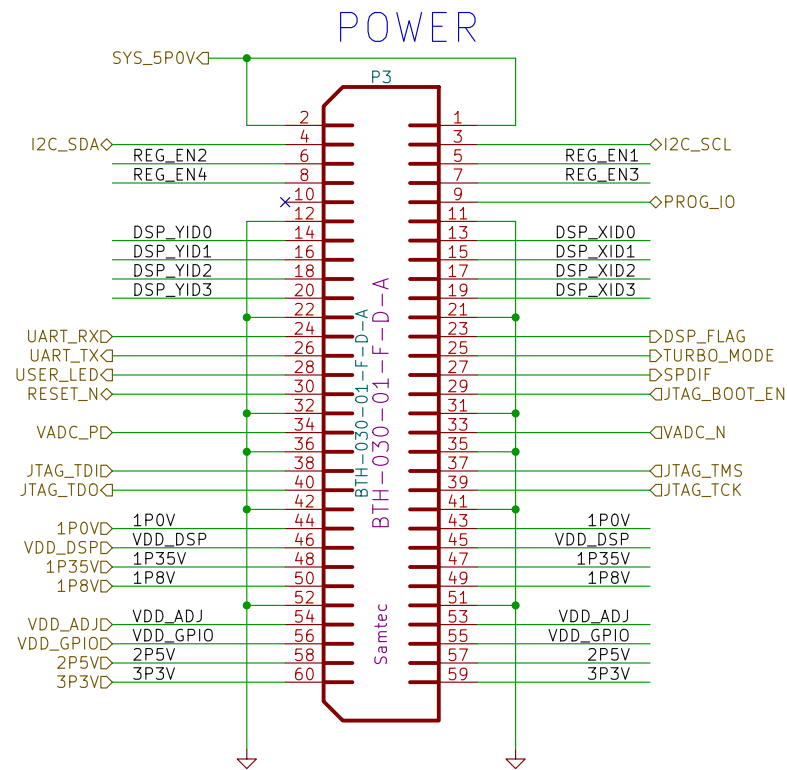
Page: 4/6

Date: 2022-03-24





REG_EN[1..4]↔REG_EN[1..4]
DSP_YID[0..3]↔DSP_YID[0..3]
DSP_XID[0..3]↔DSP_XID[0..3]



COMMENTO
VERSION 1
Paralella MLAB interface board

Title: MPPB01B

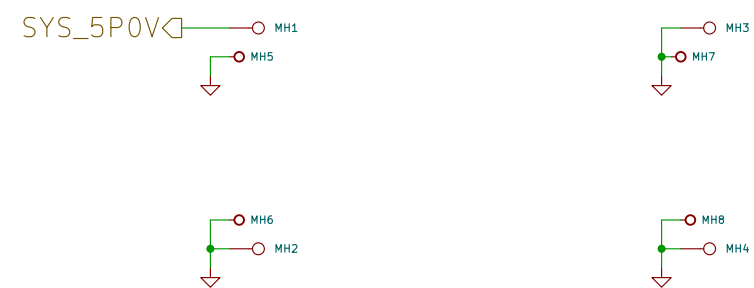
Author: MLAB.cz

Size: B

Page: 5/6

Date: 2022-03-24





COMMENTO
VERSION 1
Paralella MLAB interface board

Title: MPPB01B

Author: MLAB.cz

Size: B

Page: 6/6

Date: 2022-03-24

