EE-337 Project
Multi-cycle RISC

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1. ADD

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

t1 → alu t2 →alu alu → t3	NONE
	ADD
	C-Z
	ALU
	RB

t3 → rf-d3 IR_(5-3) → rf-a3	NONE
	X
	X-X
	STORE_C
	XB

If IR_(5_3)==111

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

2. & 3. ADC/Z

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

If (C/Z==0)

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

If (C/Z==1)

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2	NONE
	X
	X-X
	GET_AB
	QB

t1 → alu t2 →alu alu → t3	NONE
	ADD
	C-Z
	ALU
	RB

t3 → rf-d3 IR_(5-3) → rf-a3	NONE
	X
	X-X
	STORE_C
	XB

If IR_(5_3)==111

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

4. ADI

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

IR(5-0) → sgn-10 → alu t2 → alu alu → t3	NONE
	ADD
	C-Z
	ADDI
	PB

t3 → rf -d3 IR_(7-5) → rf-a3	NONE
	X
	X-X
	STORE_C
	XB

If IR_(5_3)==111

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

5. NDU

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

t1 → alu t2 →alu alu → t3	NONE
	NAND
	X-Z
	ALU
	RB

t3 → rf -d3 IR_(5-3) → rf-a3	NONE
	X
	X-X
	STORE_C
	XB

If IR_(5_3)==111

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

6. & 7. NDC/Z

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

If (C/Z==0)

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

If (C/Z==1)

t1 → alu t2 →alu alu → t3	NONE
	NAND
	X-Z
	ALU
	STORE_C

t3 → rf -d3 IR_(5-3) → rf-a3	NONE
	X
	X-X
	STORE_C
	XB

If IR_(5_3)==111

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

8. LHI

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

IR(8-0) → trail_zero_7 → rf-d3 IR(9-11) → rf-a3	NONE
	X
	X-X
	LHI
	XB

If IR_(5_3)==111

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

9. LW

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

IR(5-0) → sgn-10 → alu t2 → alu alu → t3	NONE
	ADD
	X-X
	ADDI
	PB

t3 → mem_a mem_d → t2 0 → t1	NONE
	X
	X-X
	GET_MEM
	SET_MEM

t1 → alu t2 →alu alu → t3	NONE
	ADD
	X-Z
	ALU
	RB

t3 → rf_d3 IR_(8-6) → t3	NONE
	X
	X-X
	ST_MEM
	XB

If IR_(5_3)==111

10. SW

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

IR_(5-0) → sgn-10 → alu t2 → alu alu → t3	NONE
	ADD
	X-X
	ADDI
	PB

t3 → mem_a t1 → mem_d 111 → rf_a3 PC → rf_d3	DW
	X
	X-X
	SW2
	IB

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

11. LM

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	ADD
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

t1 → mem_a , alu mem_d → t2 +1 → alu alu → t3 t4 → pr.enc → decoder decoder → t5	DR
	ADD
	X-X
	LM2
	TB

If V = 0

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

If V = 1

t2 → rf_d3 t4 →rf_a3,alu t3 → t1 t5 → alu alu → t4	NONE
	X
	X-X
	LM3
	LM2

12. SM

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	ADD
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

t1 → mem_a , alu mem_d → t2 +1 → alu alu → t3 t4 → pr.enc → decoder decoder → t5	DR
	ADD
	X-X
	LM2
	TB

if V = 0

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

if V =1

t4 → pr.enc → rf_a1 rf_d1 → t4 t3 → t1	NONE
	X
	X-X
	SM
	LM5

t4 → mem_d t1 → mem_a	DW
	X
	X-X
	LM5
	LM6

t4 → alu t5 → alu alu → t4	NONE
	XOR
	X-Z
	LM6
	LM2

13. BEQ

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	ADD
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

T1 → ALU T2 → ALU ALU → T3	NONE
	SUB
	C-Z
	ALU
	SB

IF (Z = 0)

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

14. JAL

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

IR_(9_11) → RF_A3 PC → RF_D3, ALU IR_(8_0) → SE7 → ALU ALU → T3	NONE
	ADD
	X-X
	SE7-PC
	T3-PC

111 → RF_A3 T3 → RF_D3	NONE
	X
	X-X
	T3-PC
	IB

IF (Z = 1)

PC → ALU IR_(5-0) → SE10 → ALU ALU → PC	NONE
	ADD
	X-X
	SE10-PC
	SET_PC

PC → ALU IR_(5-0) → SE10 → ALU ALU → PC	NONE
	ADD
	X-X
	SE10-PC
	SET_PC

111 → rf_a3 PC → rf_d3	NONE
	X
	X-X
	SET_PC
	IB

15. JLR

111 → rf-a1 rf-d1 → Mem-a,alu Mem_d → IR +1 → alu alu →PC	IR
	X
	X-X
	HKT
	GET_AB

IR_(11-9) → rf-a1 IR_(8-6) → rf-a2 rf-d1 → t1 rf-d2 → t2 IR_(0-7) → SE(8) → t4	NONE
	X
	X-X
	GET_AB
	SB

PC→ RF_D3 IR_(9_11) → RF_A3 IR_(6_8) → rf_a2 rf_d2→t2	NONE
	X
	X-X
	PC-REG
	T2-PC

T2 → RF_D3 111 → RF_A3	NONE
	X
	X-X
	T2-PC
	IB

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Control Word:

0	Encoding	PC	T1		T2		T3	T4		T5	IR	Memory			ALU			Register File				Type	Next Address
		c0	c1	c2	c3	c4	c5	c6	c7	c8	c9	c10	c11	c12	c13	c14	c15	c16	c17	c18	c19		
1	d001	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	1	IR	SB
2	d002	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	NA	IB
3	d003	0	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DR	S4
4	d004	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	IR	S2
5	d005	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	IR	S6
6	d006	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	DW	IB
7	d007	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	IR	S8
8	d008	0	1	0	1	0	1	0	0	1	0	0	1	0	1	0	0	0	0	0	0	NA	HKT1
9	d009	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	IR	S2
10	d010	0	1	1	0	1	0	0	0	0	0	0	0	0	1	0	1	0	1	1	1	DR	S11
11	d011	0	0	1	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	NA	HK1
12	d012	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	DW	S13
13	d013	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	NA	HKT1
14	d014	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	NA	S15
15	d015	0	1	0	0	0	0	1	1	0	0	1	0	1	0	0	0	0	0	0	0	IR	S2
16	d016	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	NA	HKT1
17	d017	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	NA	BC
18	d018	0	0	0	0	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0	1	DW	S19
19	d019	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	NA	S20
20	d020	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0		

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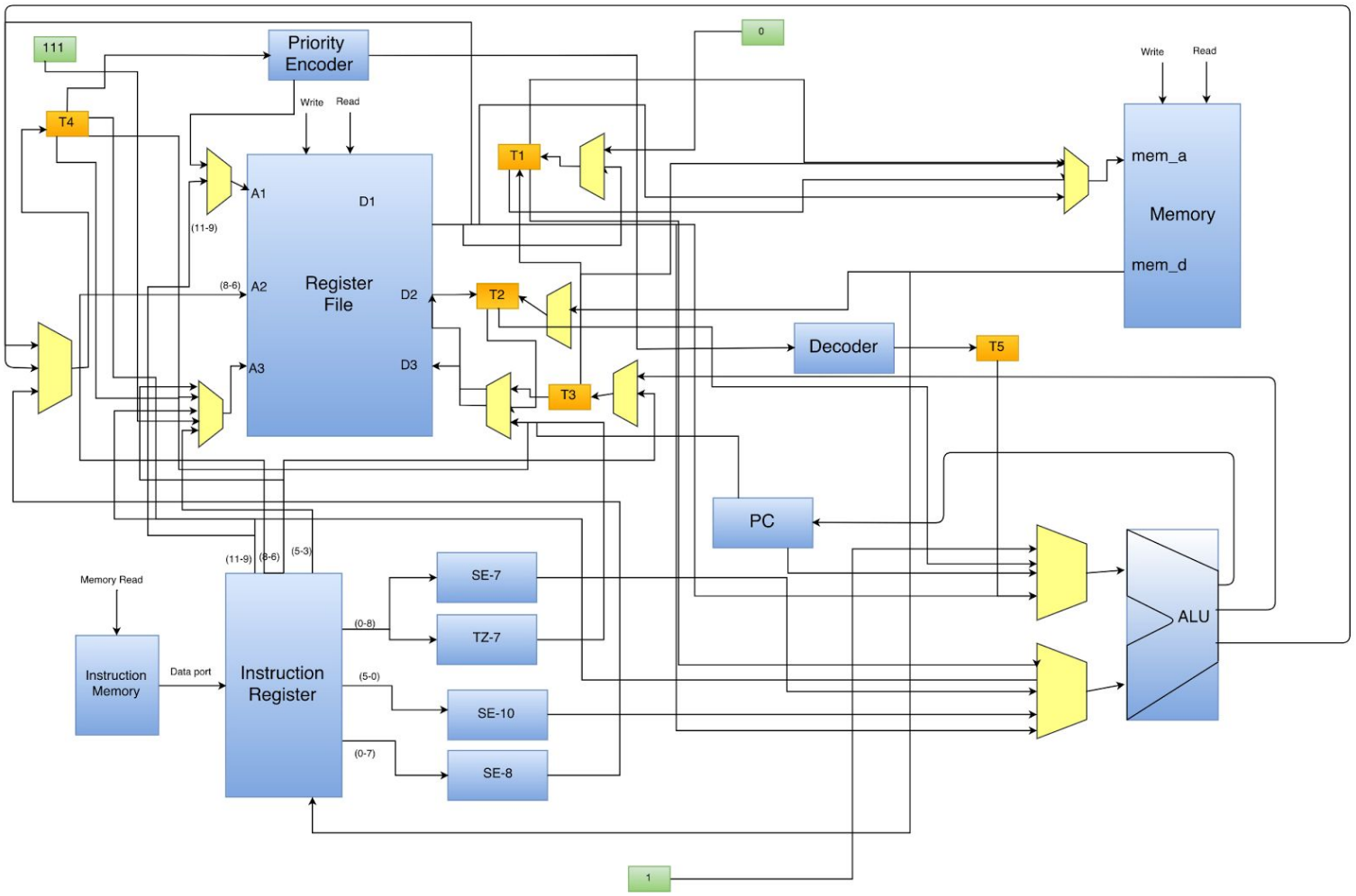
Datapath of the design:



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FSM Diagram:

Here is the FSM diagram of our microprocessor: