

Appendix 2: Microcontroller Layouts and Schematics

Pin	Pin Number	Purpose	Connect to
VDD	7	+ve terminal of supply	+12V
VSS	14	-ve terminal of supply	0V
GND	11	Ground	0V
$\overline{\text{CS}}$	12	Active Low Chip select	SPI slave select (PS7)
$\overline{\text{SHDN}}$	13	Active Low Shutdown	+5V
REFL1 and REFL2	1 & 20	-ve terminal of reference	0V
REFH1 and REFH2	2 & 19	+ve terminal of reference	+5V
DIN	8	Serial digital data input	SPI master data out of HC12 (PS5)
CLK	9	Clock	SPI clock out of HC12 (PS6)
OUT0-OUT7	3-6 & 15-18	Analog output	To processes

Table A2.1 Pin functions and connections of MAX528.

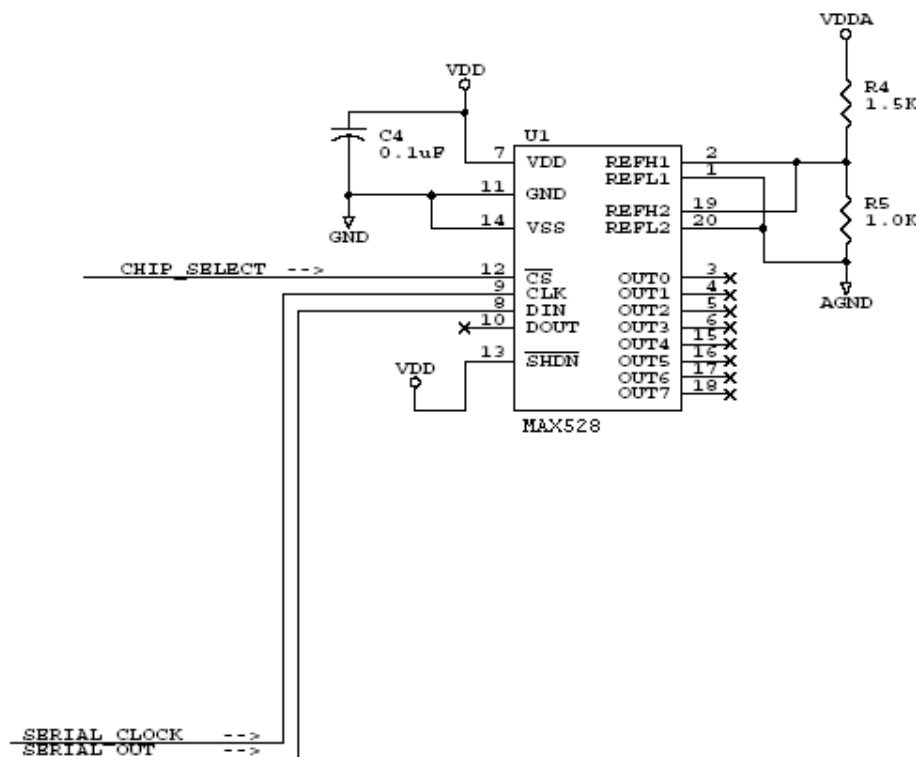


Figure A2.1 Circuit layout connection of MAX528.

		J50			
P3_3V	1	•	•	2	IRQ_B
GND	3	•	•	4	RESET_E
PS<1>	5	•	•	6	PJ<0>
PS<0>	7	•	•	8	PJ<1>
PH<4>	9	•	•	10	PAD<0>
PH<5>	11	•	•	12	PAD<1>
PT<4>	13	•	•	14	PAD<2>
PT<5>	15	•	•	16	PAD<3>
PS<5>	17	•	•	18	PAD<4>
PS<4>	19	•	•	20	PAD<5>
PS<6>	21	•	•	22	PAD<6>
PS<7>	23	•	•	24	PAD<7>
PG<0>	25	•	•	26	PJ<6>
PG<1>	27	•	•	28	PJ<7>
PG<2>	29	•	•	30	PJ<2>
PG<3>	31	•	•	32	PJ<3>
PG<4>	33	•	•	34	PT<6>
PG<5>	35	•	•	36	PT<7>
PG<6>	37	•	•	38	PS<2>
PG<7>	39	•	•	40	PS<3>

Figure A2.2 Pin connections of DEMO9S12NE64 board.

Pin	Label	Signal
1	P3_3V	3.3 VDC supplied from the DEMO9S12NE64
2	IRQ_B	IRQ_B, which is also PE1, is always an input and can always be read. This input is used for requesting an asynchronous interrupt to the MCU. When used as an interrupt pin, this signal is active-low
3	GND	GROUND
4	RESET_B	Active low bidirectional control signal that acts as an input to initialize the MCU to a known start-up state. It also acts as an open-drain output to indicate that an internal failure has been detected in either the clock monitor or COP watchdog circuit
5	PS<1>	PS1 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) transmitter is enabled the PS1 pin is configured as the transmit pin, TXD, of SCI0
6	PJ<0>	PJ0 is a general purpose I/O pin. When the EMAC MII interface is enabled it becomes the management data clock(MII_MDC) signal
7	PS<0>	PS0 is a general purpose input or output. When the Serial Communications Interface 0 (SCI0) receiver is enabled the PS0 pin is configured as the receive pin RXD0 of SCI0
8	PJ<1>	PJ1 is a general purpose I/O pin. When the EMAC MII interface is enabled it becomes the Management Data I/O (MII_MDIO) signal
9	PH<4>	PH4 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit Clock (MII_TXCLK) signal

Table A2.2 Pin functions of DEMO9S12NE64 board.

Pin	Label	Signal
10, 12, 14, 16, 18, 20, 22, 24	PAD<0> - PAD<7>	PAD[7:0] are the analog inputs for the analog to digital converter (ADC). They can also be configured as general purpose digital input
11	PH<5>	PH5 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the transmit Enabled (MII_TXEN) signal
13, 15, 34, 36	PT<4>, PT<5>, PT<6>, PT<7>	PT[7:4] are general purpose input or output pins. When the Timer system 1 (TIM1) is enabled they can also be configured as the TIM1 input capture or output compare pins IOC1[7-4]
17	PS<5>	PS5 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS5 is the master output (during master mode) or slave input (during slave mode) pin (MOSI)
19	PS<4>	PS4 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS4 is the master input (during master mode) or slave output (during slave mode) pin (MISO)
21	PS<6>	PS6 is a general purpose input or output pin. When the Serial Peripheral Interface (SPI) is enabled PS6 becomes the serial clock pin, SCK
23	PS<7>	PS7 is a general purpose input or output. When the Serial Peripheral Interface (SPI) is enabled PS7 becomes the slave select pin SS
25	PG<0>	PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD0) signal
26	PJ<6>	PJ6 is a general purpose input or output pin. When the IIC module is enabled it becomes the Serial Data Line (IIC_SDL) for the IIC module (IIC)
27	PG<1>	PG1 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD1) signal
28	PJ<7>	PJ7 is a general purpose input or output pin. When the IIC module is enabled it becomes the serial clock line (IIC_SCL) for the IIC module (IIC)
29	PG<2>	PG2 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD2) signal
30	PJ<2>	PJ2 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the carrier sense (MII_CRS) signal
31	PG<3>	PG3 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data (MII_RXD3) signal
32	PJ<3>	PJ3 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the collision (MII_COL) signal
33	PG<4>	PG4 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive clock (MII_RXCLK) signal
35	PG<5>	PG5 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive data valid (MII_RXDV) signal
37	PG<6>	PG6 is a general purpose input or output pin. When the EMAC MII interface is enabled it becomes the receive error (MII_RXER) signal
38	PS<2>	PS2 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) receiver is enabled the PS2 pin is configured as the receive pin RXD of SCI1
39	PG<7>	PG7 is a general purpose input or output pin. It can be configured to generate an interrupt(KWG/) causing the MCU to exit STOP or WAIT mode
40	PS<3>	PS3 is a general purpose input or output. When the Serial Communications Interface 1 (SCI1) transmitter is enabled the PS3 pin is configured as the transmit pin, TXD, of SCI1

Table A2.2 Pin functions of DEMO9S12NE64 board (continued).

Pin Functions	Data Direction	Pin Name	Pin Number
Ground	-	GND	3
High	-	P3_3V	1
Demo Board Interface:			
- Run/Load Switch	Input	PG4	33
- SW1	Input	PE0	-
- SW2	Input	PH4	9
- Reset	Input	RESET_B	4
- LED1	Output	PG0	25
- LED2	Output	PG1	27
- Pot	Input	PAD0	10
Analog Outputs:			
MOSI	Output	PS5	17
_SS	Output	PS7	23
SPI Clock	Output	PS6	21
Analog Inputs:			
Analog Channel 0	Input	PAD0	10
Analog Channel 1	Input	PAD1	12
Analog Channel 2	Input	PAD2	14
Analog Channel 3	Input	PAD3	16
Analog Channel 4	Input	PAD4	18
Analog Channel 5	Input	PAD5	20
Analog Channel 6	Input	PAD6	22
Analog Channel 7	Input	PAD7	24
Digital Inputs:			
Digital Input 0	Input	PJ6	26
Digital Input 1	Input	PJ7	28
Digital Input 2	Input	PJ2	30
Digital Input 3	Input	PJ3	32
Digital Input 4	Input	PT6	34
Digital Input 5	Input	PT7	36
Digital Input 6	Input	PS2	38
Digital Input 7	Input	PJ0	6
Digital Outputs:			
Digital Output 0	Output	PG0	25
Digital Output 1	Output	PG1	27
Digital Output 2	Output	PG2	29
Digital Output 3	Output	PG3	31
Digital Output 4	Output	PS4	19
Digital Output 5	Output	PG5	35
Digital Output 6	Output	PG6	37
Digital Output 7	Output	PS1	5

Table A2.3 Pin connections of DEMO9S12NE64 board.