Chapter 6: Ethernet Interface Hardware

(Motorola MC9S12NE64 Ethernet Module)

Ethernet connectivity takes advantage of the very simple TCP/IP protocol set and a microcontroller, thus enabling connectivity from virtually any source with minimal features. To be cost-effective, Ethernet connectivity must be standardized and embedded. Microcontrollers simplify Ethernet networking and bring connectivity to a range of applications. To effectively communicate in these applications, microcontrollers require some fundamental components, including a TCP/IP protocol stack, media access controller (MAC), physical layer (PHY) and sufficient program and data memory resources. The TCP/IP protocol connects the system to the Internet and is the de facto standard of transmitting data over networks. The MAC supports CSMA/CD as defined in the IEEE® 802 standard, and the PHY is a Layer 1 protocol and could be in the form of telephone modem or Ethernet (EPHY).
The Microcontroller used in our project for controlling the real processes as well as an Ethernet Interface is the Motorola MC9S12NE64 microcontroller with Ethernet capability, with the powerful HCS12 core. The MC9S12NE64 Ethernet microcontroller is a single-chip solution that's ideal for affordable embedded connectivity. We used the Freescale demonstration board DEMO9S12NE64 to develop and evaluate our application.

6.1 Motorola MC9S12NE64 Features and Advantages

The MC9S12NE64 is a 112-/80-pin cost-effective, low-end connectivity applications MCU family, it is composed of standard on-chip peripherals including:

- 16-bit central processing unit (HCS12 CPU) which has very interesting features as :

  - Upward compatible with the famous M68HC11 instruction set.
  - Enhanced indexed addressing.
  - Instruction queue.
  - Interrupt control (INT)
  - Multiplexed expansion bus interface (MEBI)
  - Memory map and interface (MMC)
  - Background debug mode (BDM) (Not used in our project)
  - Enhanced debug12 module, including breakpoints and change-of-flow trace buffer (DBG) (Not used in our project)

- 64K bytes of FLASH EEPROM, 8K bytes of RAM.
- Ethernet media access controller (EMAC) with integrated 10/100 Mbps Ethernet physical transceiver (EPHY) which is utilized in our project.
- Two asynchronous serial communications interface modules (SCI), a serial peripheral interface (SPI) which is used for connection with real processes as discussed in the

control section of this documentation. Another serial interface is available which is an inter-IC bus (IIC)

- 4-channel/16-bit timer module (TIM)
- 8-channel/10-bit analog-to-digital converter (ATD), this was used in controlling the real processes as the analog inputs from the processes are converted to digital data so that suitable control action is made, this is discussed in details in the control section of this documentation.
- Up to 21 pins available as keypad wakeup inputs (KWU) for wakeup interrupt function with digital filtering.
- Two additional external asynchronous interrupts.

The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements.

Furthermore, an on-chip bandgap-based voltage regulator (VREG_PHY) generates the internal digital supply voltage of 2.5 V (VDD) from a 3.15 V to 3.45 V external supply range. The MC9S12NE64 has full 16-bit data paths throughout. The 112-pin package version has a total of 70 I/O port pins and 10 input-only pins available.

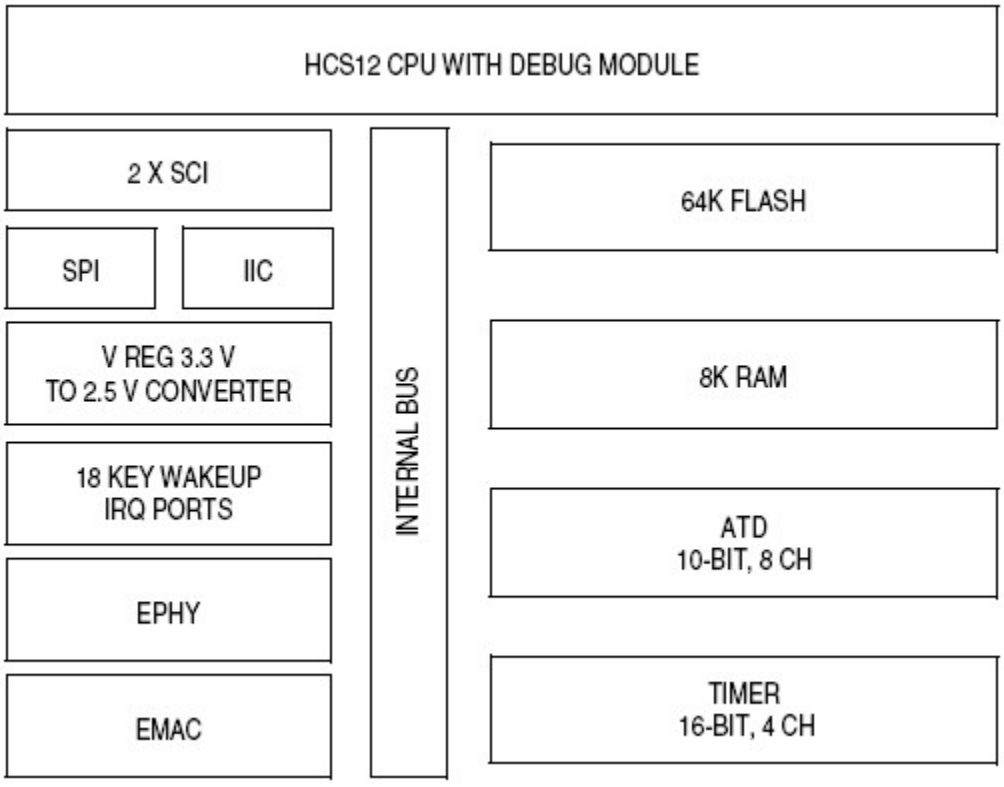

Figure 6.1 Block Diagram of MC9S12NE64 Microcontroller

Ethernet Features:

1- Ethernet Media access controller (EMAC)

- IEEE 802.3 compliant.
- Medium-independent interface (MII)
- Full-duplex and half-duplex modes.
- Flow control using pause frames.
- MII management function.
- Address recognition.
- Frames with broadcast address are always accepted or always rejected.
- Exact match for single 48-bit individual (unicast) address.
- Hash (64-bit hash) check of group (multicast) addresses.
- Promiscuous mode.

2- Ethernet 10/100 Mbps transceiver (EPHY)

- IEEE 802.3 compliant.
- Loop back modes.
- Auto-detection of link capabilities.

3-Two receive and one transmit Ethernet buffer interfaces.

4- Ethertype filter.

5- Loopback mode.

The integrated 10/100 Base-T Ethernet MAC/PHY enables the MC9S12NE64 to keep up with a variety of data rates with flexible memory addressing to support diverse packet sizes. The MC9S12NE64 combines greater processing power and typically larger memory resources (shared 8 KB RAM data/message memory) than an 8-bit solution.

The MC9S12NE64 optimizes the tradeoffs between throughput and memory usage for storing the protocol stack, application code and peripheral drivers, resulting in most of the MCU's resources remaining available for the application. The responsive MC9S12NE64 allows ample time for IP packet disassembly and assembly, for a wide range of IP packet sizes, even in demanding industrial environments. Integrating high internal bus speed and superior addressing modes, such as multi-byte pre/post-decrement indexed addressing, enable the MC9S12NE64 to undertake Ethernet networking and remote monitoring or control which is made in our project.

6.2 Demonstration Board Layout and Specifications

As mentioned before, we used the Freescale demonstration board DEMO9S12NE64 to develop and evaluate our project, it has a Maximum Clock Speed of 25 MHZ at 3.3 V (12.5-MHZ Bus) for 40 ns minimum instruction cycle time, it requires power supply of 6 to 12 VDC 0.75 Amp supplied externally.

The board is supplied with 2 LED's, 2 switches, and an analog input (potentiometer). This was used just for testing and debugging not for real use in the project implementation as the user (client) should be able to control the real-processes remotely via software from a Laptop or a PDA.

The following figures show the top and bottom side layout of the DEMO9S12NE64.

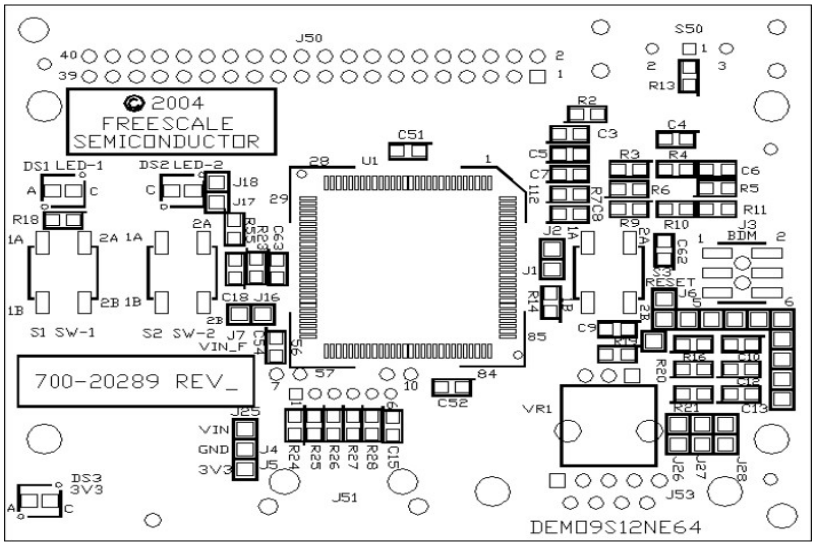

Figure 6.3 DEMO9S12NE64 Top Side

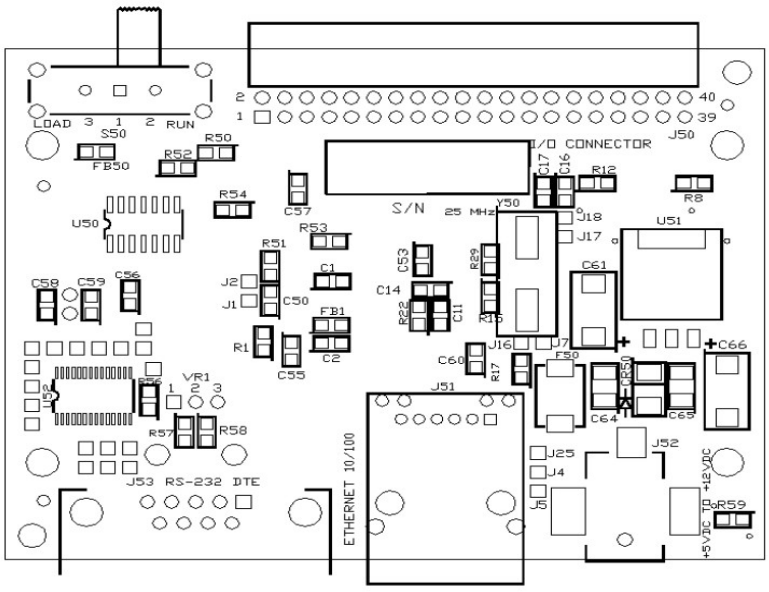

Figure 6.3 DEMO9S12NE64 Bottom Side