Integrated System Architecture
Lab session 3 report - RISC-V special project

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1 Datapath

1.1 Memory

Both instruction and data memory are implemented using a simple behavioral memory model, with both synchronous read and write operations. According to the specifications of the RV32I, instructions are 32-bit long and the biggest addressable unit is also a 32-bit word, so this data with applies in both cases.

Figure 1 shows the interface of this block, where the `address` is left parametric, as it can differ between instructions and data memory. Read and write operations are handled by the couple of control signals `memRead` and `memWrite`, of which only one should be asserted at each clock cycle to perform the desired action. Both signals active represent an forbidden condition and should be avoided by the whatever is in charge of controlling the memory.

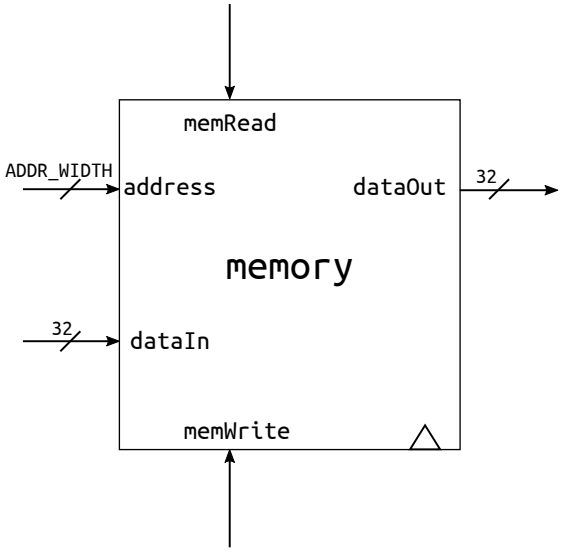

Figure 1: Memory

Figure 2 shows the usual timing diagram of this fully synchronous memory, according to which both reads and writes take place at the next clock cycle after the proper control signals are asserted.

1.2 Register file

The RISC-V register file is composed of 32 registers, each 32-bit wide (for RV32I), called `x0` to `x31`.

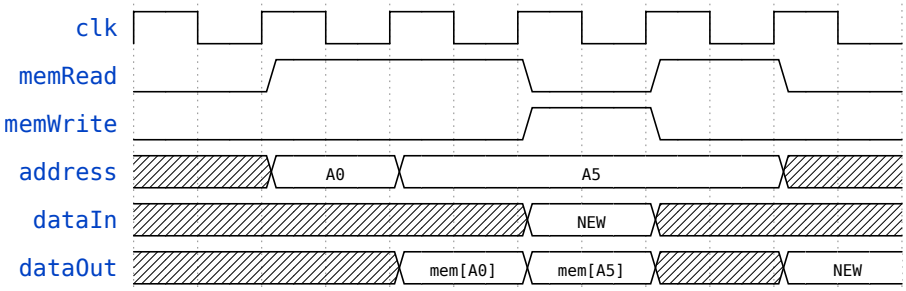

Figure 2: Memory timing diagram

1.3 ALU