Circuit Verification

CS386 Assignment: Group 12

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Assignment Specifications

- A circuit is defined by its input, output, gates and connectivity.
- There is circuit specific knowledge and circuit independent knowledge.
- Circuit independent knowledge is properties of gates (AND, OR, NOT etc) and the meaning of connectivity. You should read all this knowledge into the PROLOG memory.
- However, keep the circuit independent knowledge memory resident.
- The final goal is to verify the input and output in each row of the truth table

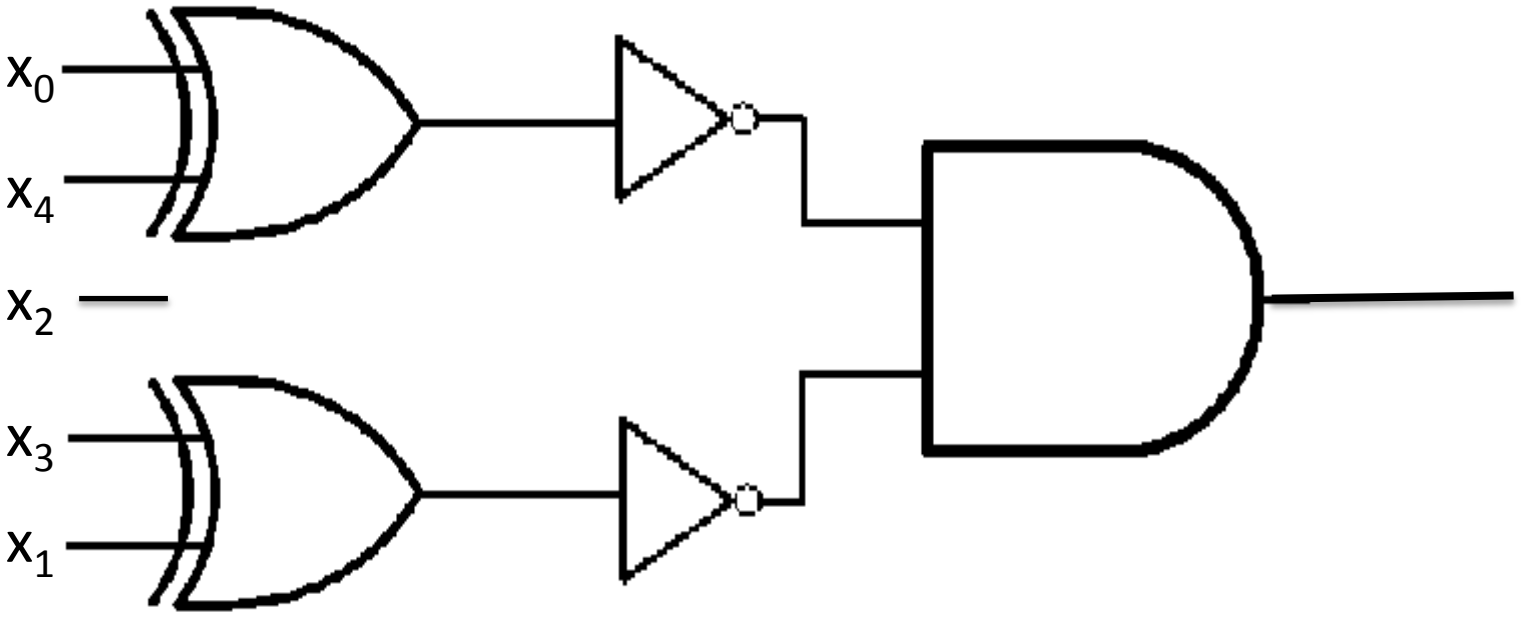
Rules Defined

- type(X, a).
  - a: 'AND', 'OR', 'NOT','XOR'
  - Represents type of gate X
- no_of_inputs(X, val).
  - val : 1, 2, ...
  - Gate X has val inputs
- count_1s(X , num_inputs, val, acc).
  - Counts number of 1s as input to gate X
  - num_inputs: input index to gate X
  - acc: accumulator variable(initialised to zero)
  - val: final result is stored in this variable
- signal(x_n,a).
  - Signal at x_n is a (x_n is input to circuit)

Rules Defined

- in(n,X, val).
  - n^{th} input to gate ‘X’ is ‘val’
- in(n,X).
  - n^{th} input to gate ‘X’
- connected(x1, x2).
  - Used to specify connections in the circuit
  - Eg: connected(x1,in(1,a1))
    - x1 is connected to 1^{st} input of gate a1
- out(X,Val).
  - Output of gate ‘X’ is stored in ‘Val’
- out(X).
  - Output of gate ‘X’

5-input Palindrome Circuit



Output= $\overline{(x_0 \oplus x_4)} \cdot \overline{(x_1 \oplus x_3)}$

5-input Weighted Majority Circuit