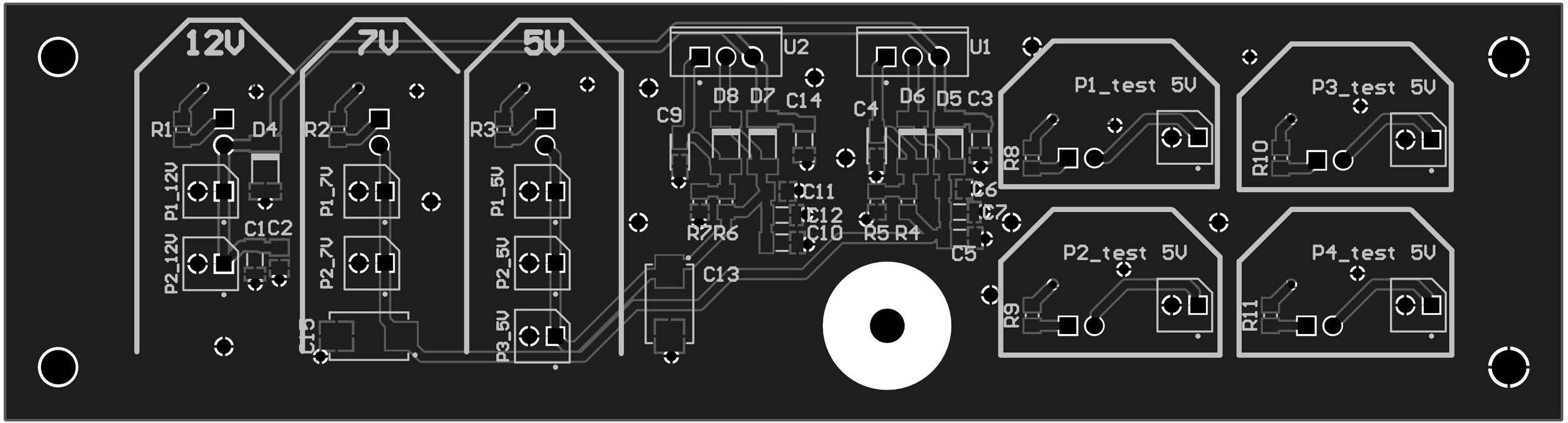
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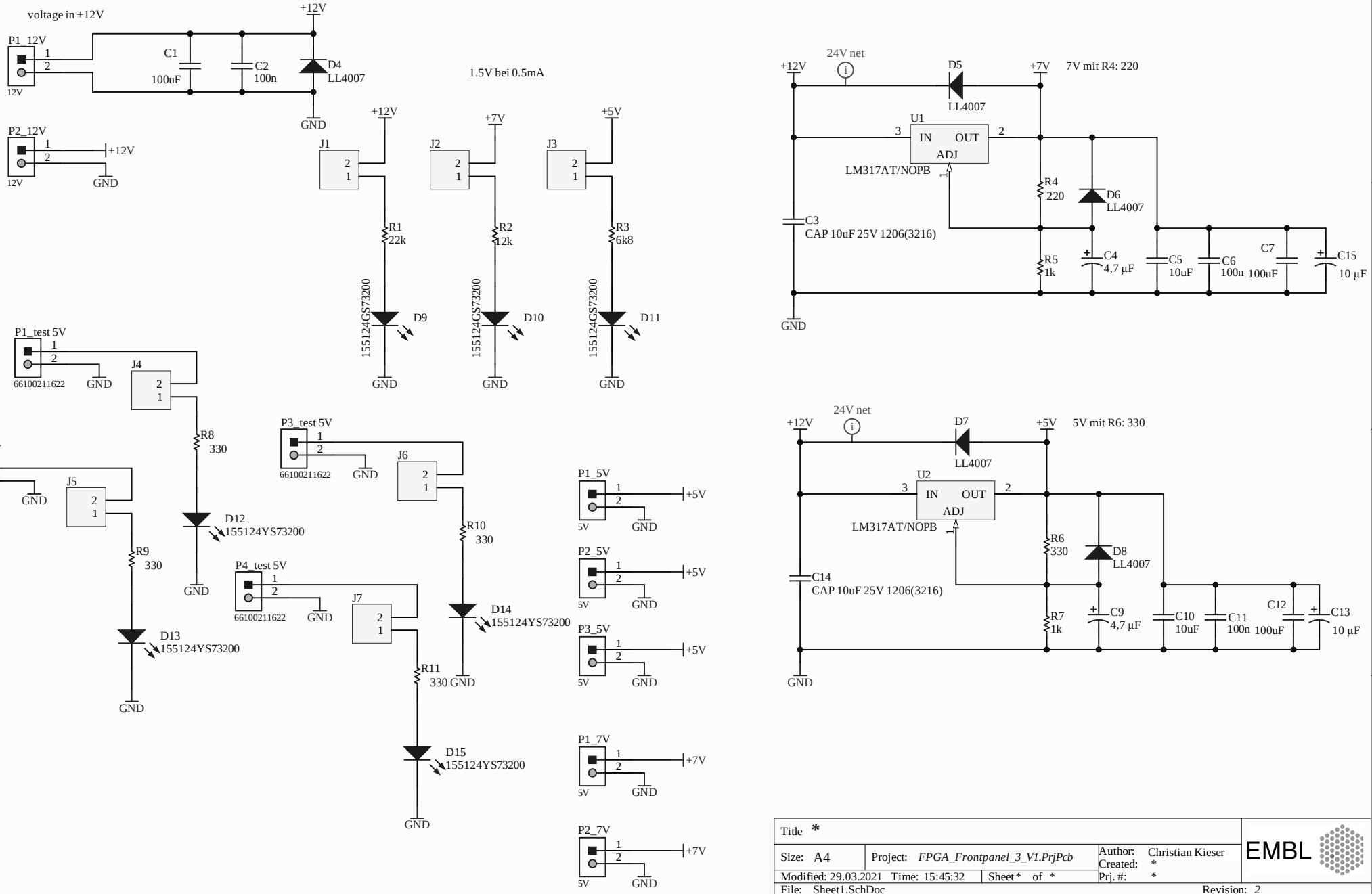
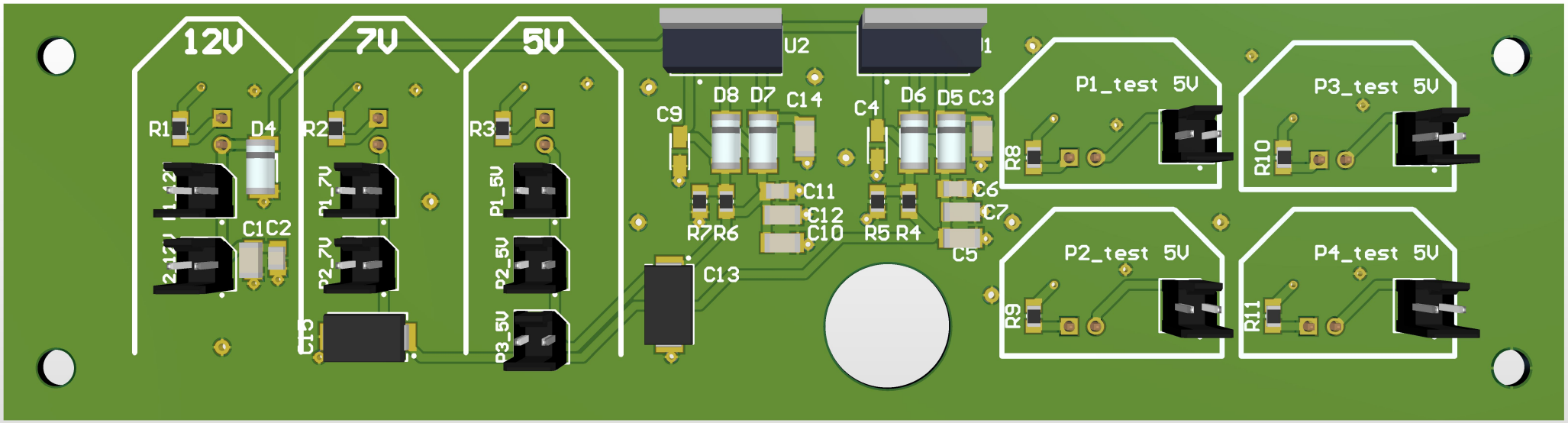
7V
5V
U2
U1
D8 D7 C14
C9
C4
D6 D5 C3
P1_test 5V
P3_test 5V
R1
D4
R2
R3
P1_12V
P2_12V
P1_7V
P2_7V
P1_5V
P2_5V
P3_5V
C11
C6
C12
C7
C10
C5
R7 R6
R5 R4
C1 C2
C13
C15
R8
R10
P2_test 5V
P4_test 5V
R9
R11



Title *			
Size: A4	Project: *FPGA_Frontpanel_3_V1.PrjPcb*	Author: Christian Kieser	EMBL
Modified: 29.03.2021 Time: 15:45:32	Sheet * of *	Created: *	
File: Sheet1.SchDoc		Prj. #: *	
		Revision: *2*	


12V
7V
5V
U2
U1
R1
D4
R2
R3
C9
D8
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R7
R6
R5
R4
C13
C1
C2
P1_7V
P2_7V
P1_5V
P2_5V
P3_5V
P1_test 5V
P3_test 5V
P2_test 5V
P4_test 5V
R8
R10
R9
R11