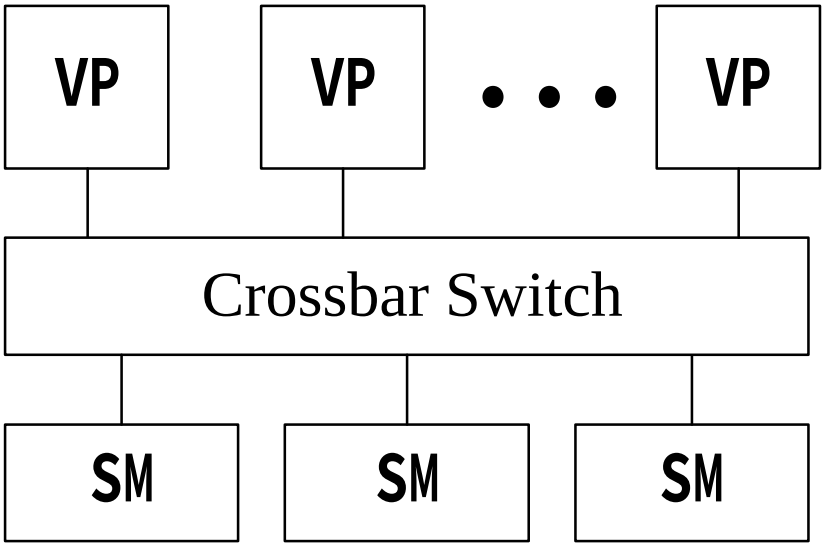
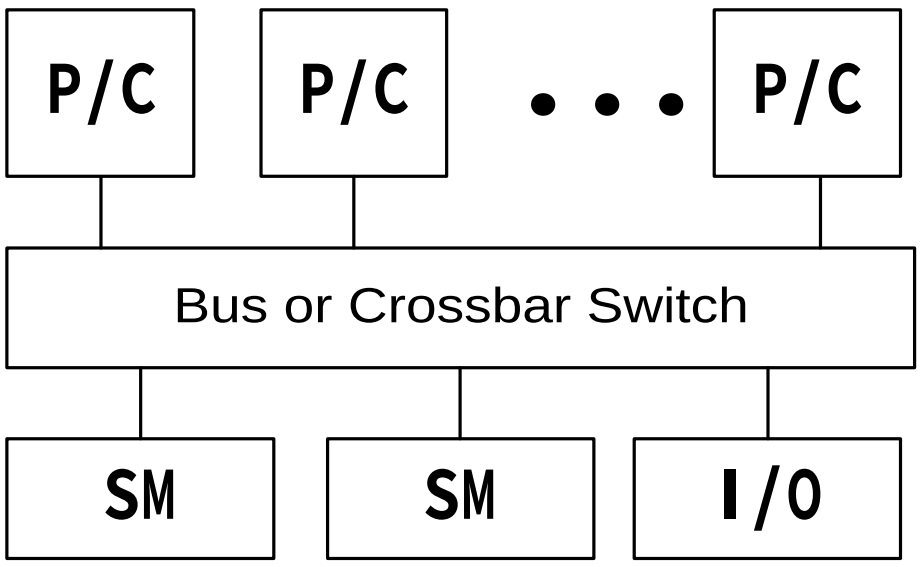
# PVP : Parallel Vector Processors

- **MIMD ,UMA , large grain.**
- **A small number of powerful custom-designed Vector Processors(VP) : ‡1G flops.**
- **A custom-designed high-bandwidth crossbar switch.**
- **A number of shared-memory modules.**
- **A large number of vector registers and instruction buffer without caches normally.**
- **Examples : Cray C-90/T-90, NEC SX-4 , Galaxy-1 etc.**
- **Typical Structure :**



# SMP: Symmetric Multiprocessors

- **MIMD ,UMA , medium grain , higher DOP(Degree of Parallelism).**
- **Commodity microprocessors with on/off-chip caches.**
- **A high-speed snoopy bus or crossbar switch.**
- **Central shared memory.**
- **Symmetric : each processor has equal access to SM(Shared Memory) , I/O and OS services.**
- **Unscalable due to SM and bus.**
- **Examples : SGI Power Challenge , DEC Alpha server 8400, Dawning-1 etc.**
- **Typical Structure :**

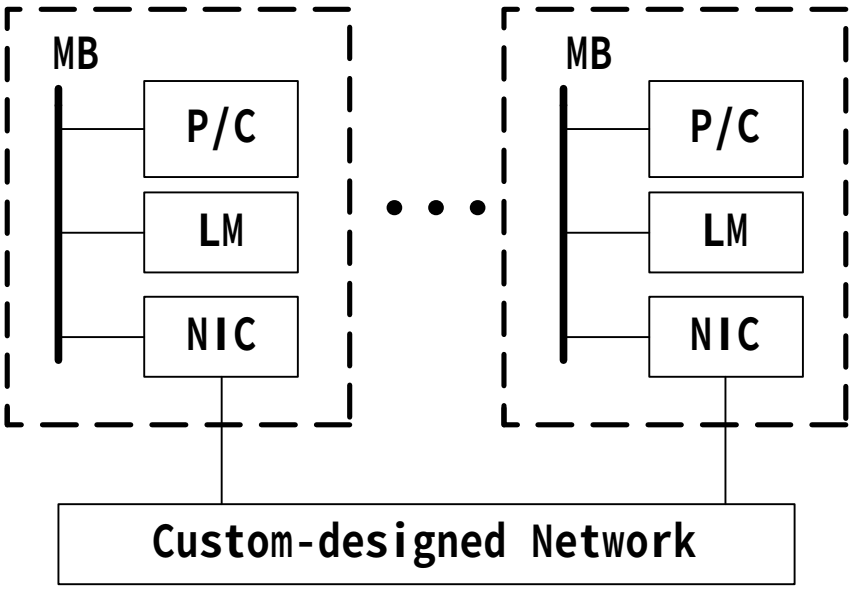


# Comparison of Five Commercial SMP Systems

| System Characteristics | DEC Alphaserver 8400 5/440 | HP 9000/ T600 | IBM RS6000/R40 | Sun Ultra Enterprise 6000 | SGI Power Challenge XL |
|---|---|---|---|---|---|
| No. processors | 12 | 12 | 8 | 30 | 36 |
| Processor type | 437 MHz Alpha 21164 | 180 MHz PA 8000 | 112 MHz PowerPC 604 | 167 MHz UltraSPARC I | 195 MHz MIPS R10000 |
| Off-chip cache per processor | 4 MB | 8 MB | 1 MB | 512 KB | 4 MB |
| Max memory | 28 GB | 16 GB | 2 GB | 30 GB | 16 GB |
| Interconnect bandwidth | Bus 2.1 GB/s | Bus 960 MB/s | Bus + Xbar 1.8 GB/s | Bus + Xbar 2.6 GB/s | Bus 1.2 GB/s |
| Internal disk | 192 GB | 168 GB | 38 GB | 63 GB | 144 GB |
| I/O channels | 12 PCI buses, each 133 MB/s | N/A | 2 MCA, each 160 MB/s | 30 Sbus, each 200 MB/s | 6 Power Channel-2 HIO, each 320 MB/s |
| I/O slots | 144 PCI slots | 112 HP-PB slots | 15 MCA | 45 Sbus slots | 12 HIO slots |
| I/O bandwidth | 1.2 GB/s | 1 GB/s | 320 MB/s | 2.6 GB/s | 320 MB per HIO slot |

# MPP:Massively Parallel Processors

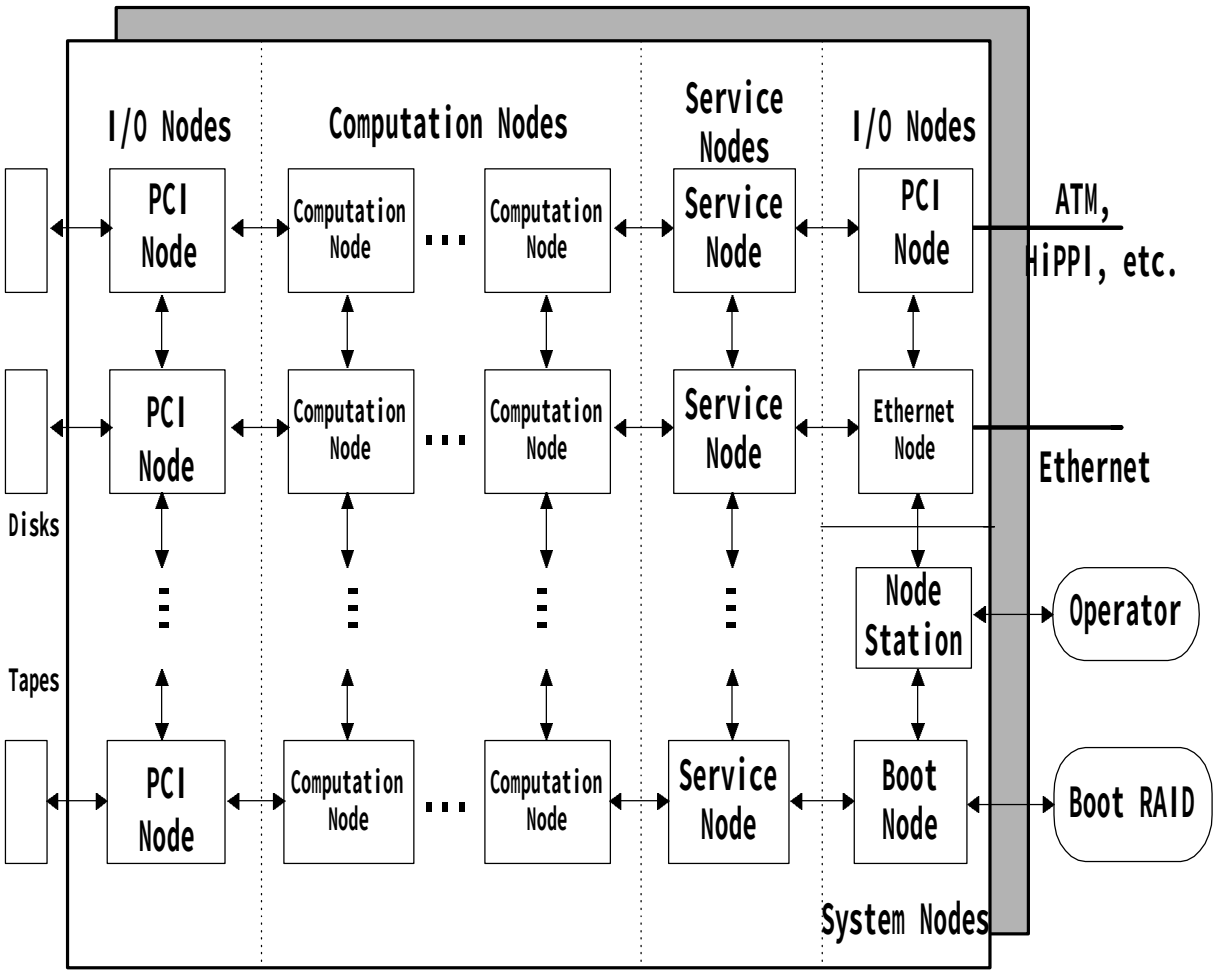
- MIMD, NUMA , medium/large grain .
- A large number of commodity microprocessors .
- A custom-designed high bandwidth , low latency communication network.
- Physically distributed memory( shared or not ).
- May or may not have local disk.
- Synchronized through blocking message-passing operations.
- Examples : Intel Paragon , IBM SP2,Dawning-1000 etc.
- Typical Structure :



# Comparison of three MPP systems

| MPP Models | Intel/Sandia ASCI Option Red | IBM SP2 | SGI/Cray Origin2000 |
|---|---|---|---|
| A Large sample configuration | 9072 processors, 1.8 Tflop/s at SNL | 400 processors,100 Gflop/s at MHPCC | 128 processors, 51 Gflop/s at NCSA |
| Available date | December 1996 | September 1994 | October 1996 |
| Processor type | 200 MHz, 200 Mflop/s Pentium Pro | 67 MHz, 267 Mflop/s POWER2 | 200 MHz, 400 Mflop/s MIPS R10000 |
| Node architecture and data storage | 2 processors, 32 to 256 MB of memory, shared disk | 1 processor, 64 MB to 2 GB local memory, 1-4.5GB Local disk | 2 processors, 64 MB to 256 GB of DSM and shared disk |
| Interconnect and memory model | Split 2D mesh, NORMA | Multistage network, NORMA | Fat hypercube, CC-NUMA |
| Node operating system | Light-weighted kernel (LWK) | Complete AIX (IBM Unix) | Microkernel Cellular IRIX |
| Native programming mechanism | MPI based on PUMA Portals | MPI and PVM | Power C Power Fortran |
| Other programming models | Nx, PVM, HPF | HPF, Linda | MPI, PVM |

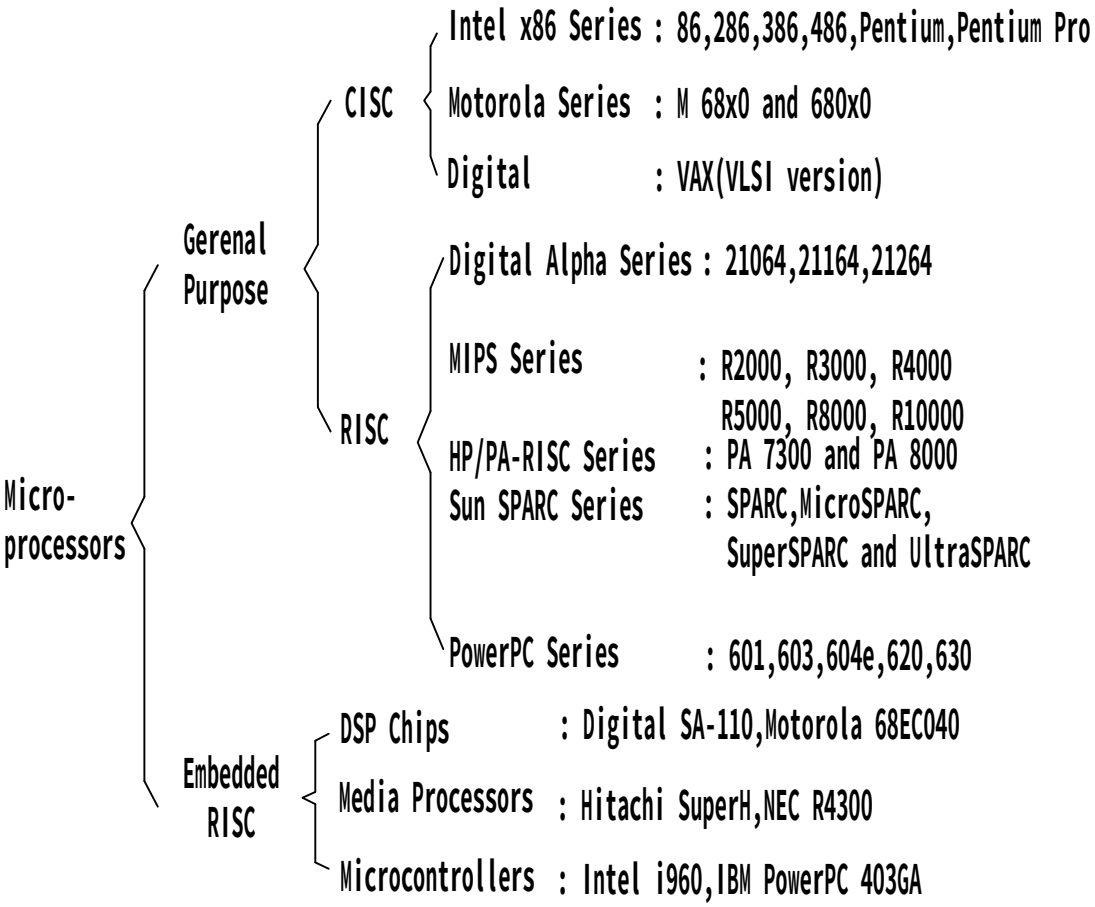
# ASCI Option-Red System



# High-Performance CPU Chips for MPP

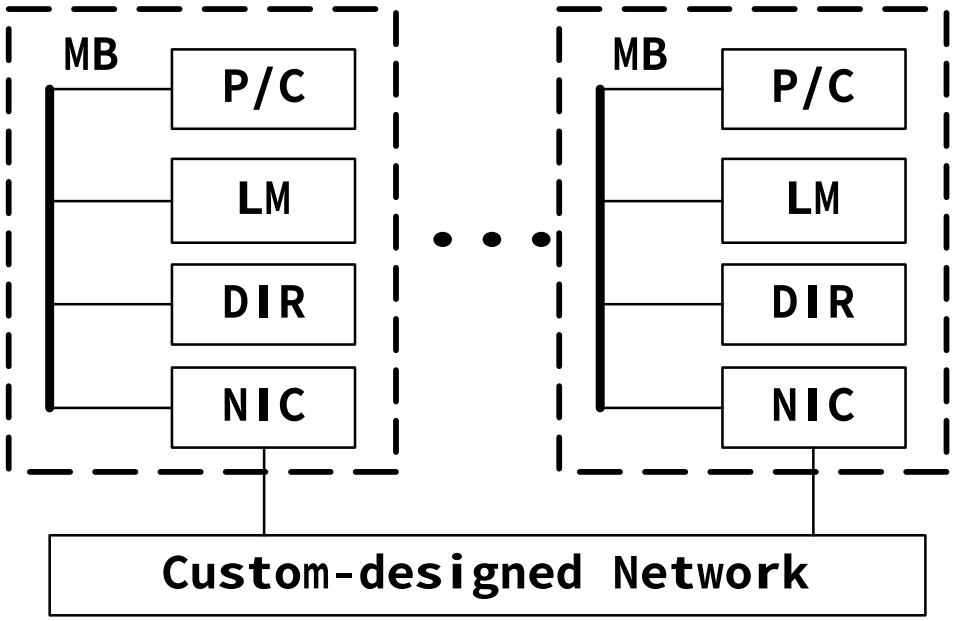
| Attribute | Pentium Pro | PowerPC 620 | Alpha 21164A | UltraSPARC II | MIPS R10000 |
|---|---|---|---|---|---|
| Technology | BiCMOS | CMOS | CMOS | CMOS | CMOS |
| Transistors | 5.5 M/15.5 M | 7 M | 9.6 M | 5.4 M | 6.8 M |
| Clock Rate | 150 MHz | 133 MHz | 417 MHz | 200 MHz | 200 MHz |
| Voltage | 2.9 V | 3.3 V | 2.2 V | 2.5 V | 3.3 V |
| Power | 20 W | 30 W | 20 W | 28 W | 30 W |
| Word Length | 32 bits | 64 bits | 64 bits | 64 bits | 64 bits |
| I/D Cache | 8KB/8KB | 32 KB/32 KB | 8 KB/8 KB | 16 KB/16KB | 32 KB/32KB |
| L2 Cache | 256 KB on a multi-chip module | 1-128 MB off-chip | 96 KB on-chip | 16 MB off-chip | 16 MB off-chip |
| Execution Units | 5 units | 6 units | 4 units | 9 units | 5 units |
| Superscalar | 3 way | 4 way | 4 way | 4 way | 4 way |
| Pipeline depth | 14 stages | 4-8 stages | 7-9 stages | 9 stages | 5-7 stages |
| SPECint92 | 366 | 225 | >500 | 350 | 300 |
| SPECfp92 | 283 | 300 | >750 | 550 | 600 |
| SPECint95 | 8.09 | 225 | >11 | NA | 7.4 |
| SPECfp95 | 6.70 | 300 | >17 | NA | 15 |
| Special Features | CISC/RISC hybrid, 2-level speculative execution | Short pipelines, large L1 caches | Highest clock rate and density with on-chip L2 cache | Multimedia and graphics instructions | MP cluster bus supports up to 4 CPUs |

# Microprocessor Families and Representative CPU Chips



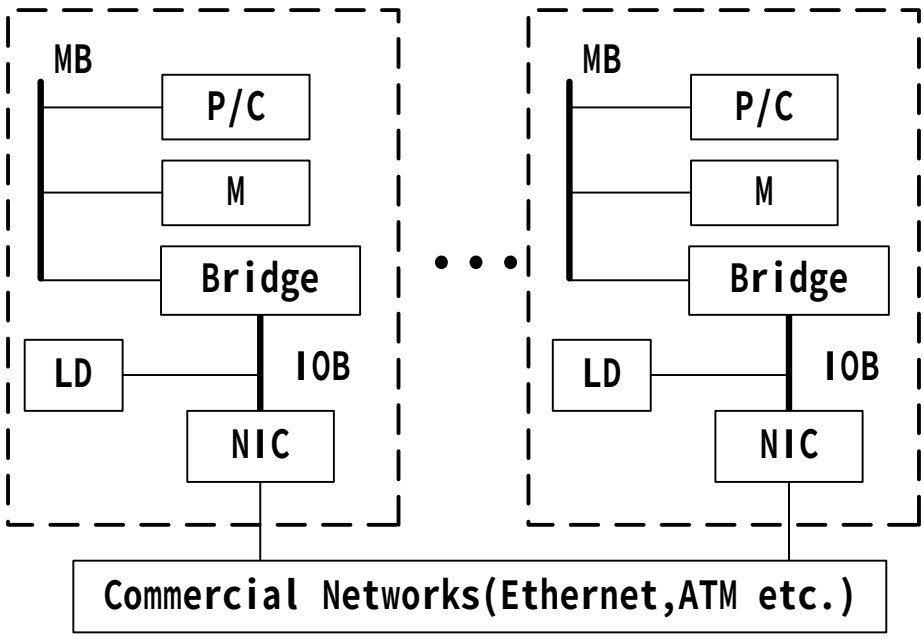
# DSM : Distributed Shared-Memory

- **MIMD , NUMA, NORMA, large grain.**
- **Memory physically distributed , but system hardware and software support a single address space to application users.**
- **DIR( Cache directory ) is used to support distributed coherent caches.**
- **A custom-designed communication network.**
- **Shared-memory programming style.**
- **Examples : Stanford DASH , Cray T3D etc.**
- **Typical Structure :**



# COW : Cluster Of Workstations

- **MIMD , NUMA , coarse grain.**
- **Distributed memory.**
- **Each node of COW is a complete computer ( SMP or PC) sometimes called headless workstation.**
- **A low-cost commodity network.**
- **There is always a local disk.**
- **A complete OS resides on each node , whereas MPP only a microkernel exists.**
- **Examples : Berkeley NOW ,Alpha Farm ,FXCOW etc.**
- **Typical Sturcture :**



# Representative of COW Research Projects

| Project/Reference | Special Features to Support Clustering |
|---|---|
| Berkeley NOW Project | A serverless network of workstations featured with active messaging, cooperative filing, and global Unix extensions |
| Princeton SHRIMP | Commodity components, efficient communication and shared virtual memory through special network interfaces |
| Karsruhe Parastaion | Efficient communication network and software development for distributed parallel processing |
| Rice TreadMarks | Software-implemented distributed shared-memory cluster of workstations |
| Wisconsin Wind Tunnel | Distributed shared memory on a cluster of workstations interconnected with a commodity network |
| The NSCP http://nscp.upenn.edu | National Scalable Cluster Project for metacomputing over three local clusters linked through Internet. |
| Argonne Globus | Developing metacomputing platform and software through an ATM-connected WAN of 17 sites in North America |
| Syracuse WWVM | A World-Wide Virtual Machine for high-performance computing with Internet and HPCC technologies |
| PearlCluster http://pearl.cs.hku.hk | A research cluster for distributed multimedia and financial digital library applications |
| Virginia Legion | Developing metacomputing software towards a national virtual computer facility |

# Comparison of MPP,SMP, COW & DSM

| System Characteristic | MPP | SMP | Cluster | Distributed System |
|---|---|---|---|---|
| Number of nodes (*N*) | *O*(100)-*O*(1000) | *O*(10) or less | *O*(100) or less | *O*(10)-*O*(1000) |
| Node complexity | Fine or medium grain | Medium or coarse grain | Medium grain | Wide range |
| Internode communi-cation | Message passing or shared variables for DSM | Shared memory | Message passing | Shared files, RPC, message passing |
| Job scheduling | Single run queue at host | Single run queue | Multiple queues but coordinated | Independent multiple queues |
| SSI support | Partially | Always | Desired | No |
| Node OS copies and Type | N (microkernel) and 1 host OS (monolithic) | One (monolithic) | *N* (homogeneous desired) | *N* (heterogenous) |
| Address space | Multiple (single if DSM) | Single | Multiple | Multiple |
| Internode security | Unnecessary | Unnecessary | Required if exposed | Required |
| Ownership | One organization | One organization | One or more organizations | Many organizations |
| Network protocol | Nonstandard | Nonstandard | Standard or nonstandard | Standard |
| System availability | Low to medium | Often low | Highly available or fault-tolerant | Medium |
| Performance metric | Throughput and turnaround time | Turnaround time | Throughput and turnaround time | Response time |

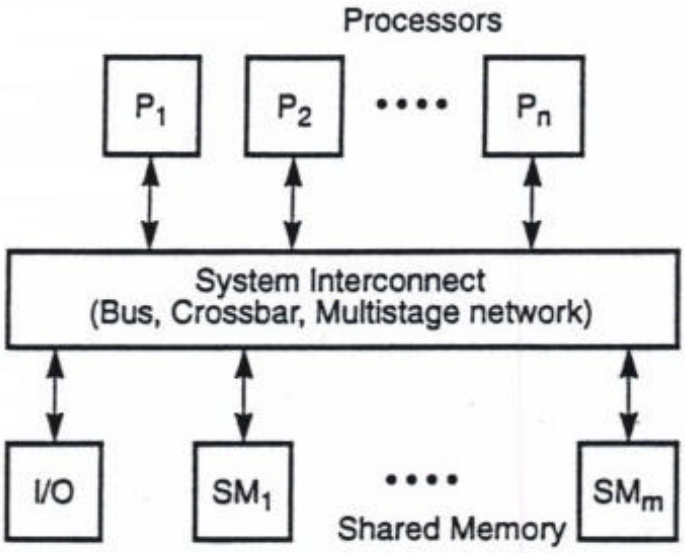
SSI: Single-system image, RPC: Remote procedure call, DSM: Distributed shared memory

## Architectural Attributes

| Attribute | PVP | SMP | DSM | MPP | COW |
|---|---|---|---|---|---|
| Example Systems | Cray C-90, Cray T-90 | Cray CS6400, DEC 8000 | DASH Cray T3D | Intel Paragon IBM SP2 | Berkeley NOW, Alpha Farm |
| Processor Type | Custom Vector Processor | Commodity Microprocessor | Commodity Microprocessor | Commodity Microprocessor | Commodity Microprocessor |
| Memory model | Centralized Shared | Centralized Shared | Distributed Shared | Distributed Unshared | Distributed Unshared |
| Address Space | Single | Single | Single | Multiple | Multiple |
| Access Model | UMA | UMA | NUMA | NORMA or NUMA | |
| Interconnect | Custom Crossbar | Bus or Crossbar | Custom Network | Custom Network | Commodity Network |

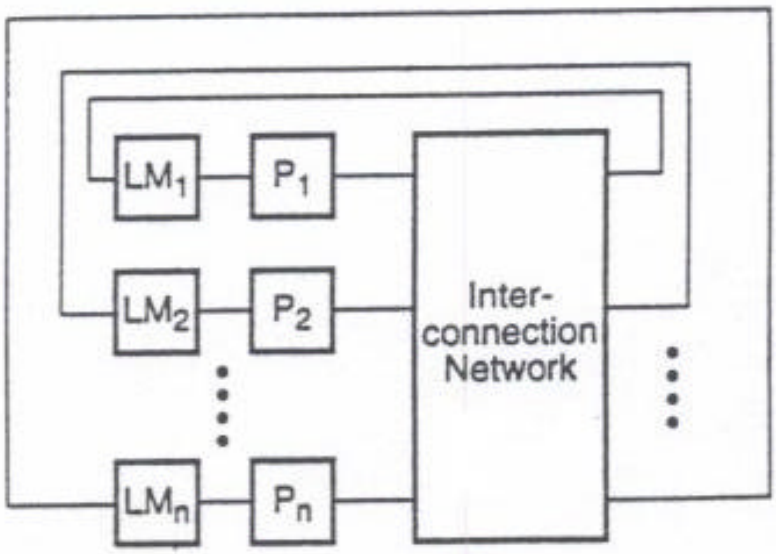
# Uniform Memory Access ( UMA )

- Physical memory is uniformly shared by all processors.
- All processors have equal access time to all memory words.
- UMA is suitable for general-purpose or time-sharing applications.
- UMA multiprocessor model is the following:

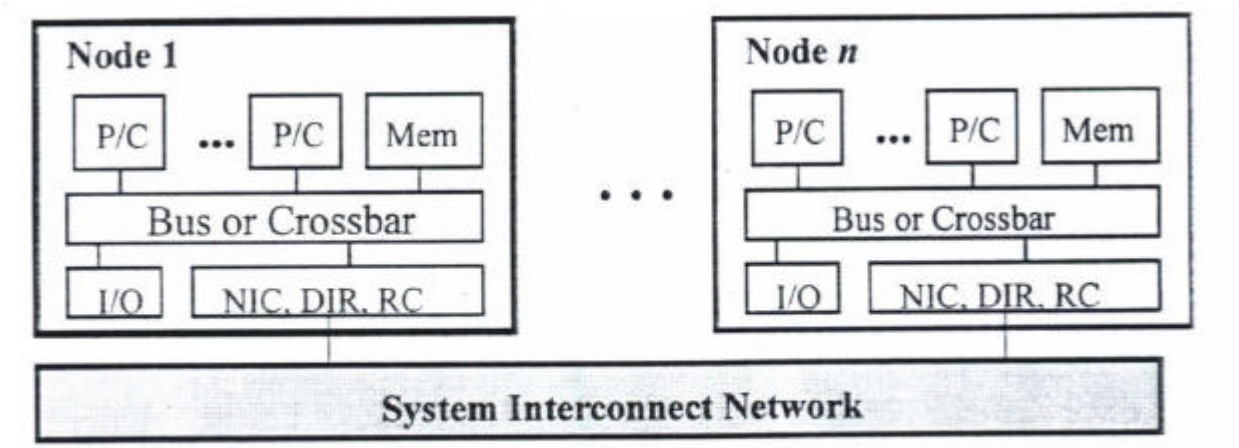


# Non-Uniform Memory Access (NUMA)

- SM is collection of all LM of processors, i.e shared local memories.
- The access time varies with location of memory words: shorter to access processor own LM; longer to access remote LM of other processor.
- Shared local memory model is the following:



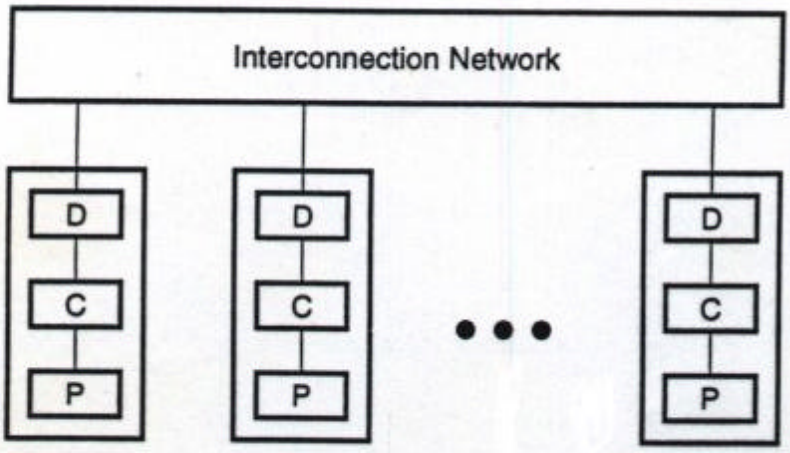
# CC-NUMA System




**CC-NUMA architecture** (DIR: Cache Directory, NIC: Network Interface Circuitry, RC: Remote Cache)

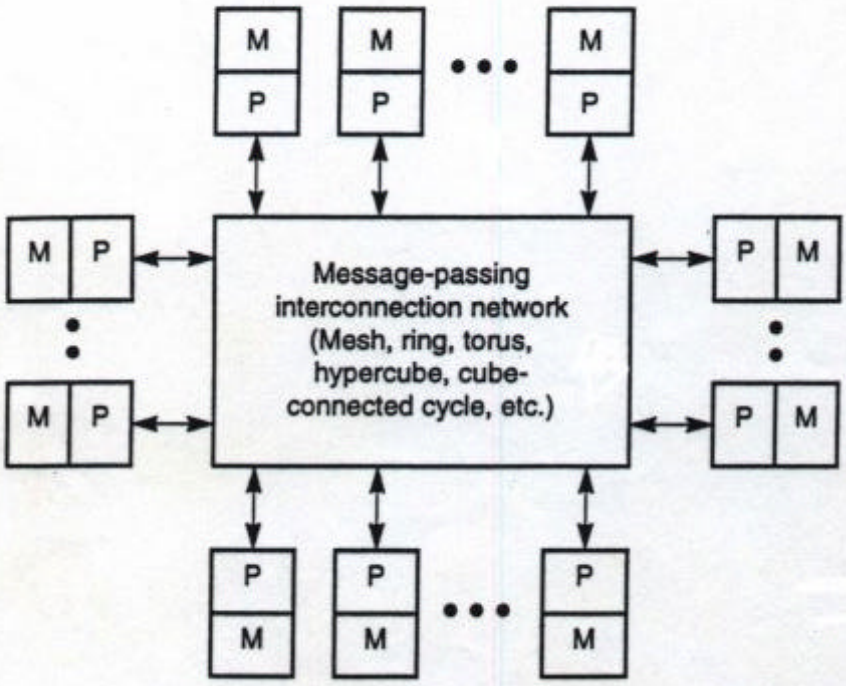
# Cache -Only Memory Access (COMA)

- COMA model is a special case of NUMA in which the distributed memories are converted to caches.
- All caches form a global address space.
- Remote cache access is assisted by the distributed cache directories.
- COMA multiprocessor model is the following:

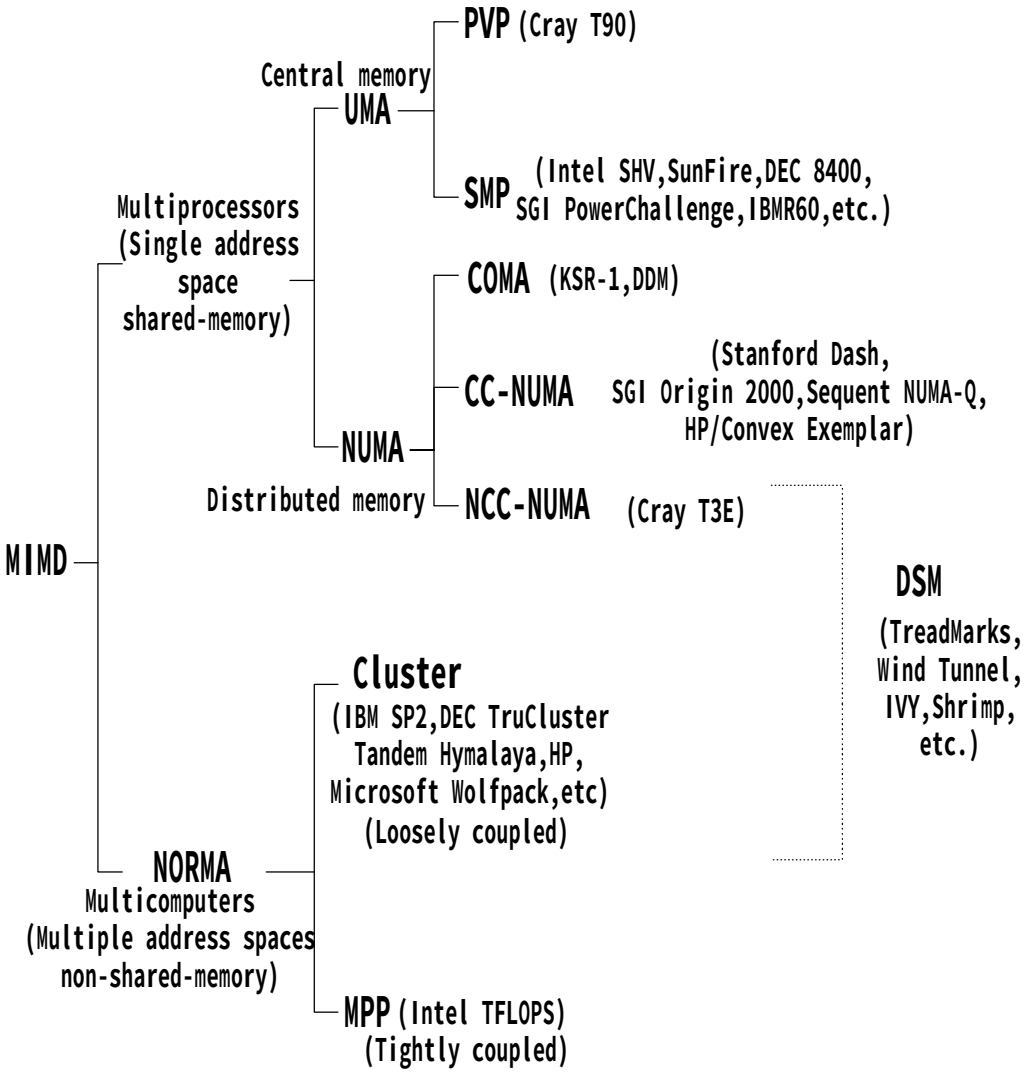


# NO-Remote Memory Access (NORMA)

- A distributed memory multicomputer system is called NORMA model if all memories are private and accessible only by local processors.
- Most of NUMA model supports no-remote memory access.
- In DSM system, NORMA will disappear.
- Generic model of message passing multicomputer is the following:

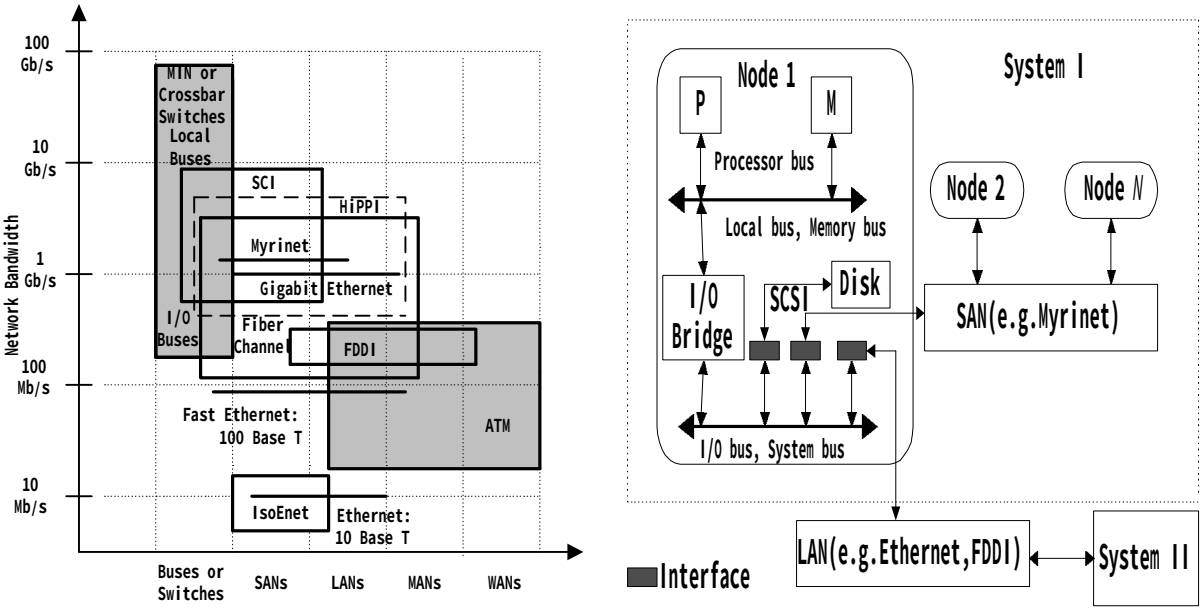


# Architectures & Memory Access Models



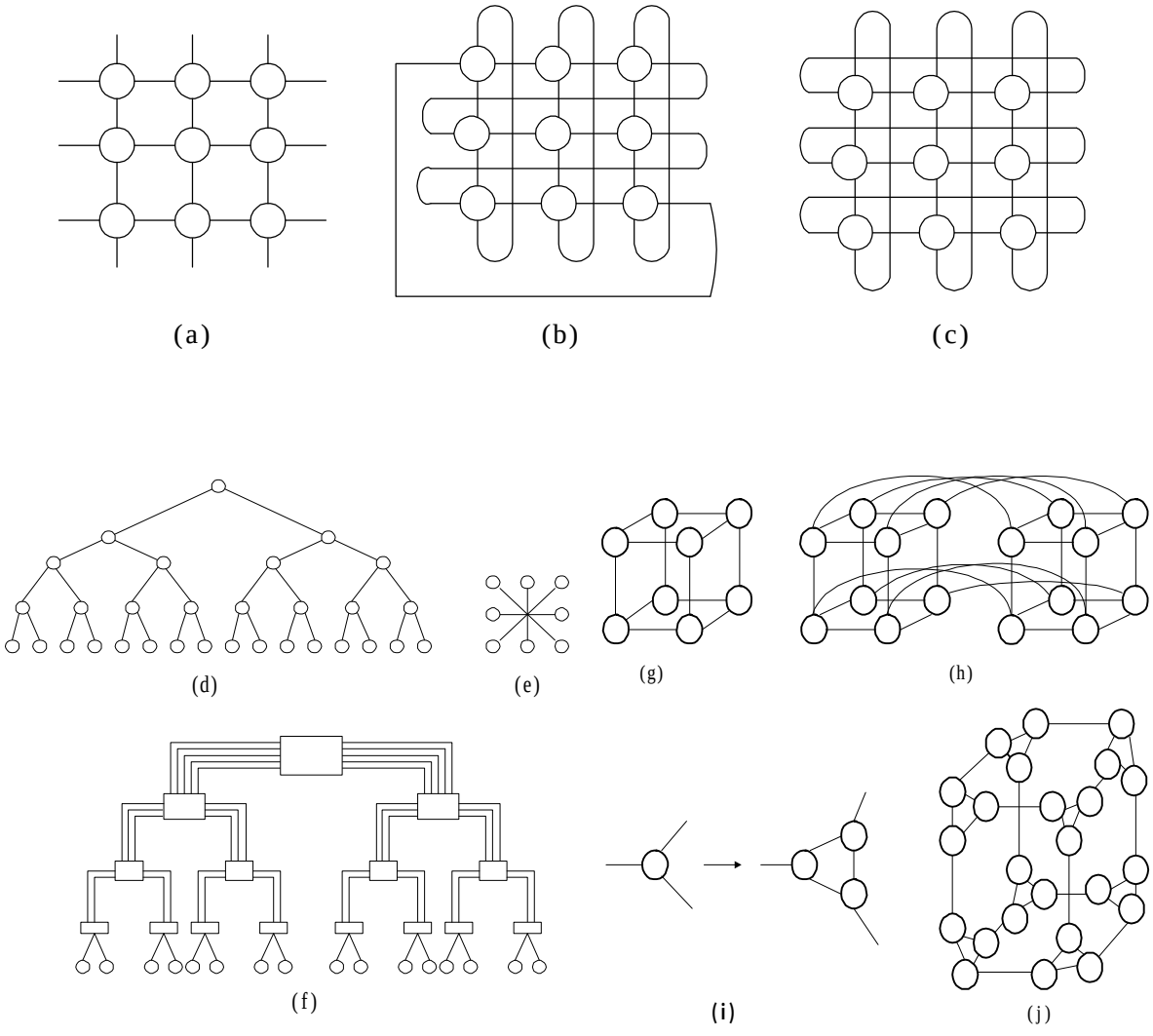
# Five Networking Environments

- **Buses: including processor bus, memory bus, I/O bus etc. They are often built on a motherboard, backplane limited to 2m.**
- **SAN(System Area Network): to connect a number of nodes to form a single system within a short distance (3-25m).**
- **LAN(Local Area Network): to confine within a building, a campus or an enterprise (25-500m), and to connect multiple systems.**
- **MAN(Metropolitan Area Network): to cover a whole district or within a city limit (£25km).**
- **WAN(Wide Area Network): to appear as an inter-network of a number of smaller networks to realize meta-computing.**



# Static-Connection Networks (1)

- **Network Topology: Linear array, Ring, Mesh, Tree, Hypercube, CCC.**



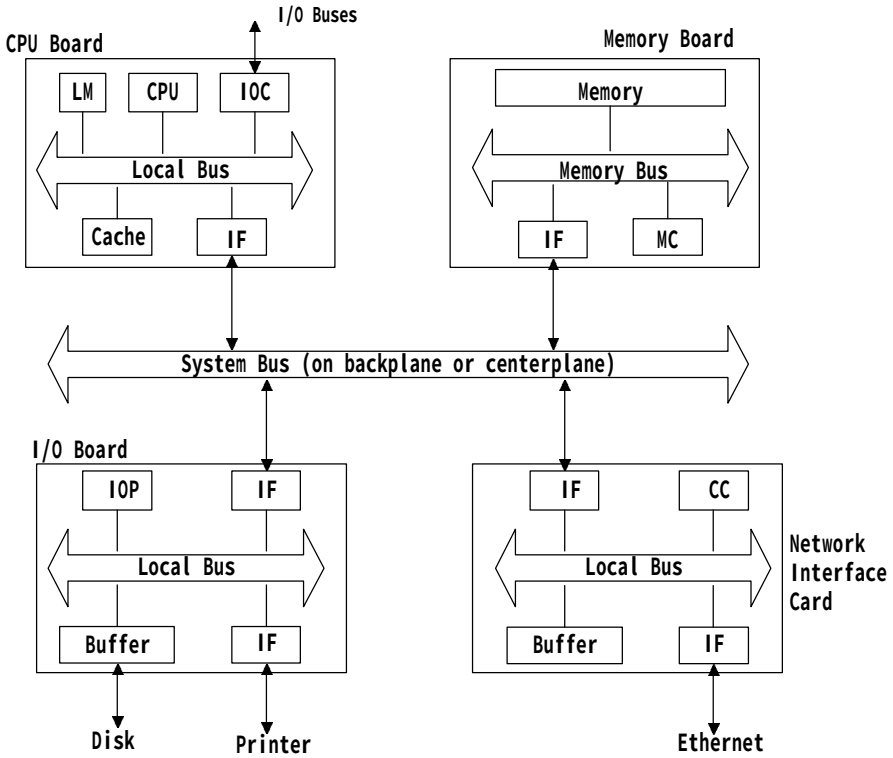
# Static-Connection Networks (2)

## ☞ Comparison of Static-Connection Networks :

| Network Type | Node Degree *d* | Network Diameter *D* | No. of Links *l* | Bisection Width *B* | Symme-try | Network Size and Remarks |
|---|---|---|---|---|---|---|
| Linear array | 2 | *N-1* | *N-1* | 1 | No | *N* nodes |
| Ring | 2 | *N/2* | N | 2 | Yes | *N* nodes |
| Completely connected | *N-1* | 1 | $\frac{N(N-1)}{2}$ | $(N/2)^2$ | Yes | *N* nodes |
| Binary tree | 3 | 2*(h-1)* | *N-1* | *1* | No | Tree height h=Ølong$_2$NØ |
| Star | *N-1* | 2 | *N-1* | *N/2* | No | *N* nodes |
| 2D Mesh | 4 | *2(r-1)* | *2N-2r* | r | No | *r*· *r* mesh for $r=N^{1/2}$ |
| Illiac Mesh | 4 | *r-1* | *2N* | *2r* | No | Chordal ring with $r=N^{1/2}$ |
| 2D Torus | 4 | 2Ø*r*/2ø | *2N* | *2r* | Yes | *r*· *r* torus for $r=N^{1/2}$ |
| Hypercube | *n* | *n* | *nN/2* | *N/2* | Yes | $N=2^n$ nodes |
| CCC | *3* | *2k-1+* Ø*k*/2ø | *3N/2* | *N/(2k)* | Yes | $N=k2^k$ nodes with cycle k‡3 |
| *k*-ary *n*-*cube* | 2n | *n* Ø*k*/2ø | *nN* | $2k^{n-1}$ | Yes | $N=k^n$ nodes |

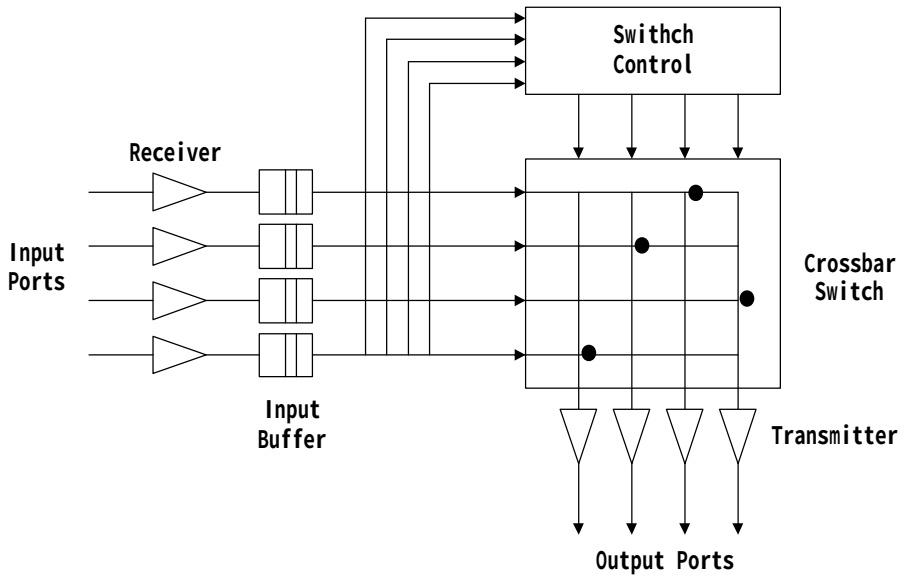
# Dynamic-Connection Networks (1)

- **Bus :**
  - **System bus (I/O bus): used for data transfer between master device (processor) and slave devices (memory etc.) on backplane or centerplane.**
  - **Local bus: on a memory board is called memory bus.**



# Dynamic-Connection Networks (2)

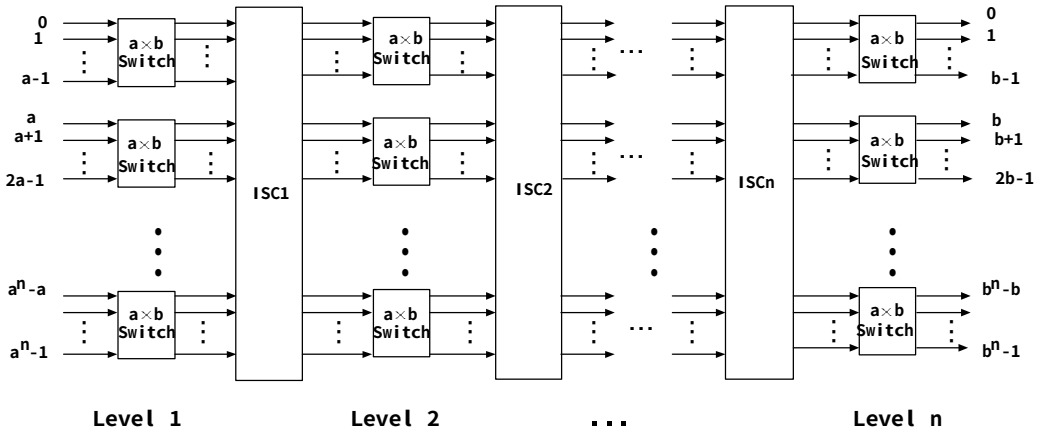
- **Crossbar Switches :**
  - **A single-stage switched network.**
  - **Complexity = $n^2$, n is the number of ports.**
  - **Crosspoint switches provide dynamic connections between all (source, destination) pairs. The crosspoint switches can be set on or off dynamically upon program control.**
  - **Two ways of using crossbar switches: inter-processor communication (ex. COW) and inter-processor-memory access (ex. SMP).**

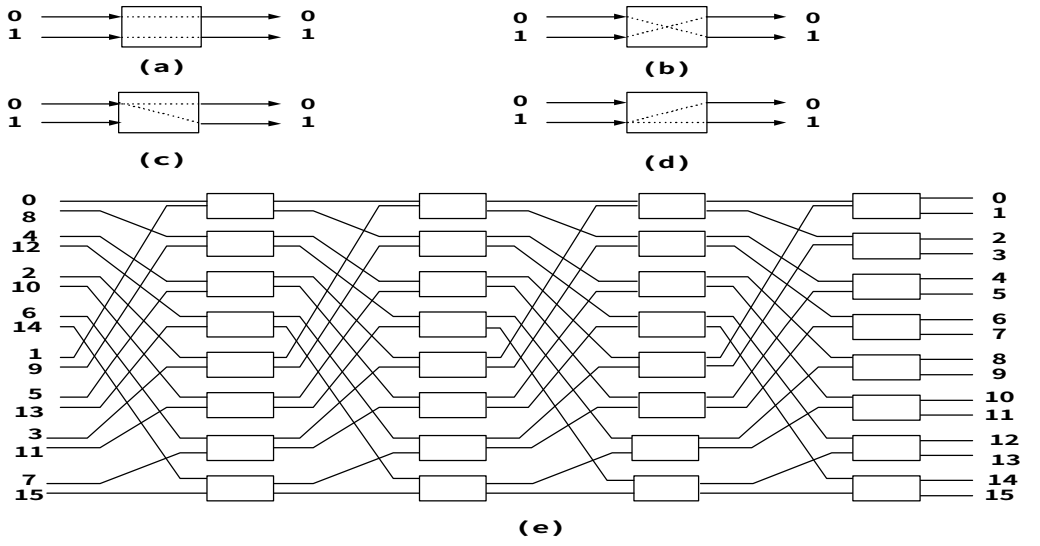


# Dynamic-Connection Networks (3)

## ☞ MIN (Multistage Interconnection Networks):

- ✍ **The number of delay = *O(log n)***
  **The number of building blocks = *O(n log n)***
- ✍ **Partial permutation between input and output.**



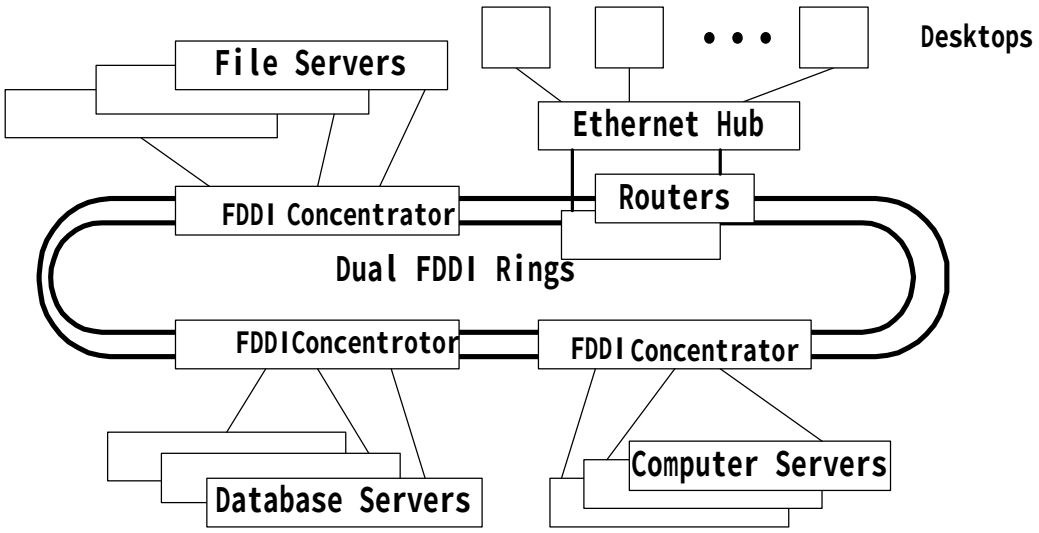
# Dynamic-Connection Networks (4)

- **Comparison of dynamic connection networks :**
  - **n: the number of connection taps**
  - **w: data path (channel) width**
  - **k: the number of input in a building block**
  - **f: clock rate**

| Interconnect Characteristics | System Bus | Multistage Network | Crossbar Switch |
|---|---|---|---|
| Hardware complexity | $O(n + w)$ | $O(nw \log_k n)$ | $O(n^2 w)$ |
| Per-processor bandwidth | $O(wf/n)$ to $O(wf)$ | $O(wf)$ | $O(wf)$ |
| Reported aggregate bandwidth | 2.67 GB/s for Gigaplane bus in SunFire server | 10.24 GB/s for 512-node HPS in IBM SP2 | 3.4 Gb/s for Digital's GIGAswitch |

## FDDI (Fiber Distributed Data Interface) Rings

- Two rings in opposite directions provide redundant paths for reliability purpose.
- FDDI provides 100-200 Mbps transmission.
- Distance : 100m over copper
  2km over multi mode fiber
  60km over single mode fiber
- Drawback : Inability to support multimedia traffic.
- Example of Dual FDDI rings as a backbone network :

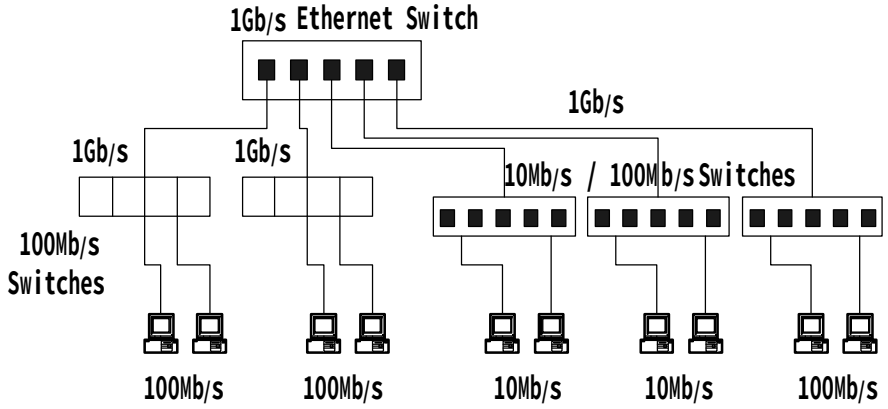


# Fast Ethernet and Gigabit Ethernet

## ☞ Three generations of Ethernet :

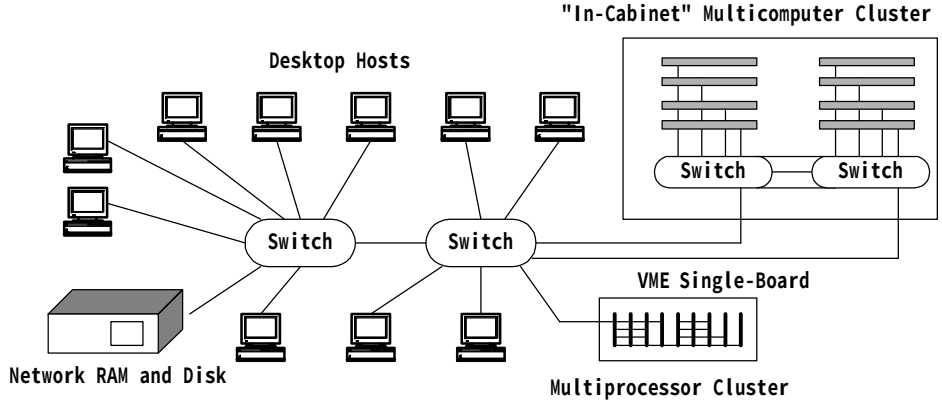
| Generation | Ethernet 10 BaseT | Fast Ethernet 100 BaseT | Gigabit Ethernet |
|---|---|---|---|
| Year of introduction | 1982 | 1994 | 1997 |
| Bandwidth (speed) | 10 Mbps | 100 Mbps | 1 Gbps |
| UTP twisted pair | 100 m | 100 m | 25-100 m |
| STP/coaxial cable | 500 m | 100 m | 25-100 m |
| Multimode fiber | 2 km | 412 m in half duplex, 2 km in full duplex | 500 m |
| Single-mode fiber | 25 km | 20 km | 2 km |
| Major applications | File sharing, printer sharing | Workgroup computing, client-server architecture, large database access | Large image files, multimedia, Intranet, Internet, data warehousing |

## ☞ The construction of a Gigabit Ethernet LAN backbone :



# Myrinet SAN & Myrinet LAN

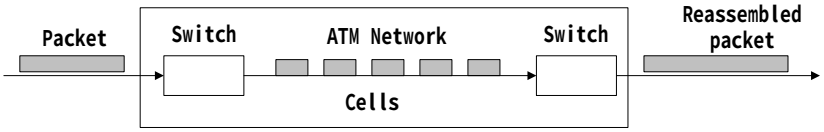
- **Goal: to connect a commodity product for building clusters of computers: either in-cabinet SAN clusters or LAN-based clusters of desktop hosts and server farms.**




- **Myrinet is defined at the data link level. The use of wormhole crossbar switches routes packets. Following a deadlock-free routing scheme, multiple packets can flow through a Myrinet simultaneously.**
- **Myricom is shipping Myrinet/SBUS for SUN workstations and Myrinet/PCI for PCs. Optic-fiber interface is also underway.**
- **Myrinet's bus-dependent host interface still pose a limitation to connect a large variety of hosts to Myrinet.**

# ATM (Asynchronous Transfer Mode)

- **ATM is a medium-independent information transmission protocol that segments traffic into short fixed-length 53-byte cells.**



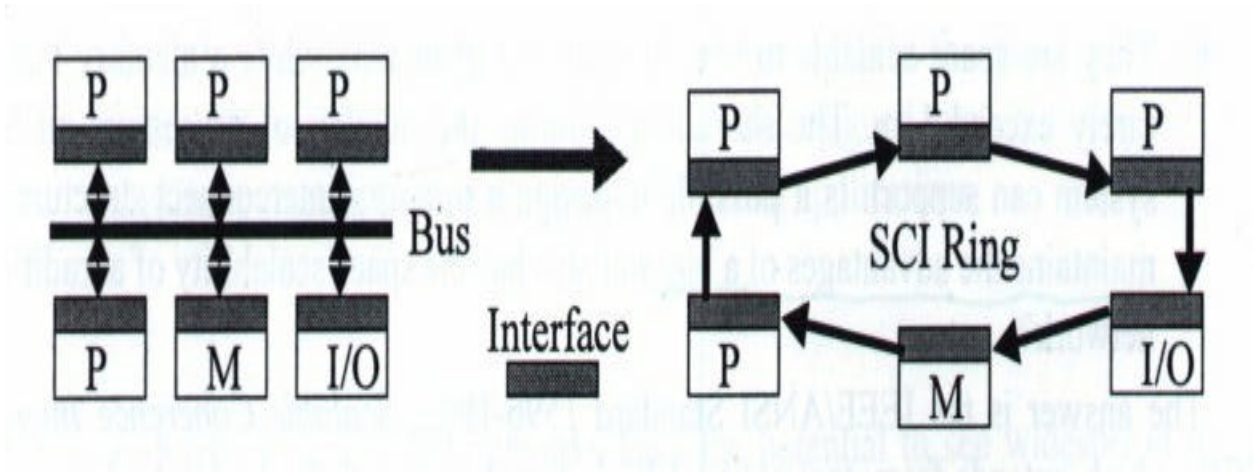

- **Shortcomings: ATM networks lack of a commonly accepted cell management and network protocols. Telephone and computer industry apply different standards at this time. Unless they agree to the same set of ATM standards, these shortcomings may outweigh the benefits of ATM technology.**
- **Four layers of ATM architecture :**

**Functionality of ATM Layers with Corresponding OSI Layers**

| OSI layer | ATM layer | ATM sublayer | Functionality |
|---|---|---|---|
| 3/4 | AAl (ATM adaptation Layer) | CS | Providing the standard interface (convergence) |
| | | SAR | Segmentation and reassembly |
| 2/3 | ATM | | Flow control, cell header generation/extration, virtual circuit/path management, cell multiplixing/ demultiplexing |
| 2 | Physical | TC | Cell rate decoupling, header checksum generation and verification, cell generation, packing/ unpacking cells from the enclosing envelope |
| 1 | | PMD | Bit timing, physical network access |

# SCI (Scalable Coherence Interface)

- **Motivation: We have discussed the above networks that they are all connected to I/O bus of a node, and communication with passing message among the computer nodes. This type of I/O communication in inferior to SM communication in a bus-based SMP.**
- **SCI extends from conventional backplane bus to a fully duplex, point-to-point interconnect structure with low-latency (<1μs) and high-bandwidth (8GB/s) providing a coherent cache image of DSM.**



# Comparison of Network Technologies

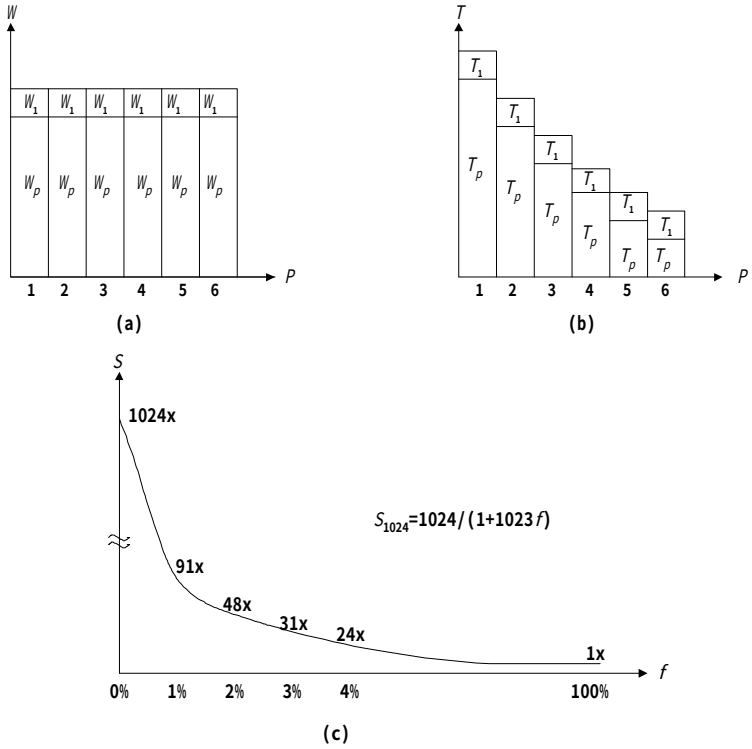
| Technology | Gigabit Ethernet | HiPPI | Fiber Channel | FDDI | SCI | ATM | Myrinet |
|---|---|---|---|---|---|---|---|
| Architecture | Shared media, switched | Switched | Shared media, switched | Shared media | Shared media | Switched | Switched |
| Media type | UTP, Coaxial, fiber | Fiber, 50-pair STP | STP, Coaxial, fiber | Fiber, copper | STP, fiber | UTP, STP, fiber | Electric links, fiber planned |
| Standard body | IEEE 802.3z, Gigabit Ethernet Alliance | ANSI X3.183, X3.210, X3.218, X3.222 | ANSI X3T11 | ANSI X3T9.5 | IEEE 1596-1992 | ATM Forum, IETF, ITU-TSS | Myricom |

UTP: unshielded twisted pair, STP: shielded twisted pair.

# Amdahl's Law: Fixed Problem Size

- In real-time applications, the computational workload $W=W_p+W_s$ is fixed, as the number of processors increases, the computational time decreases.
- Amdahl's Law: Let $f=W_s/W$, then

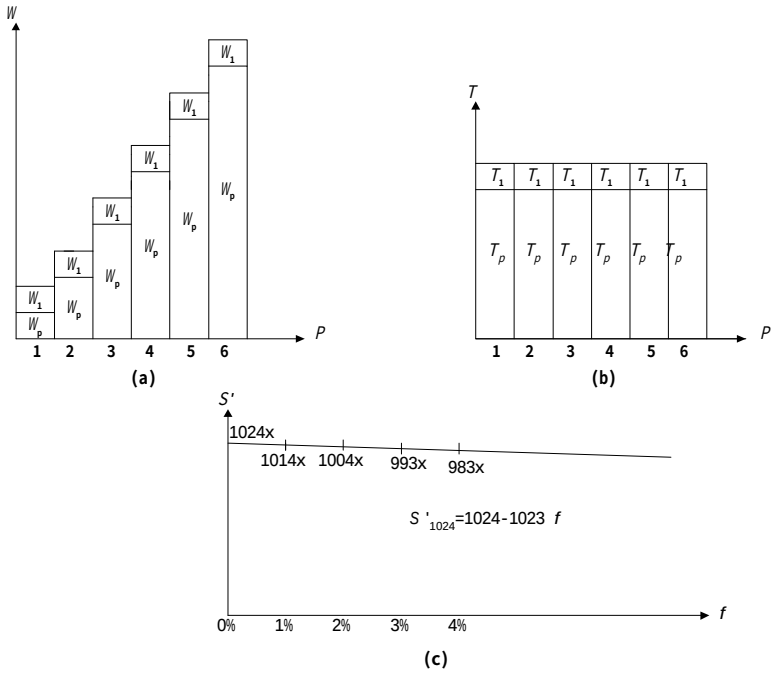
$$S=W/(W_p/p+W_s)$$
$$=f+(1-f)/(f+(1-f)/f)$$
$$=p/(1+f(p-1))$$
$$=1/f \quad (p\text{fi}¥ )$$



# Gustafson's Law: Fixed Time

- In large scientific computation applications, in order to increase accuracy, we have to increase workload. Correspondingly, we have to increase the number of processors to keep the execution time unchanged.
- Gustafson's Law:

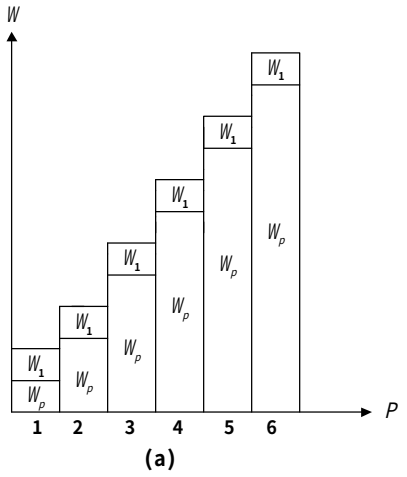
$$S=(W_s+pW_p)/(W_s+pW_p/p)$$
$$=(W_p+pW_p)/(W_s+W_p)$$
$$=f+p(1-f)$$
$$=p+f(1-p)$$
$$=p-f(p-1)$$

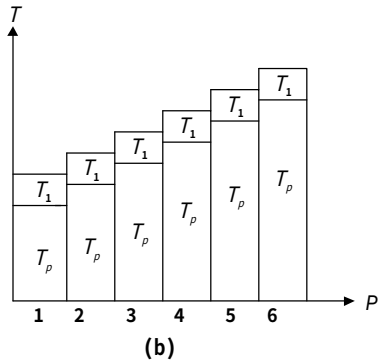


## Sun and Ni's Law: Memory Bounding

- **This law generalizes Amdahl's and Gustafson's law to maximize the use of CPU and memory capacities. The idea is to solve the largest possible problem limited by memory space. This also demands a scaled workload, providing higher speedup, greater accuracy and better resource utilization.**
- **Assume that the parallel portion of the workload can be scaled up *G(p)* times. The factor *G(p)* reflects the increase in workload as the memory capacity increase *p* times.**
- **Sun and Ni's law :**

$$S=(W_s+G(p)W_p)/(W_s+G(p)W_p/p)$$
$$=(f+G(p)(1-f))/(f+G(p)(1-f)/p)$$



# Scalability

- **Definition : A computer system (hardware, software, algorithms etc.) is called scalable, if it can scale up (increase its resources) to accommodate performance and functionality demand and/or scale down (decrease its resources) to reduce cost.**
- **Dimensions of scalability :**
  - **Scalability in Machine Size: This indicates how well the performance will improve with additional processors. This scalability measures the maximum number of processors a system can accommodate.**
  - **Scalability in Problem Size: This indicates how well the system can handle larger problems with larger data size and workload.**
  - **Technology Scalability: This indicates how well the performance improvement with the changed technology.**
- **How to measure the scalability :**
  - **Iso-efficiency**
  - **Iso-speed**
  - **Average latency**
  - **Time-Scale**

# Iso-Efficiency

## ☞ Basic concept :

**Iso-efficiency indicates how well a parallel system scales while maintaining a fixed efficiency.**

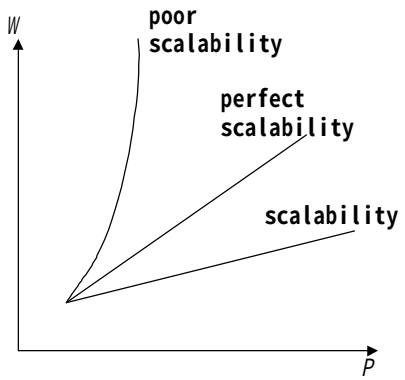
**Let $T_1$ be the sequential time on one processor (i.e. workload $W$), $T_p$ be the parallel time, $T_o$ be the total overhead, then $T_1+T_o=pT_p$, $S= T_1 / T_p=p/(1+ T_o / T_1)$, $E=S/p=1/(1+ T_o / T_1)$. If we fix E, and solve the efficiency equation for workload W, the resulting function is called the iso-efficiency function of the system, i.e. $W=f_E(p)$.**

## ☞ Advantages :

**The iso-efficiency function is the analytical method which provides a useful tool to predict the required workload growth rate with respect to the machine size.**

## ☞ Disadvantages :

**For shared-memory architecture machine, to compute the iso-efficiency function is not too easy.**



# Iso-speed

## Basic concept :

The basic concept is similar to iso-efficiency. Instead of maintaining a constant efficiency, one can preserve a constant average speed while scaling up both machine size from p to p' and problem size from $W$ to $W'$ at the same time.

Let the average speed $V=W/pT_p$ , while from p to p' and from $W$ to $W'$, in order to maintain average speed unchanged, then define $\psi(p,p')=p'W/pW'=T_p/T_{p'}$,

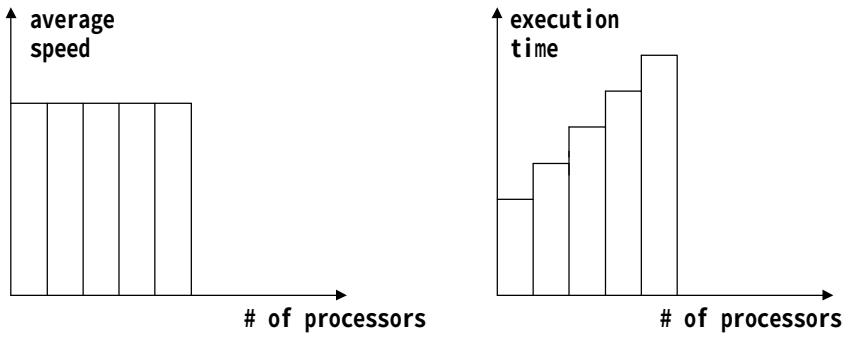
If p=1, then $\psi(1,p')=T_1/T_{p'}$.

## Advantages :

Speed is the real and normal physical quantity which is generally measured as float-point operations performed.

## Disadvantages :

Some non-floating point operations can cause major performance changes.



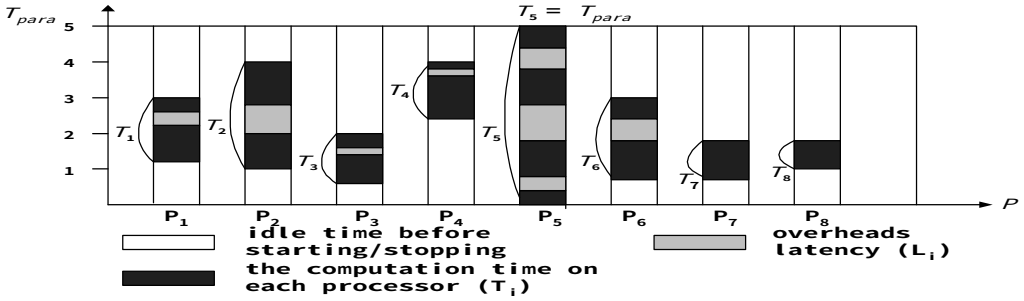
# Average Latency

## ☞ Basic Concept :

**Referring to the following figure, average latency *L(W,p)* is defined as an average amount of overhead time needed for each processor to complete the assigned work:**

$L(W,p) = \sum_{i=1}^{p}(T_{para}-T_i+L_i)/p$

**If the machine size changes from p to p', and the efficiency is kept to a constant, the average latency metric is defined as $F(E,p,p') = L_e(W,p)/L_e(W',p')$.**




## ☞ Advantages :

**Average latency is the experimental metric which can more precisely evaluate performance at lower level system.**

## ☞ Disadvantages :

**It needs specialized hardware and system software to measure the latency of the processors.**

## ☞ Conclusion :

**Iso-efficiency metric is equivalent to iso-speed metric, average latency metric can be derived from iso-speed metric.**