



# RISC-V based MYTH

MYTH- *Microprocessor for You in Thirty Hours*

## Workshop Certificate

{9<sup>th</sup> - 13<sup>th</sup> June 2021}

*Ninad*

*has successfully completed  
an online cloud based workshop conducted on VSD-IAT*

<b>Skills learned</b> <ul style="list-style-type: none"><li>• RISC-V ISA Overview</li><li>• RISC-V GNU Tool-chain</li><li>• Spike debugging</li><li>• Digital Logic</li><li>• Pipelined CPU Design</li><li>• TL-Verilog</li><li>• Markerchip IDE</li></ul>	17/17
<b>Lab Skills Activities</b>	87/87
<b>% of RISC-V Core Designed</b>	100%
<b>GitHub Repo Link</b>	<a href="https://github.com/RISCV-MYTH-WORKSHOP/riscv_myth_workshop_jun21-RISC-V%20based%20MYTH">https://github.com/RISCV-MYTH-WORKSHOP/riscv_myth_workshop_jun21-RISC-V based MYTH</a>

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(Design & Sign-off Expertise, Founder VLSI System Design)