Hardware Cards

PCI-6602

Pixel Clock
- ND_COUNTER_7
- Output ND_PFI_8 (pin 16)

Line Clock
- ND_COUNTER_6
- Output ND_PFI_12 (pin 53)

Frame Clock
- ND_COUNTER_5
- Output ND_PFI_16 (pin 23)

Photon Counter A
- ND_COUNTER_1
- Source ND_PFI_35 (pin 7)
- Gate ND_PFI_34 (pin 8)

Photon Counter B
- ND_COUNTER_4
- Source ND_PFI_23 (pin 28)
- Gate ND_PFI_22 (pin 27)

Photon Counter C
- ND_COUNTER_0
- Source ND_PFI_39 (pin 2)
- Gate ND_PFI_38 (pin 3)

Hardware Trigger
- ND_PFI_1 connected to ND_PFI_7 (pin 44 to pin 15)
- ND_PFI_1 is software controlled prompting the hardware triggering of counters via ND_PFI_7. Detection occurs on a falling edge as set with ND_HIGH_TO_LOW.

Stepper Motor/Flipper Control
- Motor Enabled State: Output ND_PFI_2 (brown pin 45)
- Motor Half Step State: Output ND_PFI_3 (yellow pin 12)
- Motor Direction: Output ND_PFI_4 (grey pin 13)
  NOTE: above three settings should be followed by a small sleep before calling any further function calls.
- Toggle Shutter State: Output ND_PFI_5 (orange pin 47)
  Three functions calls in a row required: High, Low, and High again.
- Get Shutter State: Input ND_PFI_6 (green pin 48)

Miscellaneous
- Casing earth: pin 55 & pin 30
- +5V supply for triple AND gate circuit: pin 1
- Earth for circuitry: pin 11
  Also connected to pin 53 on PCI-6120

Remaining

- Counters ND_COUNTER_3 & ND_COUNTER_4
  Both have very poor output of fast pulses. Unsure of efficiency counting pulses and recognizing fast gate signals.
- ND_PFI_0 DIO unused.

PCI-6120

Analog Outputs

- X Output: pin 22
- X Earth: pin 55
- Y Output: pin 21
- Y Earth: pin 54

Hardware Trigger

- ND_PFI_6 (pin 5). Falling edge on this DIO triggers the occurrence of the next pair of analog outputs.

Stepper Motor/Flipper Control

- Serial earth (red pin 9)
- CTR0OUT – ND_COUNTER_0 (blue pin 3)

Miscellaneous

- Casing earth: pin 50 & pin 7
- +5V for AND gate buffers circuit: pin 14
- Circuitry earth: pin 53

Remaining

- Four 16bit analog inputs
- One counter: CTR 1
- Nine PFI DIO lines. Although, after albeit minimal determination, I was unable to control output states of the digital lines. More testing required.

PCI-6040E

Analog Inputs – via BNC-2120

- Analog In 0: X Difference ACH0
- Analog In 1: Y Difference ACH1
- Analog In 2: Total ACH2

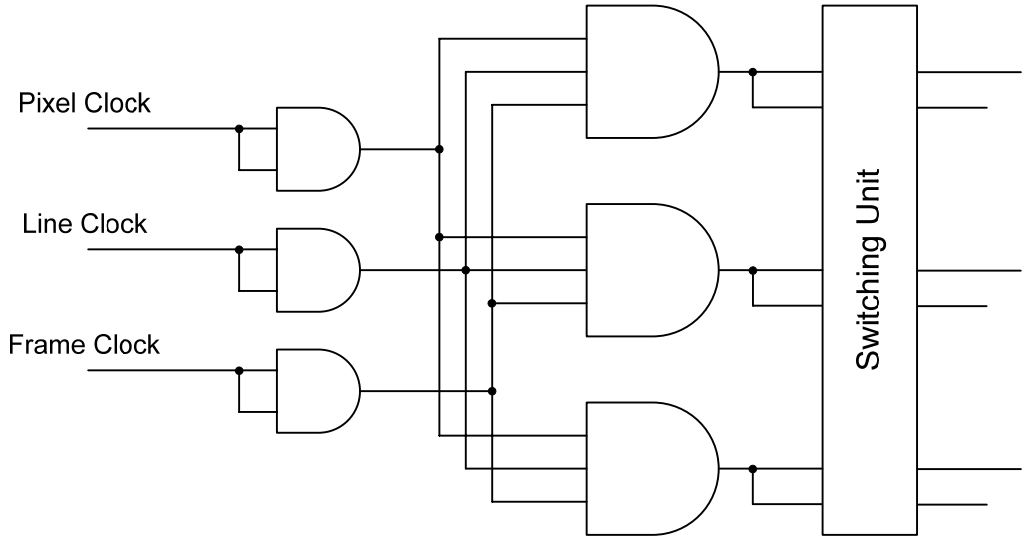
} **Diode A**

- Analog In 3: X Difference ACH3
- Analog In 4: Y Difference ACH4
- Analog In 5: Total ACH5

} **Diode B**

Hardware ‘ANDing’ Circuitry

The outputs from the pixel, line and frame clocks are each buffered by an AND gate and then ‘ANDed’ with each other three times by three different high speed triple AND gates. This allows for more usable gates signals at the high speeds required.



The switching unit allows for switching of gate and source connections to the photon counters on the PCI-6602. In the buffered pulse width measurement mode the gate created with the above circuitry dictates the duration over which the source pulses (TTL pulses from photon detecting hardware) are counted, requiring the switches to be in the UP position (see below). To measure the time between the TTL pulses from the detectors in period measurement mode requires the input source from the detectors to be connected to the gate signal of the relevant counter and the source signal to be software set to use the internal timebase. This mode is used with the switches in the DOWN position.