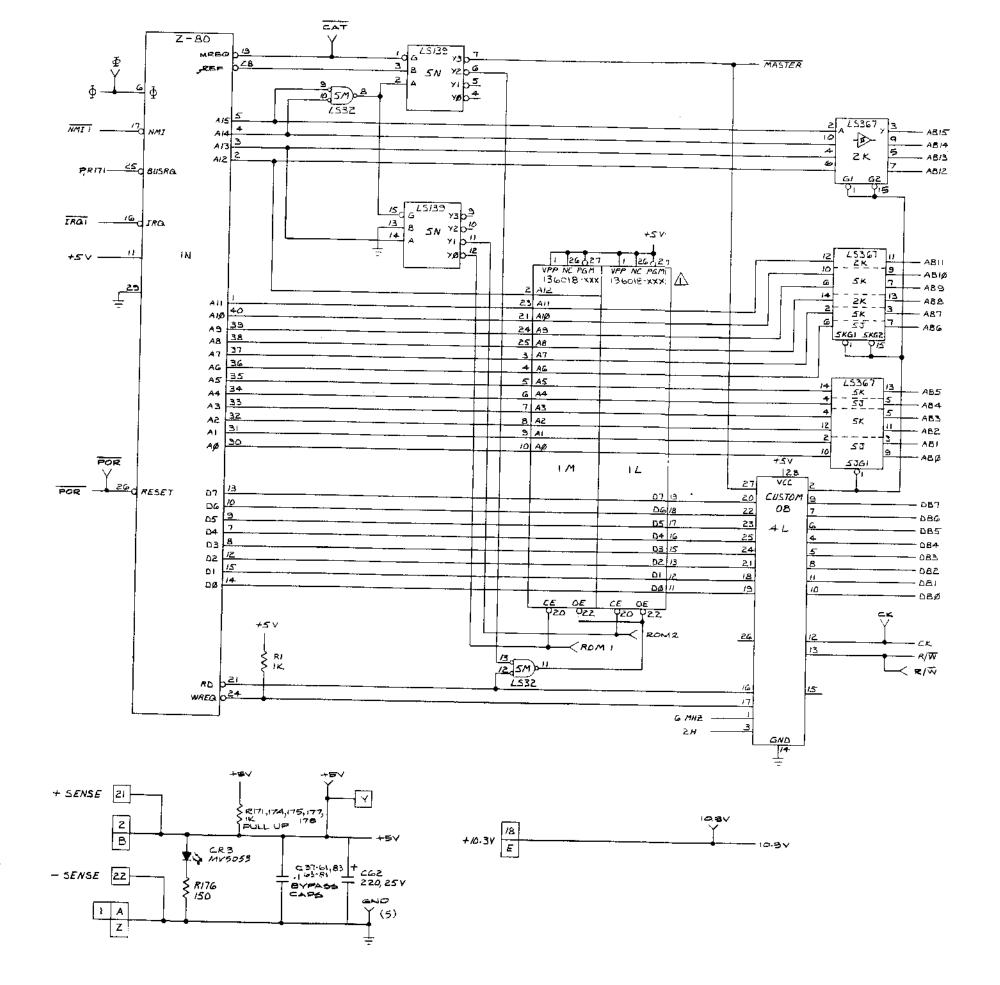
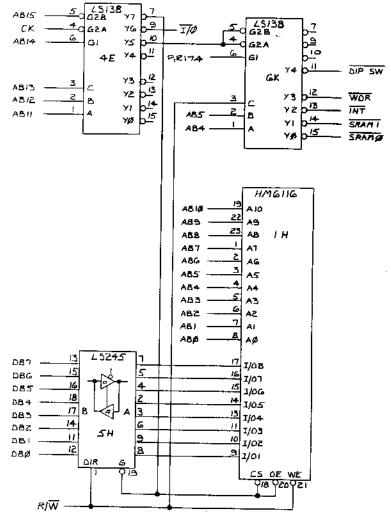
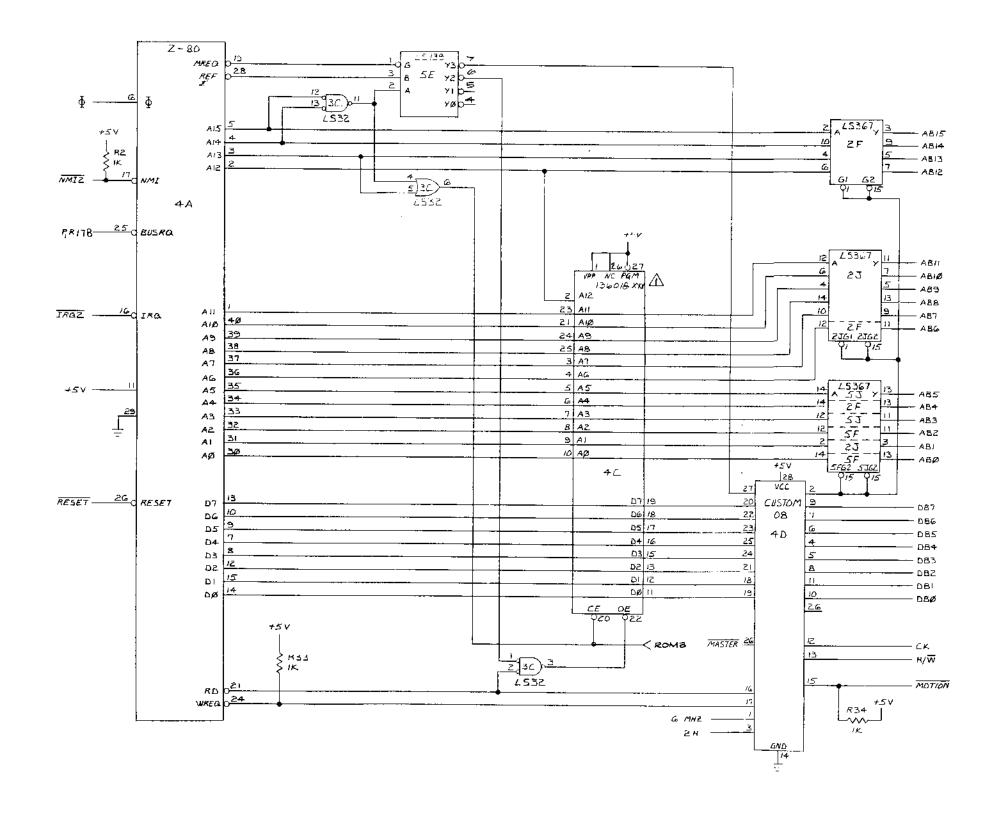
# **MEMORY MAP**

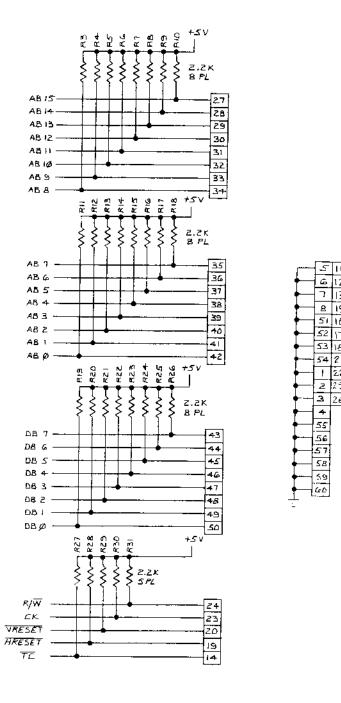
HEXA- DECIMAL ADDRESS	ADDRESS BUS SIGNAL LINES														R/W	DATA BUS SIGNAL LINES								FUNCTION		
	A15	A14	A13	A12	A11	A10	A9	A8	<b>A7</b>	A6	<b>A</b> 5	A4	А3	<b>A</b> 2	<b>A</b> 1	A0		D7	D6	D5	Đ4	D3	D2	D1	D0	
	CPU PCB																									
0000-1FFF 0000-2FFF 0000-1FFF 0000-1FFF	0 0 0	0 0 0	0 1 0 0	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	A A A	R R R	0000	0 0 0	D D D	D D D	D D D	D D D	D D D	D D D	MASTER PROGRAM MASTER PROGRAM MOTION PROGRAM SOUND PROGRAM
6800 6810 6820 6821 6822 6823 6824-6827 6830 6840 7000 7100 7800	000000000000000000000000000000000000000	1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1	0 0 0 0 0 0 0 0 1 1	1 1 1 1 1 1 1 0 0	A	A	A	A	0 0 0 0 0 0 A	0 0 1 1 1 1 1 A	0 1 0 0 0 0 0 1 A	A	0 0 0 0 0 0 0 A A	0 0 0 1 1 A A	0 0 0 1 0 1 A A		D D	D D	D D	D D	D D	D D	D D	D D	SOUND RAM 0 SOUND RAM 1 CLEAR CLEAR NMION RESET NOT USED WDR DIP SW I/O DECODE I/O CONTROL RAM
VIDEO PCB																										
8000-8FFF 9000-9FFF A000-AFFF B000-BFFF C000-CFFF D000 F000 F0001	1 1 1 1 1 1	0 0 0 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 1		A A A	A A A A	A A A A	A A A	A A A A	A A A A	A A A A	A A A A	A A A A	A A A A	A A A A O 1	R/W R/W R/W R/W R/W R R/W R/W	D D D D	D D D D	0000	0000	D D D D	0000	0000	D D D D	RAM 2S RAM 2R RAM 2P RAM 1 RAM 2 PAL BB0 (Read) BSO (Write) BB1 (Read) BS1 (Write)



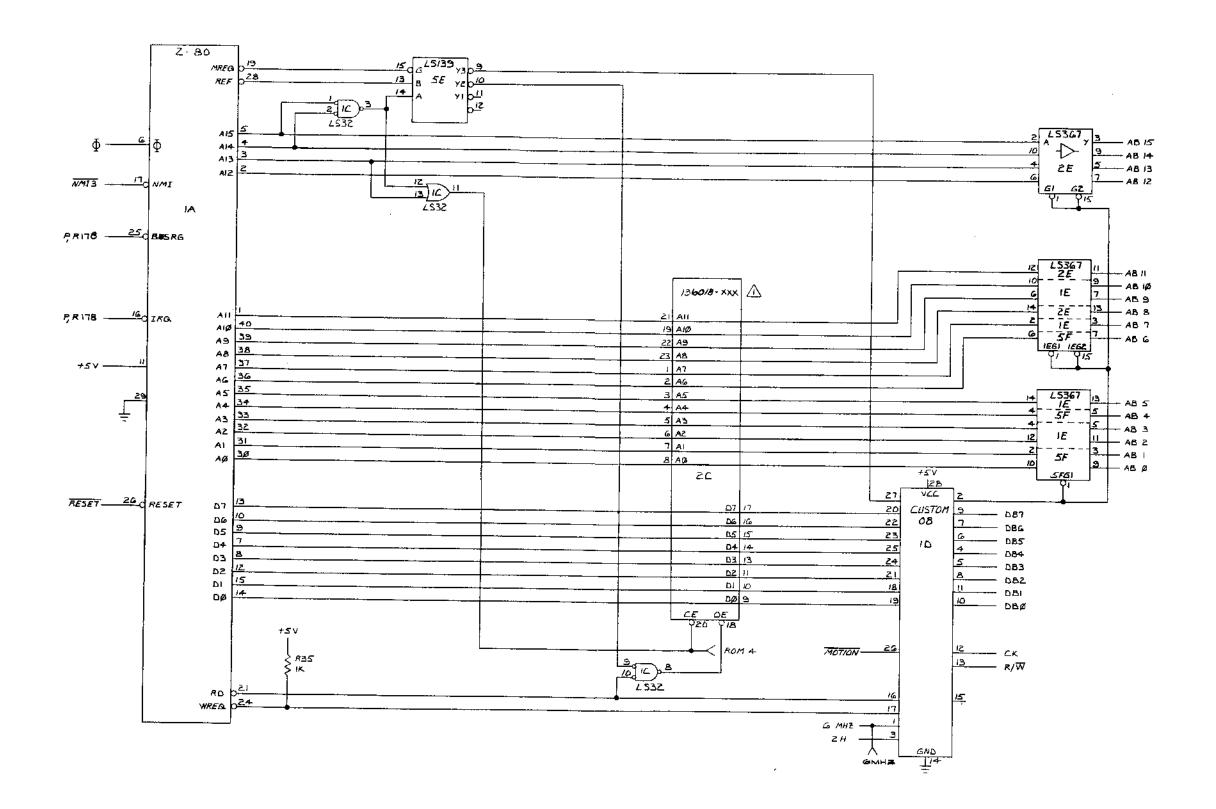


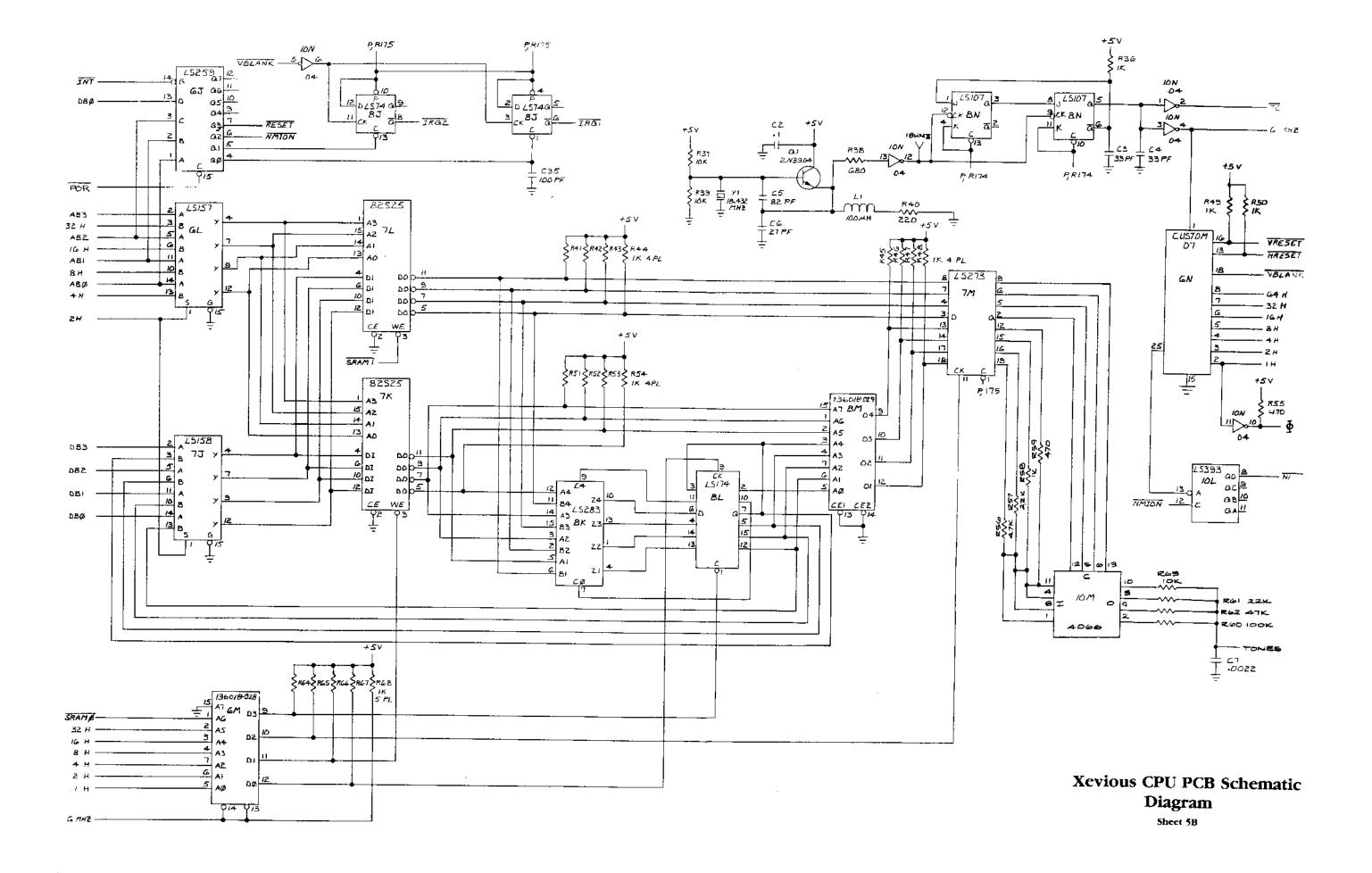
Sheet 4A

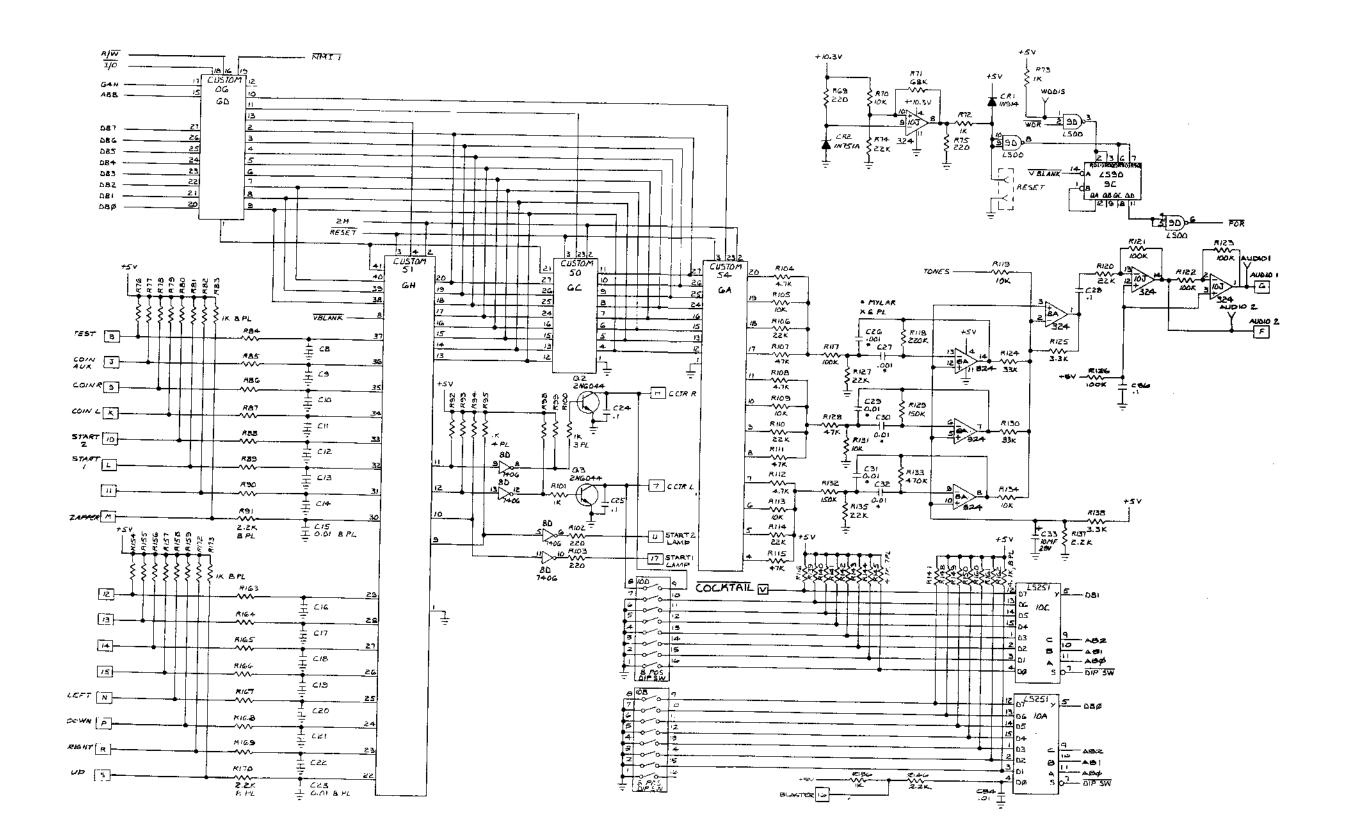




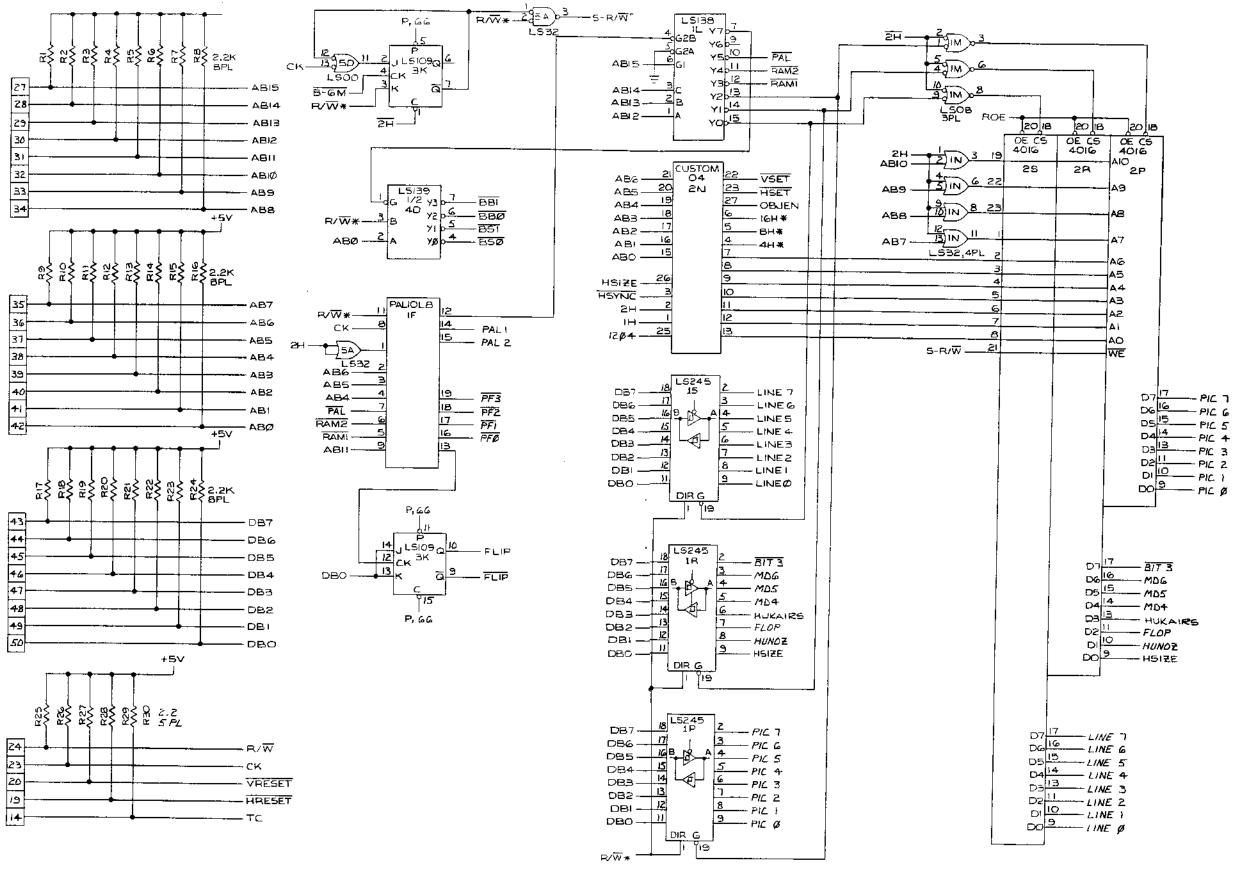
Sheet 4B





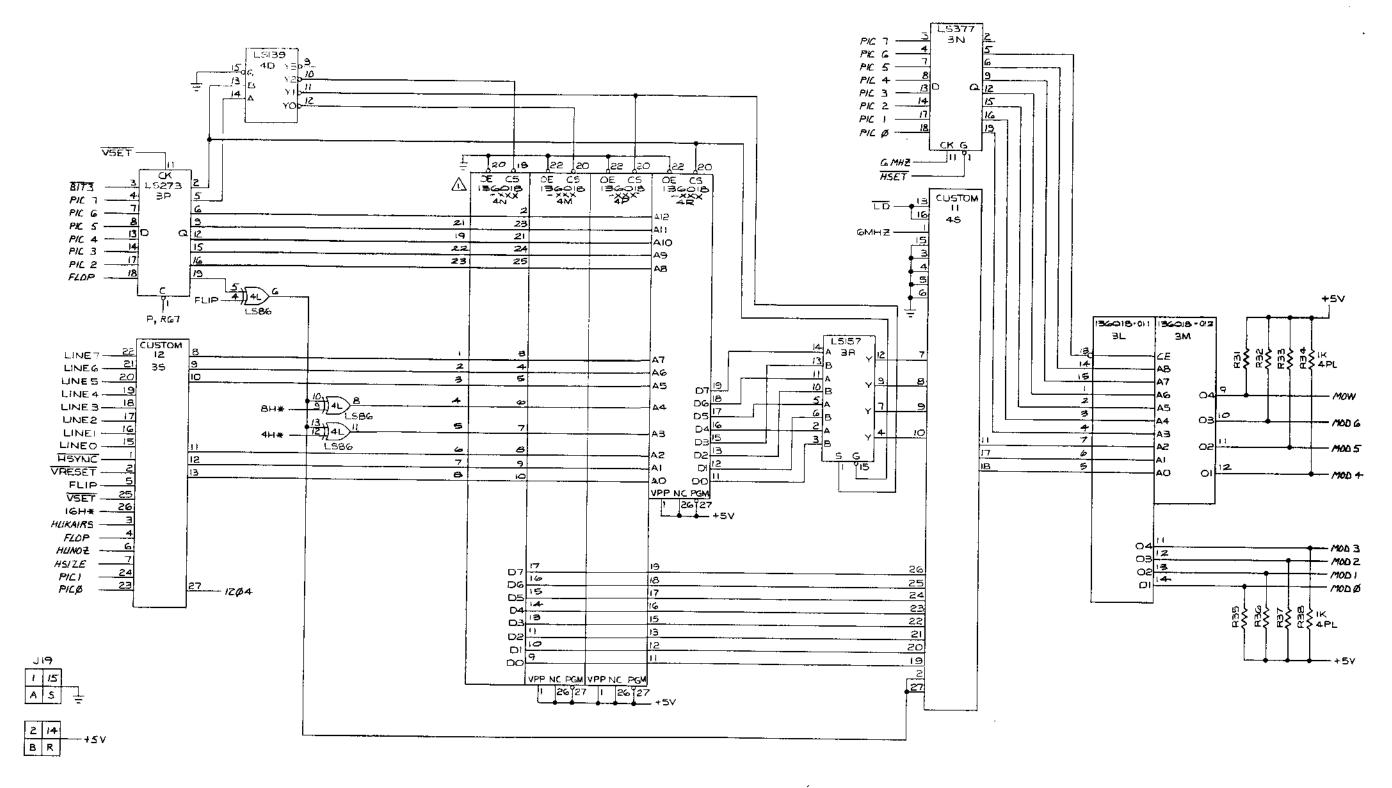


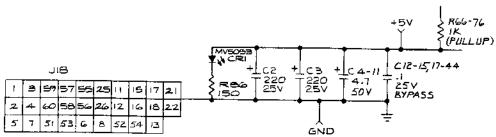
Sheet 6A



Xevious Video PCB Schematic Diagram

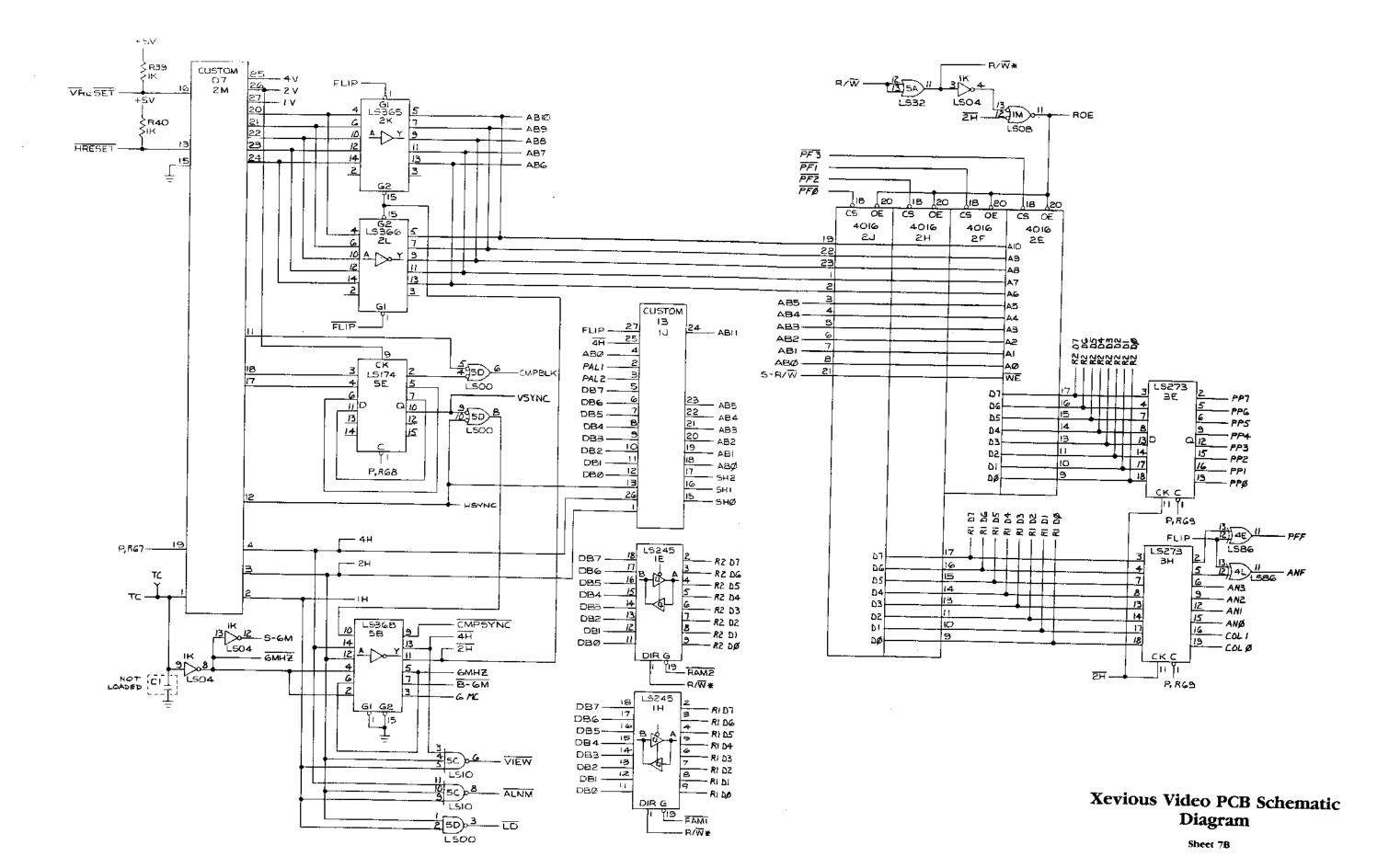
Sheet 6B

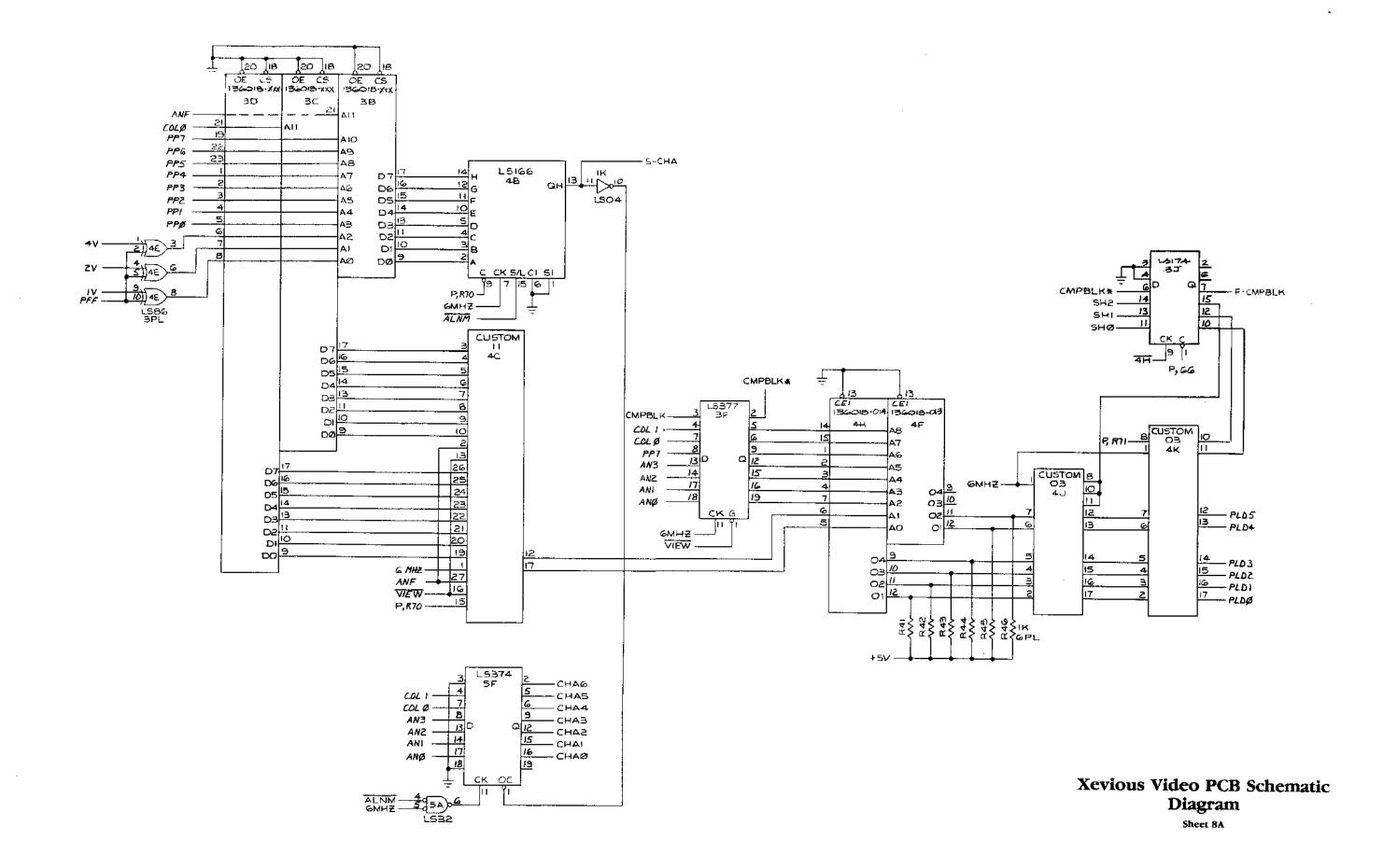


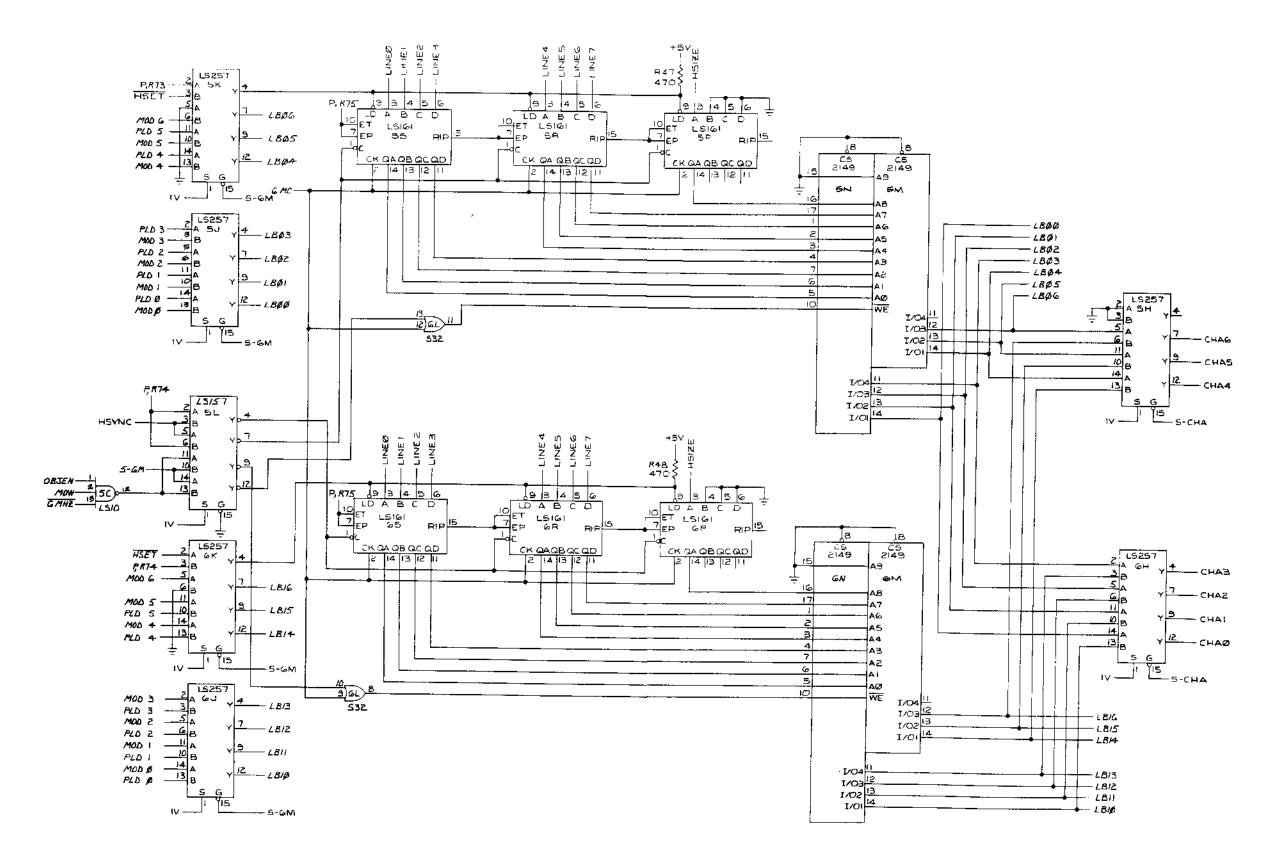


Xevious Video PCB Schematic Diagram

Sheet 7A

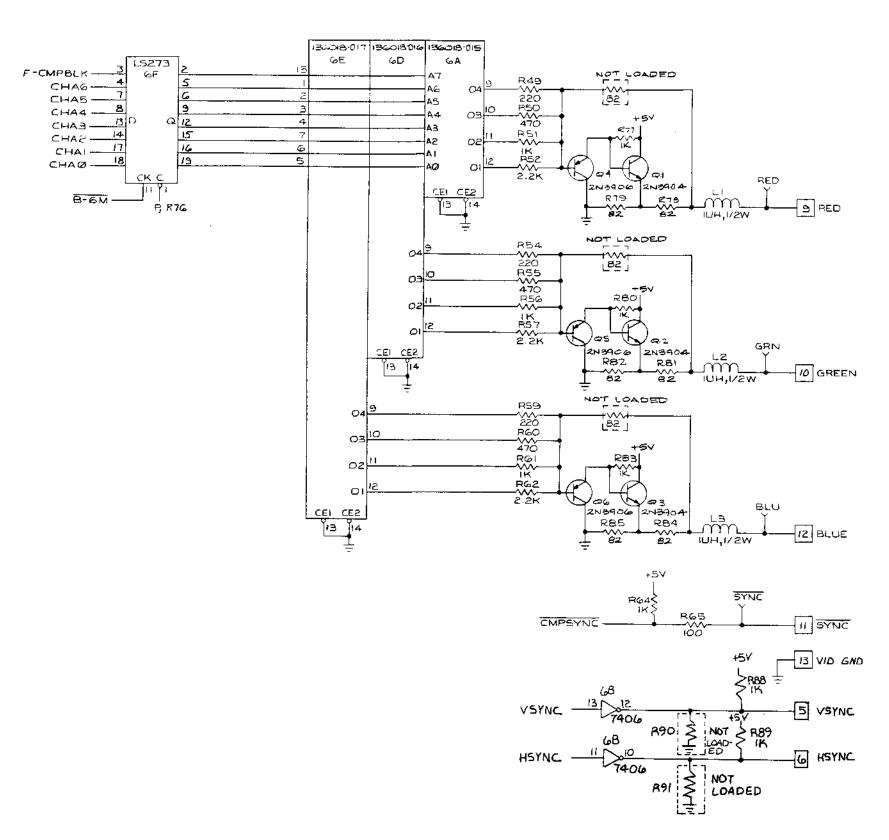






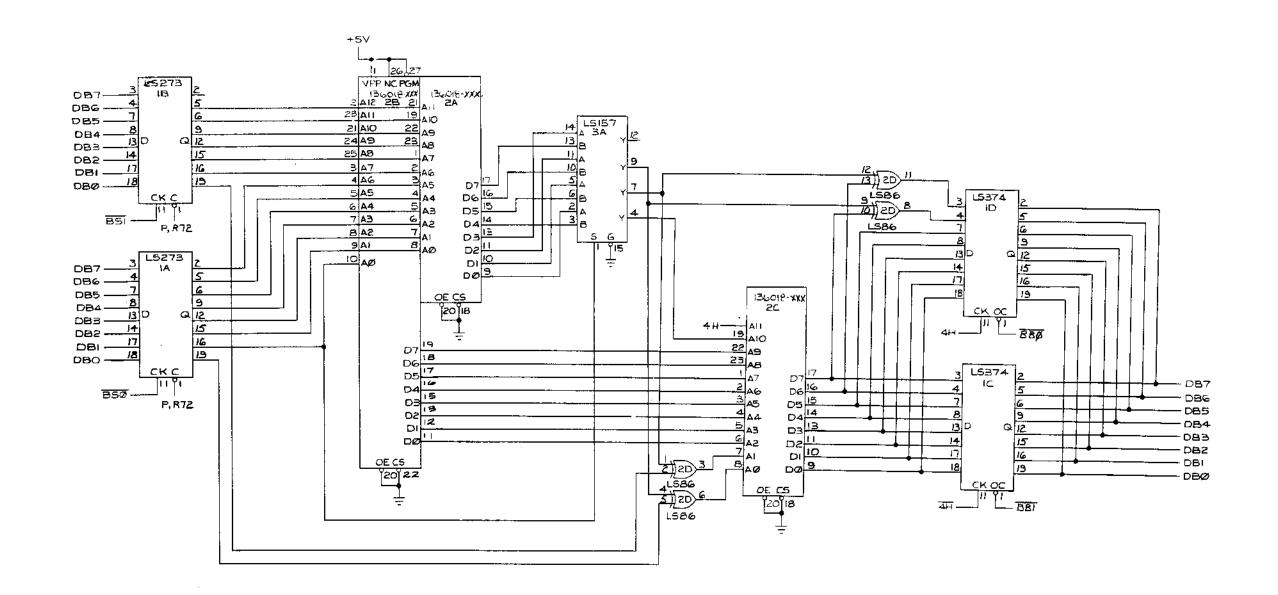
Xevious Video PCB Schematic Diagram

Sheet 8B



Xevious Video PCB Schematic Diagram

Sheet 9A



# Xevious Video PCB Schematic Diagram