Application Note
Frontends, Sub-Device Specifications, and Antenna Port Selection
Ettus Research

## Introduction

This document explains the concept of daughterboards, frontends, sub-device specifications, and antenna selection. Frontends are sub-components of daughterboards that dictate the tuning algorithms and sample mapping used by the USRP™ (Universal Software Radio Peripheral). The USRP Hardware Driver (UHD) accepts sub-device specifications, which are strings used to configure the USRP device to utilize a frontend in the desired manner. Each frontend provides access to one or more RF connectors. You must select the appropriate connector based on operational requirements, such as the need for full or half-duplex operation.

## Daughterboards, Frontends, and Sub-Device Specifications

When developing an RF system with a USRP device, it is important to understand how to select the correct frontend. One or more daughterboards can be integrated into a USRP device. The Ettus Research daughterboards provide the circuitry required for an interface between the ADCs, DACs, and the "outside world." Each of these daughterboards includes one or more channel called a frontend.

In the context of UHD, a frontend can be selected by using a sub-device specification when creating an instance of a USRP device. This is accomplished with frontend routing logic inside the FPGA that multiplexes the data according to the sub-device specification. An illustration of this architecture in the receive chain is shown in Figure 1. Several examples of the routing are shown throughout the document.

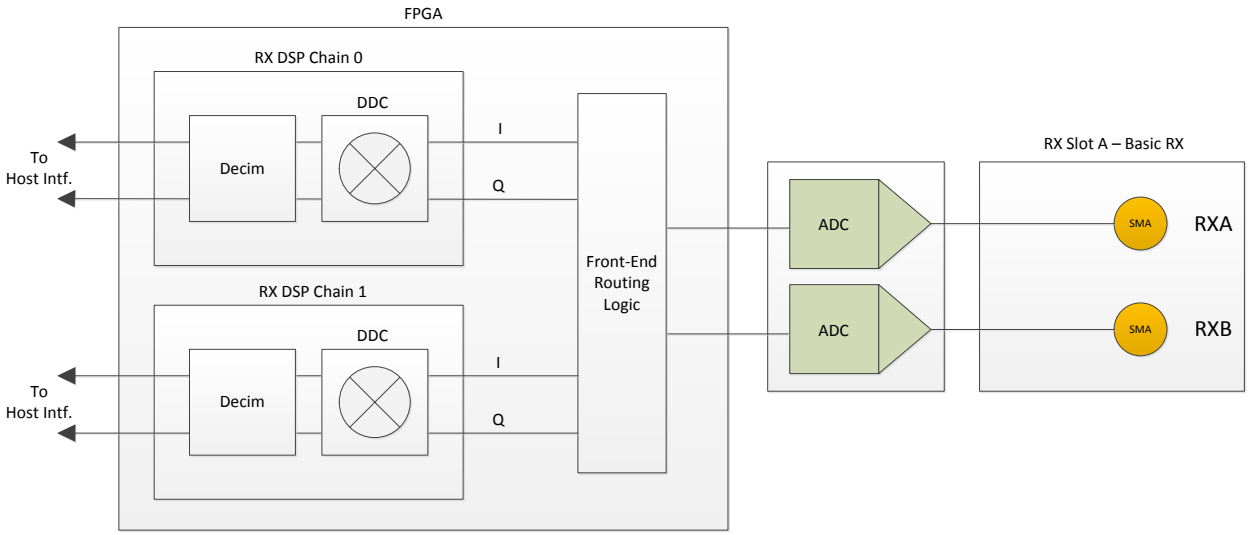


Figure 1 - Frontend Interface Architecture - Basic RX Shown as Example

The sub-device specification follows the format "X:Y". X always refers to the daughterboard slot. In the case of the USRP N200/N210, USRP E100/E110, and USRP B100, there is only one daughterboard slot

(for each direction). This is referred to as daughterboard "Slot A." The USRP1 includes two daughterboard slots, "A" and "B." The second part of the sub-device specification,"Y," selects a single frontend from daughterboard specified by the slot designator. UHD configures the FPGA's frontend router to pass the appropriate signals to a DSP chain.

For example, if you want to receive the signal from Channel 1 of a TVRX2 in Slot B, the sub-device specification is: "B:RX1." Accessing a signal from Channel 2 of a TVRX2 in Slot A would require: "A:RX2." The frontends of each daughterboard are summarized along with TX/RX directions, valid antenna selections, and associated RF connectors in Table 1.

| Daughterboard | Direction | Front-End | Valid Antenna Selections | Associated RF Connector |
|---|---|---|---|---|
| BasicRX | RX | A | n/a | RXA |
| | | B | n/a | RXB |
| | | AB | n/a | RXA & RXB(Quad Intf) |
| | | BA | n/a | RXB & RXA(Quad Intf) |
| BasicTX | TX | A | n/a | RXA |
| | | B | n/a | RXB |
| | | AB | n/a | RXA & RXB(Quad Intf) |
| | | BA | n/a | RXB & RXA(Quad Intf) |
| LFRX | RX | A | n/a | RXA |
| | | B | n/a | RXB |
| | | AB | n/a | RXA & RXB(Quad Intf) |
| | | BA | n/a | RXB & RXA(Quad Intf) |
| LFTX | TX | A | n/a | RXA |
| | | B | n/a | RXB |
| | | AB | n/a | RXA & RXB(Quad Intf) |
| | | BA | n/a | RXB & RXA(Quad Intf) |
| TVRX2 | RX | RX1 | n/a | RX1 |
| | | RX2 | n/a | RX2 |
| DBSRX2 | RX | 0 | n/a | J3 |
| RFX Series | TX | 0 | TX/RX | TX/RX |
| | RX | 0 | RX2 | RX2 |
| | | | TX/RX | TX/RX |
| WBX | TX | 0 | TX/RX | TX/RX |
| | RX | 0 | RX2 | RX2 |
| | | | TX/RX | TX/RX |
| SBX | TX | 0 | TX/RX | TX/RX |
| | RX | 0 | RX2 | RX2 |
| | | | TX/RX | TX/RX |
| XCVR2450 | TX | 0 | J1 | J1 |
| | | | J2 | J2 |
| | RX | 0 | J1 | J1 |
| | | | J2 | J2 |

Table 1 - Daughterboards, Sub-Devices, and Connectors

**Default Sub-Device and Antenna Specifications**

UHD will automatically select a sub-device and antenna specification if they are not specified by you. It is possible these defaults will change, so they are not captured in this document. Typically, UHD maps the Basic and LR daughterboard to use both RF connectors as a quadrature interface, rather than a dual IF interface. Transceiver daughterboards are typically mapped as quadrature as well.

It is good practice to specify the antenna port for full-duplex transceiver boards, even though UHD will assume "TX/RX" if no port is specified. Depending on external configurations and signal levels, it is possible to damage daughterboards if the user relies on automatic antenna selection within UHD.

**Quadrature Sampling vs. IF Sampling**

The ADC and DSP chain within the FPGA will be configured to operate with an IF or quadrature signal, depending on the daughterboard and sub-device specification. The CORDIC is a mathematical architecture used to perform phase shifting on each sample, which effectively produces frequency translation. The CORDIC accepts a complex baseband signal as input, and outputs a complex baseband sample with the specified phase shift. Sample rate conversions occur on the "host" side of the CORDIC, and the CORDIC operates at the full sample rate of the ADC/DAC interface.

When an IF signal is sampled, the unused ADC or DAC channel is filled with null-samples. When a quadrature signal is sampled, both the I and Q signals are routed to the CORDIC. In some cases, the routing logic will swap the I and Q signals to match the orientation of the selected daughterboard.

**Discussion on Basic RX, Basic TX, LFRX, and LFTX Frontends**

The Basic RX, Basic TX, LFRX, and LFTX frontends are different from the other daughterboards, because they do not require antenna specifications. Instead, the sub-device specification is used to establish the routing of ADC/DAC samples to the DSP chain within the FPGA. When the frontend "A" is used, "A" is sampled in real mode as an intermediate frequency (IF). Likewise for frontend "B." Specifying "AB" as a front-end routes both signals to the FPGA's DSP chain as a quadrature pair. "BA" swaps the signals.

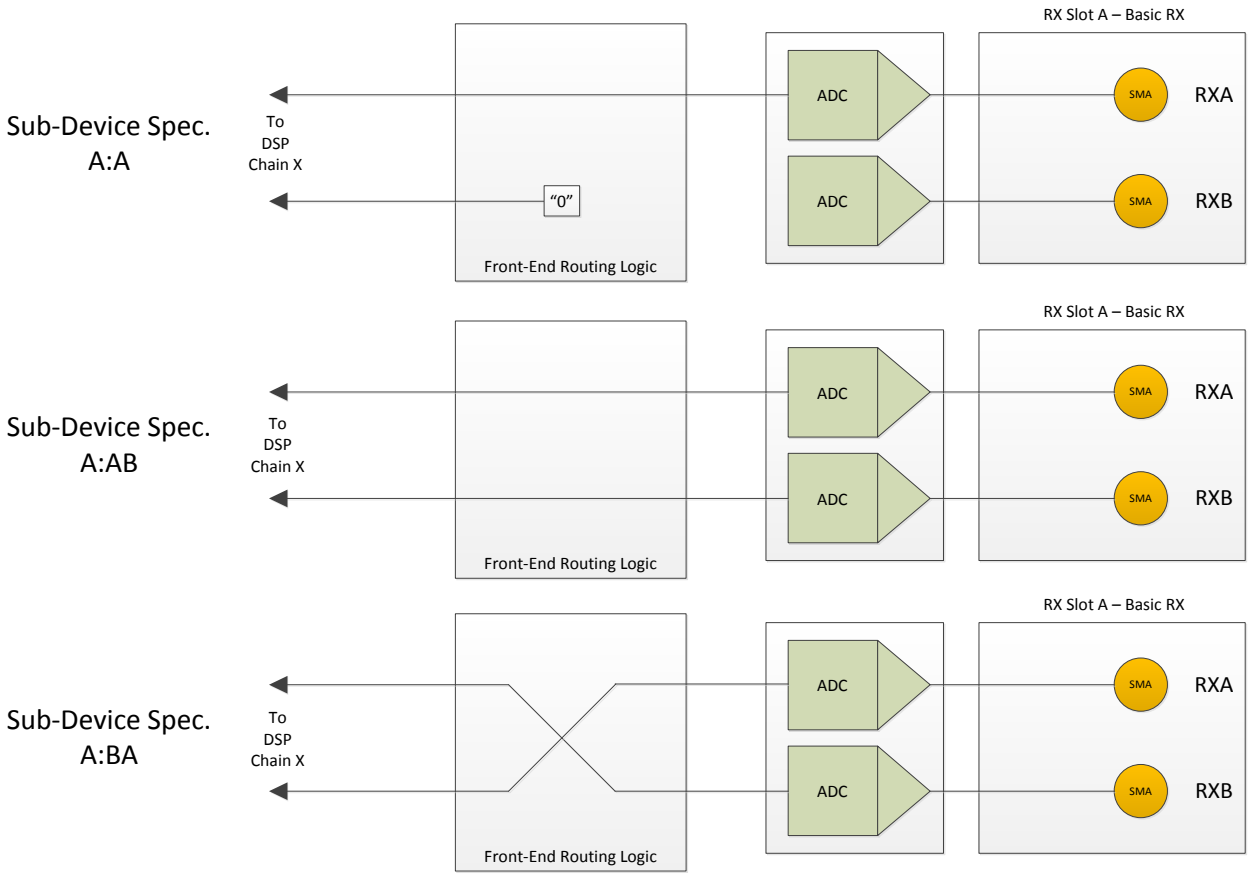


Figure 2 - BasicRX Routing w/ Various Sub-Device Specifications

This concept is illustrated with a receive chain shown with various sub-device specifications in Figure 2. The architecture is applicable to transmit daughterboards as well. The sample flows from the DSP chain to the frontend block when transmitting. While not illustrated here, it is possible to create two baseband channels to process two independent IFs. This will be discussed in another section of this document.

**Discussion on TVRX2**

The TVRX2 includes two, independent receive chains and outputs two IF signals. The USRP device can sample one of these signals or both. In this case, each IF signal is paired with a 0-filled stream to create an I/Q pair and passed along to an RX DSP Chain. In this case, two separate RX DSP chains are used.

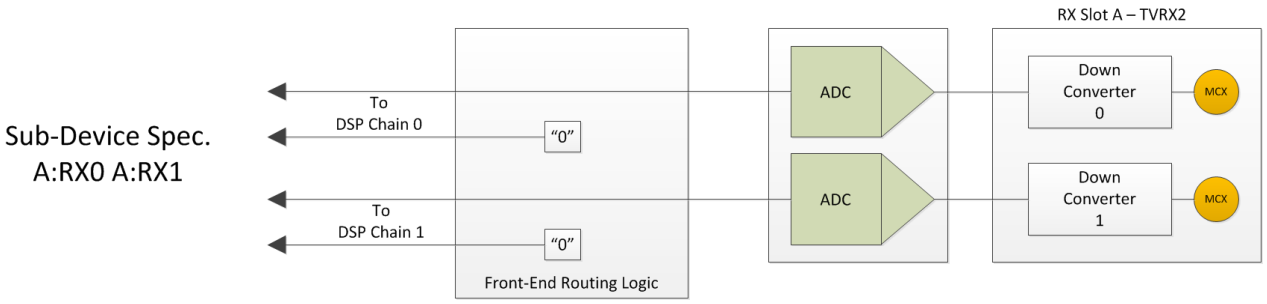


Figure 3 - Multi-Channel Front-End Configuration

## Transceiver Sub-Devices

Currently, all transceiver boards provide one frontend in each signal direction. These frontends provide a quadrature interface, and are all referenced as "0" (see Table 1). In this case, the frontend refers to the up-conversion chain or down-conversion chain. Note these frontends share antenna connections, which are controlled independently of the sub-device specification.

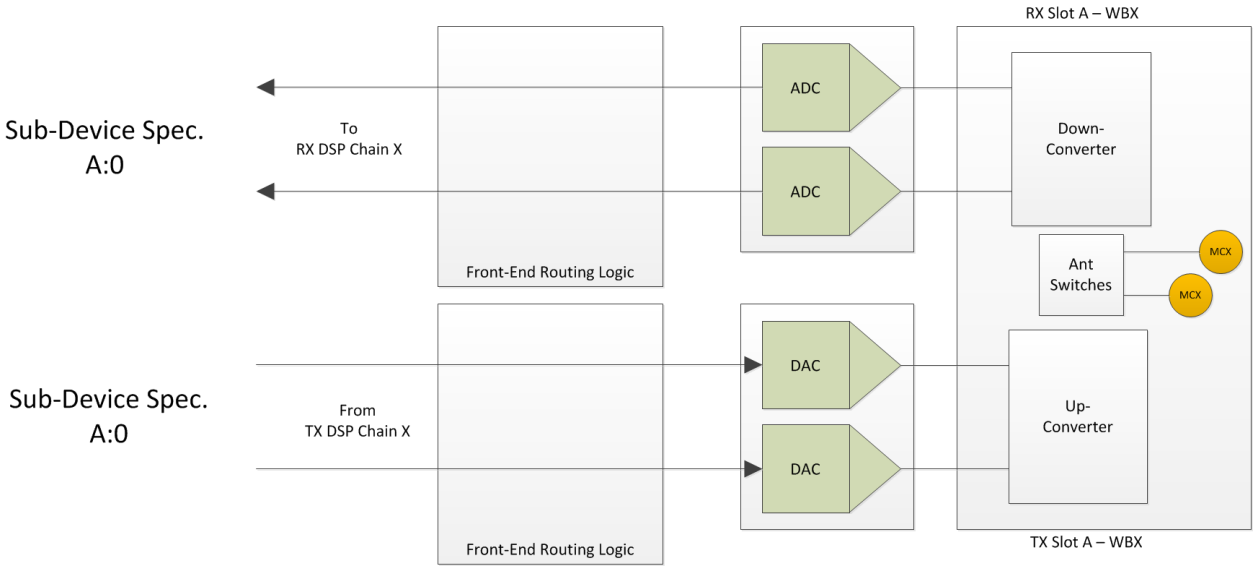


Figure 4 - Typical Transceiver Daughterboard Routing

## Sampling Multiple Channels

As illustrated in Figure 1, each USRP device has two receive chains, and two transmit chains. This enables you to receive two channels and transmit one channel in each direction. In this case, a multi-channel USRP device must be created, and multiple sub-device specifications must be provided. The frontends are assigned to the DSP chain in the order they occur. For example, the sub-device specification "A:A A:B" routes the IF-sampled signals of Slot A, frontend A to DSP 0, and Slot A, frontend B to DSP 1. It is also possible to reference a frontend in a different slot, and each specific frontend

provides an IF or quadrature interface. UHD will automatically configure any frontend routing logic accordingly.

**Transceiver Antenna Selection – Half-Duplex vs. Full Duplex**

All transceiver daughterboards, except for the XCVR2450, offer full-duplex capability. Full-duplex capability allows the application to receive and transmit at the same time. Currently, these full-duplex daughterboards provide two connectors, TX/RX and RX2. TX/RX can be used for transmission or reception. The other connector, RX2, can be used for reception only. In full-duplex operation, RX2 is used for the receive path, and TX/RX is used for the transmission path. The application may still use a single antenna for full-duplex operation if an external duplexer is used.

If the application requires the USRP device to operate in half-duplex mode with a single antenna (per USRP), the TX/RX connector can be used for transmission and reception. In this mode, automatic transmit-receive (ATR) logic switches the TX/RX port to the transmit path when the host is streaming samples. When transmit streaming stops, a state-machine in the FPGA will automatically switch the TX/RX port to the receive path. This functionality can be overridden with UHD API calls to control the transmit/receive switches through GPIO.

Figure 5 shows the RF switch configuration of the SBX daughterboard. Other daughterboards, such as the WBX, may use a different implementation but the functionality is the same.

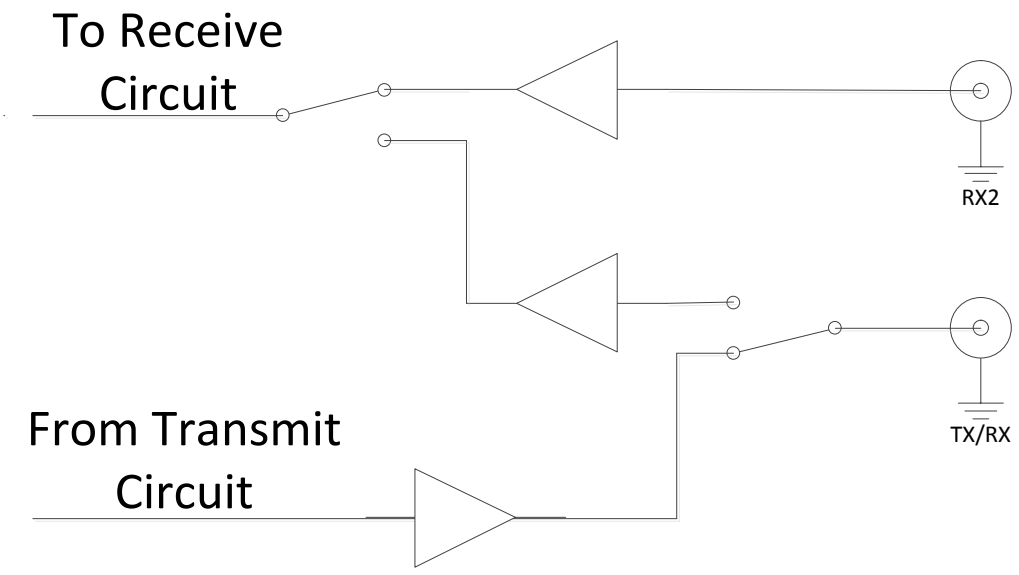


Figure 5 - Transmit and Receive Switching for RF Ports on Transceiver Daughterboards

**Conclusion**

This document provides a brief overview of daughterboard frontends, sub-device specifications, and antenna port selection. If you have any additional questions, please contact support@ettus.com.