# **Octal Bus Transceiver**

# With 5 V-Tolerant Inputs

The MC74LVX245 is an advanced high speed CMOS octal bus transceiver.

It is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by the level of the  $T/\overline{R}$  input. The output enable pin  $(\overline{OE})$  can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

#### **Features**

- High Speed:  $t_{PD} = 4.7 \text{ ns (Typ)}$  at  $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V<sub>OLP</sub> = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V; Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

#### **Application Notes**

- Do not force a signal on an I/O pin when it is an active output, damage may occur
- All floating (high impedance) input or I/O pins must be fixed by means of pullup or pulldown resistors or bus terminator ICs
- A parasitic diode is formed between the bus and V<sub>CC</sub> terminals.
   Therefore, the LVX245 cannot be used to interface 5.0 V to 3.0 V systems directly

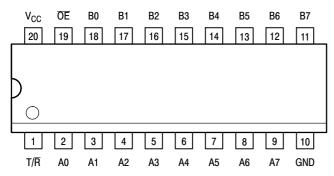


Figure 1. 20-Lead Pinout (Top View)

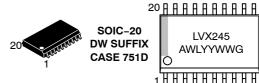
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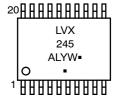
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#### MARKING DIAGRAMS









LVX245 = Specific Device Code A = Assembly Location

WL, L = Wafer Lot Y = Year WW, W = Work Week G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

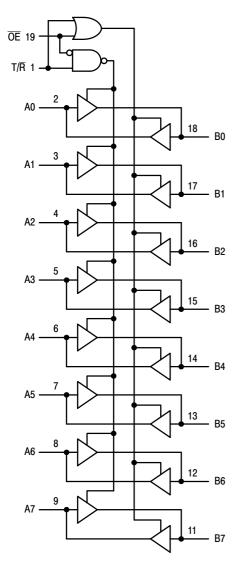


Figure 2. Logic Diagram

### **Table 1. PIN NAMES**

Pins	Function
OE	Output Enable Input
T/R	Transmit/Receive Input
A0-A7	Side A 3-State Inputs or 3-State Outputs
Bo-B7	Side B 3-State Inputs or 3-State Outputs

INP	JTS	OPERATING MODE
OE	T/R	Non-Inverting
L	L	B Data to A Bus
L	Н	A Data to B Bus
Н	Х	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions are Acceptable; For I<sub>CC</sub> reasons, Do Not Float Inputs

## **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
MC74LVX245DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74LVX245DTR2G	TSSOP-20*	2500 / Tape & Reel
MC74LVX245MG	SOEIAJ-20 (Pb-Free)	50 Units / Rail
MC74LVX245MELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

### **MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (T/R, OE)	-0.5 to +7.0	V
V <sub>I/O</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> +0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
I <sub>OK</sub>	Output Diode Current	±20	mA
l <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±75	mA
P <sub>D</sub>	Power Dissipation	180	mW
T <sub>stg</sub>	Storage Temperature	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

### **RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	3.6	V
V <sub>in</sub>	DC Input Voltage (T/R, OE)	0	5.5	V
V <sub>I/O</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

# DC ELECTRICAL CHARACTERISTICS

			v <sub>cc</sub>	Т	A = 25°	С	$T_A = -40$	) to 85°C	
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
V <sub>IH</sub>	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V <sub>IL</sub>	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V <sub>OH</sub>	High-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V <sub>OL</sub>	Low-Level Output Voltage (V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub> )	I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 50 μA I <sub>OL</sub> = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I <sub>in</sub>	Input Leakage Current	$V_{in} = 5.5 \text{ V or GND}$ (T/R, $\overline{\text{OE}}$ )	3.6			±0.1		±1.0	μΑ
l <sub>OZ</sub>	Maximum 3-State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	3.6			±0.2 5		±2.5	μΑ
I <sub>CC</sub>	Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	μΑ

### AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$ )

					A = 25°	С	$T_A = -40$	) to 85°C	
Symbol	Parameter	Test Con	ditions	Min	Тур	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Input to Output	V <sub>CC</sub> = 2.7 V	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		6.1 8.6	10.7 14.2	1.0 1.0	13.5 17.0	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		4.7 7.2	6.6 10.1	1.0 1.0	8.0 11.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time to High and Low Level	$V_{CC} = 2.7 \text{ V}$ $R_L = 1 \text{ k}\Omega$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		9.0 11.5	16.9 20.4	1.0 1.0	20.5 24.0	ns
		$V_{CC}$ = 3.3 $\pm$ 0.3 $V$ $R_L$ = 1 $k\Omega$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time From High and Low Level	$V_{CC} = 2.7 \text{ V}$ $R_L = 1 \text{ k}\Omega$	C <sub>L</sub> = 50 pF		11.5	18.0	1.0	21.0	ns
		$\begin{aligned} V_{CC} &= 3.3 \pm 0.3 \text{ V} \\ R_L &= 1 \text{ k} \Omega \end{aligned}$	C <sub>L</sub> = 50 pF		9.6	12.8	1.0	14.5	
toshl toslh	Output-to-Output Skew (Note 1)	V <sub>CC</sub> = 2.7 V V <sub>CC</sub> = 3.3 ±0.3 V	C <sub>L</sub> = 50 pF C <sub>L</sub> = 50 pF			1.5 1.5		1.5 1.5	ns

Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device.
 The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>); parameter guaranteed by design.

#### **CAPACITIVE CHARACTERISTICS**

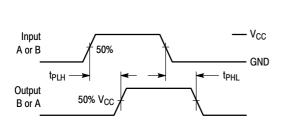
		T <sub>A</sub> = 25°C		T <sub>A</sub> = - 40 to 85°C			
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit
C <sub>in</sub>	Input Capacitance (T/R, OE)		4	10		10	pF
C <sub>I/O</sub>	Maximum 3-State I/O Capacitance		8				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 2)		21				pF

<sup>2.</sup> C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/8 (per bit). C<sub>PD</sub> is used to determine the no–load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

# **NOISE CHARACTERISTICS** (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

		T <sub>A</sub> = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.5	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	-0.5	-0.8	V
V <sub>IHD</sub>	Minimum High Level Dynamic Input Voltage		2.0	V
V <sub>ILD</sub>	Maximum Low Level Dynamic Input Voltage		0.8	V

# **SWITCHING WAVEFORMS**

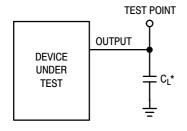


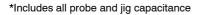
 $V_{CC}$ 50% GND  $V_{\text{CC}}$ 50% V<sub>CC</sub> 50% V<sub>CC</sub> ŌΕ GND t<sub>PZL</sub>  $t_{PLZ}$ HIGH **IMPEDANCE** 50% V<sub>CC</sub>  $A \ \text{or} \ B$  $V_{OL}$  +0.3Vt<sub>PZH</sub> t<sub>PHZ</sub> - $V_{OH}$  -0.3V50% V<sub>CC</sub> A or B HIGH **IMPEDANCE** 

Figure 3.

Figure 4.

# **TEST CIRCUITS**





DEVICE UNDER TEST  $\begin{array}{c|c} & & & & & & & \\ \hline DEVICE & & & & & & \\ UNDER & & & & & \\ TEST & & & & & \\ \hline \end{array}$ 

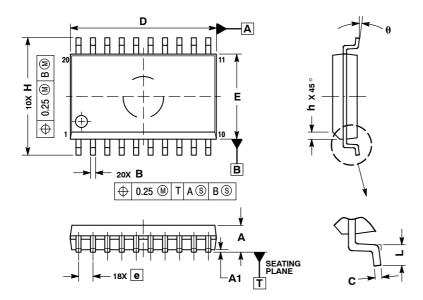
\*Includes all probe and jig capacitance

Figure 5. Propagation Delay Test Circuit

Figure 6. 3-State Test Circuit

#### PACKAGE DIMENSIONS

SOIC-20 CASE 751D-05 ISSUE G



- NOTES:

  1. DIMENSIONS ARE IN MILLIMETERS.

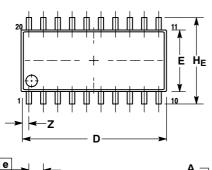
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

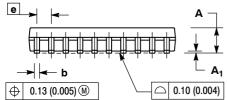
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.

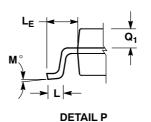
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- MAXIMUM MUDEL PROTROSION U. 15 PER 31M DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

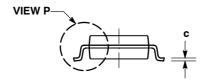
	MILLIN	MILLIMETERS					
DIM	MIN	MAX					
Α	2.35	2.65					
A1	0.10	0.25					
В	0.35	0.49					
С	0.23	0.32					
D	12.65	12.95					
E	7.40	7.60					
е	1.27	BSC					
Н	10.05	10.55					
h	0.25	0.75					
Ĺ	0.50	0.90					
θ	0 °	7 °					

SOEIAJ-20 CASE 967-01 **ISSUE A** 









#### NOTES:

- 17ES:

  1. DIMENSIONING AND TOLERANCING PER ANSI '714.5M, 1982.

  2. CONTROLLING DIMENSION: MILLIMETER.

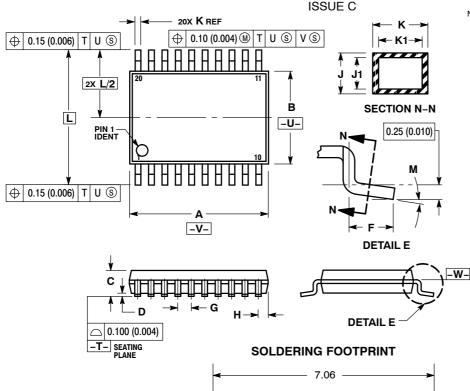
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15
- OH PHO INUSIONS SHALL NOI EXCEED 0.15
  (0.006) PER SIDE.

  4. TERMINAL NUMBERS ARE SHOWN FOR
  REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT
  INCLUDE DAMBAR PROTRUSION. ALLOWABLE
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT, MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.15	0.25	0.006	0.010
D	12.35	12.80	0.486	0.504
Е	5.10	5.45	0.201	0.215
е	1.27	BSC	0.050	BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
ᄪ	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10°
$Q_1$	0.70	0.90	0.028	0.035
Z		0.81		0.032

#### PACKAGE DIMENSIONS

#### TSSOP-20 CASE 948E-02



0.65 **PITCH** 

DIMENSIONS: MILLIMETERS

- 1. DIMENSIONING AND TOLERANCING PER
- ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION:
- MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8°	

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