XBeeO2

Variant: [No Variations]

16/05/2014
V1I1

PRELIMINARY

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

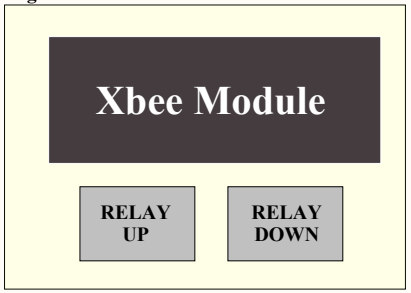
XBeeO2			iElectronic Intelligent Electronic
[01] - COVER PAGE.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 1 **Of** 7	

XBeeO2

(Block Diagram)

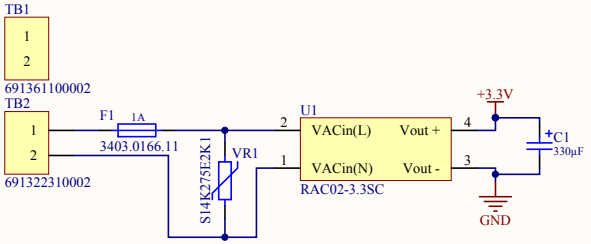
Page 1

Page 2



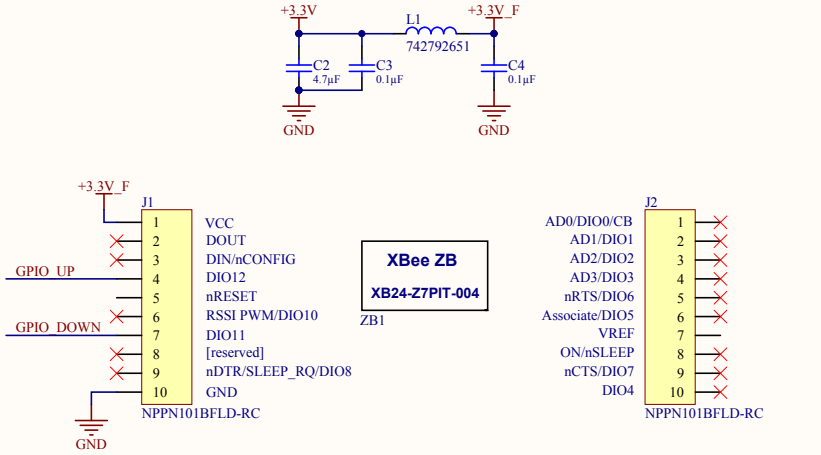
XBeeO2			iElectronic Intelligent Electronic
[02] - BLOCK DIAGRAM.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 2 **Of** 7	

POWER AC/DC



XBeeO2			iElectronic Intelligent Electronic
[03] - POWER.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 3 **Of** 7	

XBEE MODULE



Pin #	Name	Direction	Default State	Description
1	VCC	-	-	Power supply
2	DOUT	Output	Output	UART Data Out
3	DIN / $\overline{\text{CONFIG}}$	Input	Input	UART Data In
4	DIO12	Both	Disabled	Digital I/O 12
5	$\overline{\text{RESET}}$	Both	Open-Collector with pull-up	Module Reset (reset pulse must be at least 200 ns)
6	RSSI PWM / DIO10	Both	Output	RX Signal Strength Indicator / Digital IO
7	DIO11	Both	Input	Digital I/O 11
8	[reserved]	-	Disabled	Do not connect
9	$\overline{\text{DTR}}$ / SLEEP_RQ/ DIO8	Both	Input	Pin Sleep Control Line or Digital IO 8
10	GND	-	-	Ground
11	DIO4	Both	Disabled	Digital I/O 4
12	$\overline{\text{CTS}}$ / DIO7	Both	Output	Clear-to-Send Flow Control or Digital I/O 7. CTS, if enabled, is an output.
13	ON / $\overline{\text{SLEEP}}$	Output	Output	Module Status Indicator or Digital I/O 9
14	VREF	Input	-	Not used for EM250. Used for programmable secondary processor. For compatibility with other XBEE modules, we recommend connecting this pin voltage reference if Analog sampling is desired. Otherwise, connect to GND.
15	Associate / DIO5	Both	Output	Associated Indicator, Digital I/O 5
16	$\overline{\text{RTS}}$ / DIO6	Both	Input	Request-to-Send Flow Control, Digital I/O 6. RTS, if enabled, is an input.
17	AD3 / DIO3	Both	Disabled	Analog Input 3 or Digital I/O 3
18	AD2 / DIO2	Both	Disabled	Analog Input 2 or Digital I/O 2
19	AD1 / DIO1	Both	Disabled	Analog Input 1 or Digital I/O 1
20	AD0 / DIO0 / Commissioning Button	Both	Disabled	Analog Input 0, Digital IO 0, or Commissioning Button

XBeeO2			iElectronic Intelligent Electronic
[04] - XBEE.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 4 **Of** 7	

DOC: REVISION HISTORY

09-JAN-2014 **Started project.**

XBeeO2			iElectronic Intelligent Electronic
[05] - DOC REVISION HISTORY.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 5 **Of** 7	

MECHANICAL

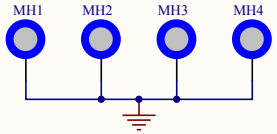
PCB

PCB1

PCB

XBeeO2 V1I1 PCB

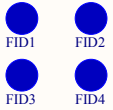
MOUNTING HOLES



Mounting holes 5mm pad 2.2mm drill1

BOARD MOUNTING HOLES - ONE IN EACH CORNER

FIDUCIALS



XBeeO2			iElectronic Intelligent Electronic
[06] - MECHANICAL.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 6 **Of** 7	

[01] - COVER PAGE.SchDoc
[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc

[03] - POWER.SchDoc
[03] - POWER.SchDoc

[04] - XBEE.SchDoc
[04] - XBEE.SchDoc

[05] - DOC REVISION HISTORY.SchDoc
[05] - DOC REVISION HISTORY.SchDoc

[06] - MECHANICAL.SchDoc
[06] - MECHANICAL.SchDoc

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example

Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

XBeeO2			iElectronic Intelligent Electronic
XBeeO2_V1I1.SchDoc			
Date: 16/05/2014	**Rev:** V1I1	**Sheet:** 7 **Of** 7	