Meltdown and Spectre Samples

Written in Assembly

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Contents

1	Intr	oduction	5
	1.1	Overview	5
	1.2	Conventions	5
		1.2.1 Introduction	5
		1.2.2 Data Sections	5
	1.3	Nasm	5
2	Cac	he Access Timing	7
	2.1	Introduction	7
	2.2	Detect Cache Access Time	7
		2.2.1 High Resolution Timer	7
		2.2.2 Cache Access Time Routine	8
	2.3	Measure Cache Access Time	8
		2.3.1 Setup	8
		•	10
	2.4		13
			13
			13
		•	14
3	Sign	nals	19
•	3.1		19
	3.2		19
	3.3		19
4	Heili	ities	21
•	4.1		21 21
	4.2		$\frac{21}{21}$
	4.3	9	$\frac{21}{22}$
	$\frac{4.3}{4.4}$		23
	4.4		$\frac{23}{23}$
		9 9	$\frac{23}{23}$
	4.5	9 9	$\frac{25}{25}$
	4.0		$\frac{25}{25}$
۸	Clea		29
A	Glos		
В	Acre	onyms	31

Contents

C	x86-	Instructions	33
D	Cod	e Chunks	35
E	Lice	nse	37
	E.1	GNU Free Documentation License	37
	E.2	Code License	46
		E.2.1 GNU GENERAL PUBLIC LICENSE	46
		E.2.2 Code Chunk of GPL	60

1 Introduction

1.1 Overview

TBD

1.2 Conventions

1.2.1 Introduction

In this section we define some convention that are specific for this document.

1.2.2 Data Sections

The data is divided into three parts: read-only data, initialized data and uninitialized data. Code chunks with this type of data will all have defined sufficies.

Definition 1 Read-only data is data that is not modified during program execution. The suffix for read-only data is **-rodata**.

Definition 2 Initialized data is data that is changeable during program execution. The data is already initialized with data when the program starts. The suffix for initialized data is **-idata**.

Definition 3 Uninitialized data is data that is changeable during program execution. The data is not initialized. The suffix for uninitialized data is **-udata**.

1.3 Nasm

pagesize, used in chunks 8, 9, 13, 14, 17b, and 18.

2 Cache Access Timing

2.1 Introduction

TBD

2.2 Detect Cache Access Time

2.2.1 High Resolution Timer

First we need a high resolution timer to determine the cache access time. For this we use the time stamp counter. The time stamp counter is monotonically incrementing. When reading the time stamp counter (with rdtsc) the result is delivered back in the registers EDX and EAX forming a 64bit value. The time stamp counter is not an absolute value but a relative value, meaning that you cannot (easily) calculate from the time stamp counter to some time units (e.g. ns). But this is no problem as we only want to measure relative times.

To retrieve a 64bit value for the time we shift the value in EDX 32 bits to the left and add the value of EAX to this.

7
$$\langle tsc\text{-}64bit \ 7 \rangle \equiv$$
 (8a)

rdtsc

shl RDX,32

add RAX,RDX

2.2.2 Cache Access Time Routine

Next we need a routine that calculates the cache access time for us.

First we have to ensure in this routine that the speculative execution of the processor does not interfere with our time measurement. For this we use the instruction lfence which ensures that all previous reads are done before executing the next instructions.

Next we access a memory location with the address RDI by loading this into RCX and measure the time before and after the access.

The command lfence before reading the time stamp counter is needed because we have to ensure that all reads before the time measurements are done.

At last we calculate the relative time needed to access the memory location. In theory we should see a difference whether the memory location is accessed before or not.

Parameters

RDI the address of the memory which is loaded either from the cache or from memory

```
\langle calculate\text{-}cache\text{-}access\text{-}time \ 8a \rangle \equiv
                                                                                                                                     (12\ 18)
8a
             _calccachetime:
                      lfence
             \langle tsc-64bit 7 \rangle
                      mov
                                        R8, RAX
                      mov
                                        RCX, [RDI]
                      lfence
             \langle tsc-64bit 7 \rangle
                      sub
                                        RAX,R8
                      ret
          Defines:
```

_calccachetime, used in chunks 10c, 11b, and 16.

2.3 Measure Cache Access Time

2.3.1 **Setup**

To measure the cache timing we create a standalone program that shows us the time for a cached and for an uncached memory access.

First we need some area in memory with data which we can later read from. This data area goes into the area .bss which contains uninitialized data. We align the data at a page boundary and reserve 2 pages for our data.

```
8b \langle cache\text{-}data \ 8b \rangle \equiv (9b 18)

data: resb pagesize

Defines:
data, used in chunks 9-11, 13a, and 14b.
Uses pagesize 5.
```

From time to time we need a small scratch area so we define an area with 32 bytes.

9a
$$\langle scratch-data \ 9a \rangle \equiv$$
 (9b)

scratch: resb 32

Defines:

scratch, used in chunk 11.

9b
$$\langle cachetiming\text{-}udata 9b \rangle \equiv$$
 (12)

align pagesize

 $\langle cache\text{-}data \ 8b \rangle$

 $\langle scratch\text{-}data 9a \rangle$

Uses pagesize 5.

The program begins with the label _start.

9c
$$\langle cachetiming\text{-}program \text{ 9c} \rangle \equiv$$
 (12) 9d \triangleright

_start:

9d

Uses _start 5.

Now we start with initialising the data area with some random data. For this we load RDI with the address of the data area.

$$\langle cachetiming\text{-}program 9c \rangle + \equiv$$
 (12) $\triangleleft 9c 9e \triangleright$

mov RDI, data

Uses data 8b.

Next we load the number of bytes to fill into RSI. For this we load the pagesize into RSI.

9e
$$\langle cachetiming-program \ 9c \rangle + \equiv$$
 (12) $\triangleleft 9d \ 9f \triangleright$

mov RSI, pagesize

Uses pagesize 5.

At last we load EDX with some random seed. For this we use rdtsc and only use the lower 32 bit of the value.

9f
$$\langle cachetiming-program \ 9c \rangle + \equiv$$
 (12) $\triangleleft 9e \ 9g \triangleright$

rdtsc

mov EDX, EAX

Now we call _xorshift to fill the data area.

9g
$$\langle cachetiming-program \ 9c \rangle + \equiv$$
 (12) $\triangleleft 9f \ 10a \triangleright$

call _xorshift

Uses _xorshift 22a.

2.3.2 Measure Time

Now that we have setup our data area we can now cache data from the first page by loading it into a register which also loads this into the cache.

For this we load RDI with the address of the data area.

```
10a \langle cachetiming\text{-}program 9c \rangle + \equiv (12) \triangleleft 9g 10b \triangleright mov RDI, data
```

Uses data 8b.

Before we load the data into a register now we will clear the cache lines with the given address. For this we use the instruction clflush. After flushing the cache line we ensure (with lfence) that all reads from memory are finished before we load the data into a register again (and filling the cache).

```
10b ⟨cachetiming-program 9c⟩+≡ (12) ⊲10a 10c⊳
clflush [RDI]
lfence
mov RCX,[RDI]
```

Now we can determine the time that is needed to load this data once again. We do not need to load RDI again because it has not changed.

```
10c \langle cachetiming\text{-}program \text{ 9c} \rangle + \equiv (12) \triangleleft 10b 10e \triangleright call _calcachetime
```

Uses _calccachetime 8a.

Now we have the relative cache access time in register RAX. We store this value to the stack and print out an explaining text.

For this we define the text to print and (as a helper) a carriage return (CR).

```
10d \langle cachetiming\text{-}rodata \ 10d \rangle \equiv (12) 11c> scr: db 0x0a scached: db "Cached Access Time: ",0x00
```

Defines:

scached, used in chunk 10e. scr, used in chunk 11.

Now we can print the text.

```
10e \langle cachetiming\text{-}program \ 9c \rangle + \equiv (12) \triangleleft 10c 11a> push RAX mov RDI, scached call _print
```

Uses $\mbox{-print }24a \ {\rm and } \ {\rm scached } \ 10d.$

Then we restore the value and print the measured time to **stdout**. At last we append a CR to the output.

```
11a \langle cachetiming\text{-}program \ 9c \rangle + \equiv (12) \triangleleft 10e 11b\triangleright pop RDI mov RSI,scratch call _printdu64bit mov RSI,scr mov RDI,1 call _nprint
```

Uses _nprint 23b, _printdu64bit 25a, scr 10d, and scratch 9a.

Now we do the same with an uncached value. The difference is that we do not load the value before.

```
11b ⟨cachetiming-program 9c⟩+≡ (12) ⊲11a 11d⊳
mov RDI,data
clflush [RDI]
lfence
call _calccachetime
```

Uses _calccachetime 8a and data 8b.

Now we have the time of the uncached data access in RAX and can print it out with some explaining text.

```
11c \langle cachetiming\text{-}rodata \ 10d \rangle + \equiv (12) \triangleleft 10d suncached: db "Uncached Access Time: ",0x00
```

Defines:

suncached, used in chunk 11d.

```
11d
        \langle cachetiming-program \ 9c \rangle + \equiv
                                                                                      (12) ⊲11b 11e⊳
                push
                             RAX
                mov
                             RDI, suncached
                call
                             _print
                             RDI
                pop
                             RSI, scratch
                mov
                             _printdu64bit
                call
                             RSI,scr
                mov
                             RDI,1
                mov
                             _nprint
                call
```

 $Uses \verb| _nprint 23b, _print 24a, _printdu64bit 25a, scr 10d, scratch 9a, and suncached 11c.$

At last we exit the program.

```
11e \langle cachetiming-program \ 9c \rangle + \equiv (12) \langle exitProgram \ 21b \rangle
```

2 Cache Access Timing

Now we can put everything together and have our cachetiming program that we can now execute.

```
12 \langle cachetiming.asm \ 12 \rangle \equiv \langle preamble \ 5 \rangle

section .rodata \langle cachetiming-rodata \ 10d \rangle

section .bss \langle cachetiming-udata \ 9b \rangle

section .text \langle cachetiming-program \ 9c \rangle
\langle calculate-cache-access-time \ 8a \rangle
\langle xorshift-prng \ 22a \rangle
\langle utilities \ 21a \rangle
```

The program is placed in asm/. With make in the folder we can create an executable which is moved to bin/. There we can execute this program.

\$./cachetiming

Cached Access Time: 72 Uncached Access Time: 372

\$

2.4 Read Array via Cache Access Time

2.4.1 Introduction

Now that we have seen that we can determine if a value was in the cache or not (see 2.3 Measure Cache Access Time) we will read a complete array of data by only measuring the cache access time.

2.4.2 **Setup**

For this we start with some data area that we can read later as defined before.

So start with the program and fill the data area with some random data (similar to the chunks 9c, 9d, 9e, 9f and 9g).

```
13a ⟨cacheread-program 13a⟩≡
_start:

mov RDI,data
mov RSI,pagesize
rdtsc
mov EDX,EAX
call _xorshift
```

Uses _start 5, _xorshift 22a, data 8b, and pagesize 5.

Next we will create a probe area that is 256 * pagesize. We only access the first byte of each page but we divide the data over such a large area (1 MiB) to ensure that the cache lines that we use do not interfere each other.

```
13b ⟨cacheread-udata 13b⟩≡
    probe: times 256 resb pagesize

Defines:
    probe, used in chunk 14.
Uses pagesize 5. (18) 17b⊳
```

Next we fill this area also with some random data.

```
14a
        \langle cacheread\text{-}program \ 13a \rangle + \equiv
                                                                                                     (18) ⊲13a
                                RDI, probe
                  mov
                  mov
                                RAX, pagesize
                                RCX,256
                  mov
                                RCX
                  mul
                  mov
                                RSI, RCX
                  rdtsc
                                EDX, EAX
                  mov
                  call
                                _xorshift
```

Uses _xorshift 22a, pagesize 5, and probe 13b.

2.4.3 Reading Bytes via Cache

As we saw we can determine if a memory datum is in cache or not. For reading a complete byte we have to do a little bit more. Basically we use the byte accessed to index a different probe area. Because the memory is not cached byte by byte but in so called cache lines we cannot use a simple 256 bytes sized probe array but must at least have a space between the accessed bytes that is larger than a cache line size. This is the reason why we use a probe array of 256 * pagesize bytes of size.

Basically we use the following code to access the data. We load the content of the address we want to probe into a register. Then we multiply the register with some arbitary value (we use pagesize) and the access the probe area with the calculated offset. We can then test the cache which page was cached and have our value from the data.

```
14b \langle cacheread\text{-}sample \ 14b \rangle \equiv
mov RAX,[data]
mul RAX,pagesize
mov RBX,[probe+RAX]
Uses data 8b, pagesize 5, and probe 13b.
```

First we write a subroutine to clear the cache lines from data from our probe area. We assume that we use 256 values (0...255) for the indexing into the probe array. Also the probe area must be at least 256 * RSI bytes in size.

Parameters

```
RDI the address of the probe array
```

RSI the interval between the probe addresses used

```
\langle clear\text{-}cache \ 15 \rangle \equiv
15
                                                                                                      (18)
          _clear_cache:
                cld
                mov
                              RCX,256
                xor
                              RAX, RAX
          .clear_next:
                              RSI
                mul
                              [RDI+RAX]
                clflush
                add
                              RAX,RSI
                loop
                              .clear_next
                lfence
                ret
       Defines:
          _clear_cache, never used.
```

2 Cache Access Timing

Uses _calccachetime 8a.

Next we need a subroutine that determines the cache line access times for the data in the probe area. So we create a subroutine that loops similar to the _clear_cache subroutine over all addresses and measures the cache access time for each page.

Parameters

```
RDI
                    the address of the probe array
                    the interval between the probe addresses used
       RSI
       RDX
                    the address of the results of the cache measurements. The area needs to be
                    256* 8 bytes in size
16
       \langle detect\text{-}cache\text{-}area\text{-}time | 16 \rangle \equiv
                                                                                                    (18)
         _calcareacachetime:
                             RCX,RCX
                xor
          .next_timing:
                push
                             RCX
                call
                             _calccachetime
                             RCX
                pop
                             [RDX+8*RCX], RAX
                mov
                add
                             RDI,RSI
                             RCX
                inc
                cmp
                             RCX,256
                jb
                             .next_timing
                ret
       Defines:
         \_{\tt calcareacachetime}, \, used in \, chunk \, 17a.
```

We now can determine the cache line with the lowest access time. This is the cache line that was cached before.

Parameters

RDI the address of the probe array

RSI the interval between the probe addresses used

RDX the address of the results of the cache measurements. The area needs to be

256 * 8 bytes in size

Return

RAX the byte (in AL) which is found by cache timing analysis

TBD

```
\langle detect\text{-}byte \ 17a \rangle \equiv
17a
                                                                                                (18)
          _detectbytebycl:
                push
                call
                             _calcareacachetime
                             RDI
                pop
                             RSI, RDX
                mov
                             RCX, RCX
                xor
                             R8,0xfffffffffffffff
                mov
                             R9, R9
                xor
          .nextbyte:
                mov
                             RAX, [RDI+8*RCX]
                             RAX, R8
                cmp
                jа
                             .nextbyte
                mov
                             R8,RAX
                mov
                             R9,RCX
                             RCX
                inc
                             RCX,256
                cmp
                jb
                             .nextbyte
                mov
                             RAX, R9
```

Uses _calcareacachetime 16.

ret

Now we need some area to store all the data. Once we use an area for the timing data and another area for the read memory data.

```
17b \langle cacheread\text{-}udata \ 13b \rangle + \equiv (18) \triangleleft 13b result: resb pagesize timing: resq 256

Uses pagesize 5.
```

2 Cache Access Timing

```
\operatorname{TBD}
```

```
\langle cacheread.asm \ 18 \rangle \equiv
18
                \langle preamble 5 \rangle
                section .bss
                           align
                                                            pagesize
                \langle cache-data 8b \rangle
                \langle cacheread\text{-}udata \ 13b \rangle
                section .text
                \langle cacheread\text{-}program 13a \rangle
                \langle exitProgram 21b \rangle
                \langle clear\text{-}cache \ 15 \rangle
                \langle calculate\text{-}cache\text{-}access\text{-}time \ 8a \rangle
                \langle detect\text{-}cache\text{-}area\text{-}time \ 16 \rangle
                \langle detect\text{-}byte \ 17a \rangle
                \langle xorshift\text{-}prng 22a \rangle
                \langle utilities 21a \rangle
            Uses pagesize 5.
```

3 Signals

3.1 Basics

TBD

3.2 Detecting Signals

TBD

3.3 Handling Signals

TBD

4 Utilities

4.1 Introduction

```
TBD
```

```
21a \langle utilities 21a \rangle \equiv (12 18) \langle nprint 23b \rangle \langle print 24a \rangle \langle print du64bit 25a \rangle
```

4.2 Exit Program

TBD

```
21b \langle exitProgram \ 21b \rangle \equiv (11e 18)

xor RDI,RDI

mov RAX,60

syscall
```

4.3 Random Number Generator

To initialize the data a random number generator (RNG) is used. The sample programs use xorshift¹ as RNG.

First we clear the direction flag to ensure that we are incrementing the data pointer RDI.

Next we move the number of values to be generated to RCX (which is a counter in x86 processors) and divide it by 4 (because we use a 32bit RNG). Additionally we move the seed to EAX.

Parameters

RDI the address of the memory which is to be filled with random numbers

RSI the number of bytes that are filled with random numbers. This must be a multiple of 4

EDX the seed of the RNG

```
22a ⟨xorshift-prng 22a⟩≡
_xorshift:
cld
mov RCX,RSI
shr RCX,2
mov EAX,EDX
```

Defines:

_xorshift, used in chunks 9g, 13a, and 14a.

Now we can generate the next 32bit random number.

```
\langle xorshift\text{-}prng 22a \rangle + \equiv
22b
                                                                                             (12 18) ⊲22a 23a⊳
            .next_random:
                  mov
                                 EBX, EAX
                  shl
                                 EAX,13
                                 EAX, EBX
                  xor
                                 EBX, EAX
                  mov
                                 EAX, 17
                  shr
                                 EAX, EBX
                  xor
```

mov EBX,EAX shl EAX,5 xor EAX,EBX

¹https://en.wikipedia.org/wiki/Xorshift

Because we want to generate multiple random numbers we store the value of EAX to [RDI] and loop for the next random number.

```
23a \langle xorshift\text{-}prng 22a \rangle + \equiv (12 18) \triangleleft 22b stosd loop .next_random ret
```

4.4 Printing Strings

4.4.1 Printing Strings with Length

The routine _nprint prints a string with the given length to stdout.

We move the number of bytes to print to RDX which is the 3rd parameter to the systemcall. Next we move the address of the bytes to print to RSI which is the 2nd parameter to the systemcall. The 1st argument (in RDI) to the systemcall is the file descriptor (1 is stdout). Additionally the number of the systemcall (1) is passed in RAX. The systemcall (syscall) now prints RDX bytes from [RSI] to the file descriptor RDI.

At the end we return to the caller.

Parameters

```
RDI the number of bytes to print to stdout

RSI the address to the bytes to print to stdout
```

```
23b ⟨nprint 23b⟩≡
_nprint:

mov RDX,RDI

mov RDI,1

mov RAX,1

syscall
ret

(21a)
```

Defines:

_nprint, used in chunks 11, 24d, and 27b.

4.4.2 Printing C-Strings

The routine _print prints a null-terminated string to stdout.

First we clear the direction flag to increment the address in RDI while scanning the data.

Next we start with clearing AL (setting it to null) and saving the address of the string to RSI. We're using RSI because we later need the address to calculate the length of the string.

Parameters

RDI the address to the null-terminated bytes to print to stdout

```
24a ⟨print 24a⟩≡
_print:
cld
xor AL,AL
mov RSI,RDI
```

Defines:

_print, used in chunks 10e and 11d.

Next we search for the terminating null ('\0') character. For this we use the instruction scasb (scan string byte) which compares the byte at the address [RDI] with the value in AL and sets the flags accordingly. When the byte at [RDI] is not the value of AL the next instruction (jne) jumps to the given label (.next_char in this case).

scasb additionally increments RDI so that we go through the string until '\0' is found.

After we have found the string termination we calculate the number of bytes that the string has. In RSI we now have the starting address of the bytes to print and in RDI we have the end address of the bytes to print. After that we calculate the number of bytes to print.

24c
$$\langle print \ 24a \rangle + \equiv$$
 (21a) \triangleleft 24b 24d \triangleright sub RDI,RSI

Now we have the address of the string in RDI and the length of the string in RSI which are the 1st and 2nd argument in the call of _nprint.

4.5 Printing Numbers

4.5.1 Printing a 64bit Unsigned Integer

The routine _printdu64bit print a given number as unsigned decimal number with 64bit to stdout.

To print a decimal number we have to divide the number by 10 and get the remainder for printing (from right to left). For this we move the divisor to a register and the dividend to RAX. We have to use RAX because this is the only register we can use for division.

Additionally we need the address of the scratch area in RDI for storing the result. We also save the address of the scratch area to R8 for later use.

To increment the address during the processing we clear the direction flag.

Parameters

RDI the number number to print to stdout

RSI the address of a scratch area with a size of at least 20 bytes

```
25a ⟨printdu64bit 25a⟩≡ (21a) 25b⊳
_printdu64bit:

mov RAX,RDI
mov RDI,RSI
mov R8,RDI
mov RCX,10
cld
```

Defines:

 $\verb|_printdu64bit|, used in chunk 11|.$

Now we define a label to jump back when we see that there are still more digits to print. Then we test RAX for 0 and end the processing of the digits.

```
25b \langle printdu64bit 25a \rangle + \equiv (21a) \triangleleft 25a 25c \triangleright .next: cmp RAX,0 je .done
```

Next we divide RAX by RCX. For this we have to clear RDX because this is the higher value of the dividend. The result is then placed into RAX and the remainder into RDX.

```
25c \langle printdu64bit 25a \rangle + \equiv (21a) \triangleleft 25b 26a \triangleright xor RDX,RDX div RCX
```

We now exchange the result and the remainder because we now need the remainder in RAX (or AL) for further processing. Now we can add the ASCII character '0' to AL and have the correct ASCII value in AL. Now we can store the ASCII character to the scratch area.

```
26a \langle printdu64bit 25a \rangle + \equiv (21a) \triangleleft 25c 26b \triangleright xchg RDX,RAX add AL,'0' stosb
```

Now we restore RAX (which we saved to RDX) to go into the next round.

```
26b \langle printdu64bit 25a \rangle + \equiv (21a) \triangleleft 26a 26c \triangleright mov RAX,RDX jmp .next
```

Now that we have all the numbers as ASCII characters we are nearly done. We now have to reverse the number in memory because the number saved at the lowest address is the digit with the least significance.

We now start with checking if we have written any character. If not then we write the ASCII character '0' into the memory. We use the instruction stosb for this to adjust the address in RDI at the same time.

```
26c ⟨printdu64bit 25a⟩+≡ (21a) ⊲26b 26d⊳
.done:

cmp RDI,RSI
jne .printout
mov AL,'0'
stosb
.printout:
```

Next we calculate the number of digits that the number has. For this we move the address of the last digit to RDX and subtract the start of the scratch area from this. Next we adjust RDI because it points to the first address after the number.

```
26d \langle printdu64bit 25a \rangle + \equiv (21a) \triangleleft 26c 27a\triangleright mov RDX,RDI sub RDX,RSI dec RDI
```

We now have RSI with the address of the start of the number and RDI with the address of the end. We now have to exchange the digits from the front and the end to get the right number. For this we increment RSI and decrement RDI after each exchange and when the addresses pass each other we are done.

```
\langle printdu64bit 25a \rangle + \equiv
27a
                                                                                         (21a) ⊲26d 27b⊳
           .reverse:
                 mov
                               AL, [RSI]
                               AH, [RDI]
                 mov
                               [RSI], AH
                 mov
                               [RDI],AL
                 mov
                               RDI
                 dec
                 inc
                               RSI
                 cmp
                               RSI,RDI
                 jb
                               .reverse
```

Now we restore the address of the scratch area to RSI and move the number of digits (which we stored in RDX) to RDI and can the call _nprint to print the number.

```
27b ⟨printdu64bit 25a⟩+≡ (21a) ⊲27a

mov RSI,R8

mov RDI,RDX

call _nprint

ret

Uses _nprint 23b.
```

A Glossary

 ${\bf x86}\,$ x86 denotes a microprocessor architecture based on the $8086/8088\,$ 22

B Acronyms

ASCII American Standard Code for Information Interchange 26

CR carriage return 10, 11

 ${\bf RNG}$ random number generator 22

C x86-Instructions

```
clflush Flush Cache Line, introduced with Intel<sup>®</sup> Pentium<sup>®</sup> 4 10

lfence Load Fence, introduced with Intel<sup>®</sup> Pentium<sup>®</sup> 4 8, 10

rdtsc Read Time Stamp Counter, introduced with Intel<sup>®</sup> Pentium<sup>®</sup> 7, 9
```

D Code Chunks

```
\langle cache-data 8b \rangle
\langle cacheread\text{-}program 13a \rangle
\langle cacheread\text{-}sample | 14b \rangle
\langle cacheread\text{-}udata \ 13b \rangle
\langle cacheread.asm \ 18 \rangle
\langle cachetiming-program \ 9c \rangle
\langle cachetiming-rodata \ 10d \rangle
\langle cachetiming-udata | 9b \rangle
\langle cachetiming.asm 12 \rangle
\langle calculate\text{-}cache\text{-}access\text{-}time \ 8a \rangle
\langle clear\text{-}cache \ 15 \rangle
\langle detect-byte 17a\rangle
\langle detect\text{-}cache\text{-}area\text{-}time | 16 \rangle
\langle exitProgram 21b \rangle
\langle license 60 \rangle
\langle nprint 23b \rangle
\langle preamble 5 \rangle
\langle print 24a \rangle
\langle printdu64bit 25a \rangle
\langle scratch\text{-}data 9a \rangle
\langle tsc-64bit 7 \rangle
\langle utilities 21a \rangle
\langle xorshift\text{-}prng 22a \rangle
```

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- d) Convey the object code by offering access from a designated place (gratis or for a charge), and offer equivalent access to the Corresponding Source in the same way through the same place at no further charge. You need not require recipients to copy the Corresponding Source along with the object code. If the place to copy the object code is a network server, the Corresponding Source may be on a different server (operated by you or a third party) that supports equivalent copying facilities, provided you maintain clear directions next to the object code saying where to find the Corresponding Source. Regardless of what server hosts the Corresponding Source, you remain obligated to ensure that it is available for as long as needed to satisfy these requirements.
- e) Convey the object code using peer-to-peer transmission, provided you inform other peers where the object code and Corresponding Source of the work are being offered to the general public at no charge under subsection 6d.

A separable portion of the object code, whose source code is excluded from the Corresponding Source as a System Library, need not be included in conveying the object code work.

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