

x86 Assembly Tutorial

From 8086 to Intel Core Processors

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1 Introduction

1.1 Overview

The [x86](#) architecture is a wide spread microprocessor architecture used today. From time to time it could be helpful to understand the architecture more in depth or even develop some parts of a program in assembly language because you either want to tune the performance or to reduce the space needed.

In this book I will go through the assembly language instructions found in modern [x86](#) processors. I will start with the [8086](#) assembly language in chapter 2 and go on to the [8087](#) assembly language extensions in chapter 3, which is the first [x87 floating point unit \(FPU\)](#).

Further on I will visit the other CPUs in historical order. We go on with the [80286](#) in chapter 6, the [80386](#) in chapter 8 and the [80486](#) in chapter 10.

After that I will not go on with different processors but with features. This starts with the chapter [Processor with CPUID](#) which is the first feature I'll discuss. This is the base for all other features because with the [CPUID](#) you can determine all other features. This is because not every processor implements all features.

I start with the [8086](#) and go on through all other succeeding processors because some of the idiosyncrasies of the modern processors can be easier understand if you have the history in mind.

I will look at the processors from the softwares view. If there are differences in the hardware I do not concern as long as it does not influence the software run on the processor.

1.2 Environment

2 8086

2.1 Introduction

- released 1978 (Intel)
- Intel 8086
- Intel 8088
- AMD 8086
- AMD 8088

2.2 Special Commands

TBD	HLT
TBD	LOCK
TBD	NOP
TBD	WAIT

2.3 Moving Data Around

TBD	CBW
TBD	CWD
TBD	LAHF
TBD	MOV
TBD	SAHF
TBD	XCHG

2.4 Doing Arithmetic

TBD	AAA
TBD	AAD
TBD	AAM
TBD	AAS
TBD	ADC
TBD	ADD
TBD	DAA

DAS	TBD
DEC	TBD
DIV	TBD
IDIV	TBD
IMUL	TBD
INC	TBD
MUL	TBD
NEG	TBD
SBB	TBD
SUB	TBD
XCHG	TBD

2.5 Doing Boolean Arithmetic

AND	TBD
NOT	TBD
OR	TBD
XOR	TBD

2.6 Shifting and Rotating

RCL	TBD
RCR	TBD
ROL	TBD
ROR	TBD
SAL	TBD
SAR	TBD
SHL	TBD
SHR	TBD

2.7 Accessing Memory

LDS	TBD
LEA	TBD
LES	TBD
LODS	TBD
MOV	TBD
MOVS	TBD
SCAS	TBD
STOS	TBD
XCHG	TBD
XLAT	TBD

2.8 Conditions and Control Flow

TBD	CLC
TBD	CLD
TBD	CMC
TBD	CMP
TBD	CMPS
TBD	Jcc
TBD	JMP
TBD	LOOP/LOOPcc
TBD	REPcc
TBD	STC
TBD	STD
TBD	TEST

2.9 Using Subroutines

TBD	CALL
TBD	POP
TBD	POPF
TBD	PUSH
TBD	PUSHF
TBD	RET

2.10 Interrupting Work and Using System Subroutines

TBD	CLI
TBD	INT
TBD	INTO
TBD	IRET
TBD	STI

2.11 Communicating with Periphery

TBD	IN
TBD	OUT

3 8087

- released 1980 (Intel)
- Intel 8087

[illegible]

F2XM1
FABS
FADD
FADDP
FBLD
FBSTP
FCHS
FCLEX
FCOM
FCOMP
FCOMPP
FDECSTP
FDISI
FDIV
FDIVP
FDIVR
FDIVRP
FENI
FFREE
FIADD
FICOM
FICOMP
FIDIV
FIDIVR
FILD
FIMUL
FINCSTP
FINIT
FIST
FISTP
FISUB
FISUBR
FLD

FLD1	TBD
FLDCW	TBD
FLDENV	TBD
FLDL2E	TBD
FLDL2T	TBD
FLDLG2	TBD
FLDLN2	TBD
FLDPI	TBD
FLDZ	TBD
FMUL	TBD
FMULP	TBD
FNCLEX	TBD
FNDISI	TBD
FNENI	TBD
FNINIT	TBD
FNOP	TBD
FNSAVE	TBD
FNSTCW	TBD
FNSTENV	TBD
FNSTSW	TBD
FPATAN	TBD
FPREM	TBD
FPTAN	TBD
FRNDINT	TBD
FRSTOR	TBD
FSAVE	TBD
FSCALE	TBD
FST	TBD
FSTCW	TBD
FSTENV	TBD
FSTP	TBD
FSTSW	TBD
FSUB	TBD
FSUBP	TBD
FSUBR	TBD
FSUBP	TBD
FTST	TBD
FWAIT	TBD
FXAM	TBD
FXCH	TBD
FXTRACT	TBD
FYL2X	TBD
FYL2XP1	TBD

4 80186

- released 1982 (Intel)
- Intel 80186

TBD	BOUND
TBD	ENTER
TBD	INS
TBD	LEAVE
TBD	OUTS
TBD	POPA
TBD	PUSHA
TBD (immediate)	PUSH
TBD (immediate)	IMUL
TBD (immediate)	SHL
TBD (immediate)	SHR
TBD (immediate)	SAL
TBD (immediate)	SAR
TBD (immediate)	ROL
TBD (immediate)	ROR
TBD (immediate)	RCL
TBD (immediate)	RCR

5 80187

- released ??? (Intel)
- Intel 80187 (8087 interface/80387 core)

6 80286

- released 1982 (Intel)
- Intel 80286
- i286 (Intel)
- Am286 (AMD)

TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD
TBD

ARPL
CLTS
LAR
LGDT
LIDT
LLDT
LMSW
LSL
LTR
SGDT
SIDT
SLDT
SMSW
STR
VERR
VERW

7 80287

- released ??? (Intel)
- Intel 80287
- i287 (Intel)

TBD

FSETPM

8 80386

- released 1985 (Intel)
- Intel 80386
- i386 (Intel)
- Am386 (AMD)

TBD (extend)	ADC
TBD (extend)	ADD
TBD (extend)	AND
TBD (extend)	BOUND
TBD	BSF
TBD	BSR
TBD	BT
TBD	BTC
TBD	BTR
TBD	BTS
TBD (extend)	CALL
TBD	CDQ
TBD (extend)	CMP
TBD (extend)	CMPS
TBD	CWDE
TBD (extend)	DEC
TBD (extend)	DIV
TBD (extend)	ENTER
TBD (extend)	IDIV
TBD (extend)	IMUL
TBD (extend)	IN
TBD (extend)	INC
TBD (extend)	INS
TBD (extend)	IRET
TBD (extend)	Jcc
TBD (extend)	JMP
TBD (extend)	LAR
TBD	LFS
TBD	LGS
TBD	LSS

LEA	TBD (extend)
LEAVE	TBD (extend)
LODS	TBD (extend)
LOOP/LOOPcc	TBD (extend)
LSL	TBD (extend)
MOV	TBD (extend)
MOVS	TBD (extend)
MOVSX	TBD
MOVZX	TBD
MUL	TBD (extend)
NEG	TBD (extend)
NOT	TBD (extend)
OR	TBD (extend)
OUT	TBD (extend)
OUTS	TBD (extend)
POP	TBD (extend)
POPA	TBD (extend)
POPF	TBD (extend)
PUSH	TBD (extend)
PUSHA	TBD (extend)
PUSHF	TBD (extend)
RCL	TBD (extend)
RCR	TBD (extend)
REPcc	TBD (extend)
ROL	TBD (extend)
ROR	TBD (extend)
SAL	TBD (extend)
SAR	TBD (extend)
SBB	TBD (extend)
SCAS	TBD (extend)
SETcc	TBD
SGDT	TBD (extend)
SHL	TBD (extend)
SHLD	TBD
SHR	TBD (extend)
SHRD	TBD
SIDT	TBD (extend)
SMSW	TBD (extend)
STOS	TBD (extend)
SUB	TBD (extend)
TEST	TBD (extend)
XCHG	TBD (extend)
XLAT	TBD (extend)
XOR	TBD (extend)

9 80387

- released 1987 (Intel)
- Intel 80387
- i387 (Intel)

TBD

TBD (extend)

TBD (extend)

TBD (extend)

TBD

TBD (extend)

TBD (extend)

TBD (extend)

TBD (extend)

TBD

TBD

TBD

TBD

TBD

FCOS

FNSAVE

FNSTENV

FNSTSW

FPREM1

FRSTOR

FSAVE

FSTENV

FSTSW

FSIN

FSINCOS

FUCOM

FUCOMP

FUCOMPP

10 80486

- released 1989 (Intel)
- i486 (Intel)
- Am486 (AMD)
- Am5x86 (AMD)

TBD
TBD
TBD
TBD
TBD
TBD

BSWAP
CMPXCHG
INVD
INVLPG
WBINVD
XADD

11 RSM

- released 1993 (Intel)

TBD

RSM

12 Processor with CUID

- released 1993 (Intel)
- Intel Pentium (Intel)
- AMD K5 (AMD)

TBD

CUID

13 CX8

- released 1993 (Intel)

TBD

CMPXCHG8B

14 MSR

- released 1993 (Intel)

TBD

TBD

RDMSR

WRMSR

15 TSC

- released 1993 (Intel)
- Invariant TSC

TBD

RD TSC

16 PMC

- released 1997 (Intel)

TBD

RDPMC

17 MMX

- released 1997 (Intel)

[illegible]

EMMS
MOVD
MOVQ
PACKSSDW
PACKSSWB
PACKUSWB
PADDB
PADDW
PADDD
PADDDQ
PADDSB
PADDSW
PADDUSB
PADDUSW
PAND
PANDN
PCMPEQB
PCMPEQW
PCMPEQD
PCMPGTB
PCMPGTW
PCMPGTD
PMADDWD
PMULHW
PMULLW
POR
PSLLW
PSLLD
PSLLQ
PDRAW
PDRAD
PDRAQ
PDRLW
PDRLD
PDRLQ

17 MMX

PSUBB	TBD
PSUBW	TBD
PSUBD	TBD
PSUBSB	TBD
PSUBSW	TBD
PSUBUSB	TBD
PSUBUSW	TBD
PUNPCKHBW	TBD
PUNPCKHDQ	TBD
PUNPCKHWD	TBD
PUNPCKLBW	TBD
PUNPCKLDQ	TBD
PUNPCKLWD	TBD
PXOR	TBD

18 Temp

This is a temporary chapter to help me organize this book.

- CLFSH
- CMPXCHG16B
- CMOV
- RDTSCP
- SEP
- SYSCALL/SYSRET in 64-bit Mode
- 3DNow (AMD)
- MMX ext (AMD)
- 3DNow ext (AMD)
- PREFETCHW (3DNow AMD)
- SSE
- SSE2
- SSE3
- SSSE3
- SSE4A (AMD)
- SSE4.2
- Intel 64 Architecture/Long Mode (AMD)
- MISCSELECT (SGX) (Intel)
- SGX1 (Intel)
- SGX2 (Intel)
- ENCLV (SGX) (Intel)

- ENCLS (SGX) (Intel)
- SVM (AMD)
- AVX
- AVX2
- XOP (AMD)
- AESNI (AES (AMD))
- FMA
- FMA4 (AMD)
- F16C
- RDRAND
- LZCNT (ABM (AMD))
- BMI1
- BMI2
- POPCNT
- TBM (AMD)
- MOVBE
- MONITOR
- MONITORX (AMD)
- PCMULQDQ
- FXSR
- SKINIT (AMD)
- LAHF/SAHF in 64-bit Mode
- FSGSBASE
- SHA
- CLFLUSHOPT (CLFLOPT (AMD))
- SMAP
- ADX

- RDSEED
- SME (AMD)
- SEV (AMD)
- PageFlushMgr (AMD)
- ES (AMD)
- CLZERO (AMD)
- Instruction Retired Counter (AMD)
- Error Pointer (AMD)
- XSAVEOPT
- XSAVEC
- XGETBV
- XSAVES
- XSAVE
- OSXSAVE
- HTT
- PSE-36
- PAT
- MCA
- PGE
- MTRR
- APIC
- MCE
- PAE
- PSE
- DE
- VME
- SMEP

- DTSE64 (Intel)
- MONITOR (Intel)
- DS-CPL (Intel)
- VMX (Intel)
- SMX (Intel)
- EIST (Intel)
- TM2 (Intel)
- CNXT-ID (Intel)
- SDBG (Intel)
- xTPR Update Control (Intel)
- PDCM (Intel)
- PCID (Intel)
- DCA (Intel)
- x2APIC (Intel)
- TSC-Deadline (Intel)
- PSN (Intel)
- DS (Intel)
- ACPI (Intel)
- SS (Intel)
- TM (Intel)
- PBE (Intel)
- Execute Disable Flag (Intel)
- IA32_TSC_ADJUST (Intel)
- HLE (Intel)
- INVPCID (Intel)
- RTM (Intel)
- RDT-M (Intel)

- MPX (Intel)
- RDT-A (Intel)
- AVX512F (Intel)
- AVX512DQ (Intel)
- AVX512_IFMA (Intel)
- CLWB (Intel)
- Intel Processor Trace (Intel)
- AVX512PF (Intel)
- AVX512ER (Intel)
- AVX512CD (Intel)
- AVX512BW (Intel)
- AVX512VL (Intel)

A Glossary

x86 a microprocessor architecture based on the 8086/8088 from Intel [5](#), [47](#)

x87 a mathematical coprocessor for the [x86](#) [5](#), [53–55](#)

B Acronyms

BCD binary coded decimal [52](#)

FPU floating point unit [5](#), [53–55](#)

TLB translation lookaside buffer [56](#)

C x86-Instructions

AAA ASCII adjust AL after addition, introduced with [8086 7](#)

AAD ASCII adjust AX before division, introduced with [8086 7](#)

AAM ASCII adjust AX after multiplication, introduced with [8086 7](#)

AAS ASCII adjust AL after subtraction, introduced with [8086 7](#)

ADC Add with carry, introduced with [8086](#), extended with [80386 7, 21](#)

ADD Add, introduced with [8086](#), extended with [80386 7, 21](#)

AND Logical AND, introduced with [8086](#), extended with [80386 8, 21](#)

ARPL Adjust RPL field of selector, introduced with [80286 17](#)

BOUND Check array index against bounds, introduced with [80186](#), extended with [80386 13, 21](#)

BSF Bit scan forward, introduced with [80386 21](#)

BSR Bit scan reverse, introduced with [80386 21](#)

BSWAP Byte swap, introduced with [80486 25](#)

BTC Bit test and complement, introduced with [80386 21](#)

BTR Bit test and reset, introduced with [80386 21](#)

BTS Bit test and set, introduced with [80386 21](#)

BT Bit test, introduced with [80386 21](#)

CALL Call procedure, introduced with [8086](#), extended with [80386 9, 21](#)

CBW Convert byte to word, introduced with [8086 7](#)

CDQ Convert double-word to quad-word, introduced with [80386 21](#)

CLC Clear carry flag, introduced with [8086 9](#)

CLD Clear direction flag, introduced with [8086 9](#)

CLI Clear interrupt flag, introduced with [8086 9](#)

CLTS Clear task-switched flag in CR0, introduced with [80286 17](#)

CMC Complement carry flag, introduced with [8086 9](#)

CMPS Compare string operands, introduced with [8086](#), extended with [80386 9, 21](#)

CMPXCHG8B Compare and exchange bytes, introduced with [CX8 31](#)

CMPXCHG Compare and exchange, introduced with [80486 25](#)

CMP Compare two operands, introduced with [8086](#), extended with [80386 9, 21](#)

CPUID CPU identification, introduced with [80486 5, 29](#)

CWDE Convert word to double-word, introduced with [80386 21](#)

CWD Convert word to doubleword, introduced with [8086 7](#)

DAA Decimal adjust AL after addition, introduced with [8086 7](#)

DAS Decimal adjust AL after subtraction, introduced with [8086 8](#)

DEC Decrement by 1, introduced with [8086](#), extended with [80386 8, 21](#)

DIV Unsigned divide, introduced with [8086](#), extended with [80386 8, 21](#)

EMMS Empty MMX technology state, introduced with [MMX 39](#)

ENTER Make stack frame for procedure parameters, introduced with [80186](#), extended with [80386 13, 21](#)

F2XM1 Computer $2^x - 1$, introduced with [8087 11](#)

FABS Absolute value, introduced with [8087 11](#)

FADDP Add and pop, introduced with [8087 11](#)

FADD Add, introduced with [8087 11](#)

FBLD Load [binary coded decimal \(BCD\)](#), introduced with [8087 11](#)

FBSTP Store [BCD](#) integer and pop, introduced with [8087 11](#)

FCHS Change sign, introduced with [8087 11](#)

FCLEX Clear exceptions, introduced with [8087 11](#)

FCOMPP Compare floating point values and pop twice, introduced with [8087 11](#)

FCOMP Compare floating point values and pop, introduced with [8087 11](#)

FCOM Compare floating point values, introduced with [8087 11](#)

FCOS Cosine, introduced with 80387 23

FDECSTP Decrement stack-top pointer, introduced with 8087 11

FDISI Disable interrupts, introduced with 8087, FNOP on other FPU's 11

FDIVP Divide and pop, introduced with 8087 11

FDIVRP Reverse divide and pop, introduced with 8087 11

FDIVR Reverse divide, introduced with 8087 11

FDIV Divide, introduced with 8087 11

FENI Enable interrupts, introduced with 8087, FNOP on other FPU's 11

FFREE Free floating-point register, introduced with 8087 11

FIADD Add integer, introduced with 8087 11

FICOMP Compare integer and pop, introduced with 8087 11

FICOM Compare integer, introduced with 8087 11

FIDIVR Reverse divide integer, introduced with 8087 11

FIDIV Divide integer, introduced with 8087 11

FILD Load integer, introduced with 8087 11

FIMUL Multiply integer, introduced with 8087 11

FINCSTP Increment stack-top pointer, introduced with 8087 11

FINIT Initialize floating point unit, introduced with 8087 11

FISTP Store integer and pop, introduced with 8087 11

FIST Store integer, introduced with 8087 11

FISUBR Reverse subtract integer, introduced with 8087 11

FISUB Subtract integer, introduced with 8087 11

FLD1 Load constant 1.0, introduced with 8087 12

FLDCW Load x87 FPU control word, introduced with 8087 12

FLDENV Load x87 FPU environment, introduced with 8087 12

FLDL2E Load constant $\log_2(e)$, introduced with 8087 12

FLDL2T Load constant $\log_2(10)$, introduced with 8087 12

FLDLG2 Load constant $\log_2(2)$, introduced with 8087 12

FLDLN2 Load constant $\ln(2)$, introduced with 8087 12

FLDPI Load constant π , introduced with 8087 12

FLDZ Load constant 0.0, introduced with 8087 12

FLD Load floating point value, introduced with 8087 11

FMULP Multiply and pop, introduced with 8087 12

FMUL Multiply, introduced with 8087 12

FNCLEX Clear exceptions, no wait, introduced with 8087 12

FNDISI Disable interrupts, no wait, introduced with 8087, **FNOP** on other FPU's 12

FNENI Enable interrupts, no wait, introduced with 8087, **FNOP** on other FPU's 12

FNINIT Initialize floating point unit, no wait, introduced with 8087 12

FNOP No operation, introduced with 8087 12, 53, 54

FNSAVE Save **x87 FPU** state, no wait, introduced with 8087, extended with 80387 12, 23

FNSTCW Store **x87 FPU** control word, no wait, introduced with 8087 12

FNSTENV Store **x87 FPU** environment, no wait, introduced with 8087, extended with 80387 12, 23

FNSTSW Store **x87 FPU** status word, no wait, introduced with 8087, extended with 80387 12, 23

FPATAN Partial arctangent, introduced with 8087 12

FPREM1 Partial remainder (IEEE), introduced with 80387 23

FPREM Partial remainder, introduced with 8087 12

FPTAN Partial tangent, introduced with 8087 12

FRNDINT Round to integer, introduced with 8087 12

FRSTOR Restore **x87 FPU** state, introduced with 8087, extended with 80387 12, 23

FSAVE Save **x87 FPU** state, introduced with 8087, extended with 80387 12, 23

FSCALE Scale, introduced with 8087 12

FSETPM Set protected mode, introduced with 80287, **FNOP** on other FPU's 19

FSINCOS Sine and cosine, introduced with 80387 23

FSIN Sine, introduced with 80387 23
 FSTCW Store x87 FPU control word, introduced with 8087 12
 FSTENV Store x87 FPU environment, introduced with 8087, extended with 80387 12, 23
 FSTP Store floating point value and pop, introduced with 8087 12
 FSTSW Store x87 FPU status word, introduced with 8087, extended with 80387 12, 23
 FST Store floating point value, introduced with 8087 12
 FSUBP Subtract and pop, introduced with 8087 12
 FSUBR Reverse subtract, introduced with 8087 12
 FSUB Subtract, introduced with 8087 12
 FTST Test, introduced with 8087 12
 FUCOMPP Unordered compare floating point values and pop twice, introduced with 80387 23
 FUCOMP Unordered compare floating point values and pop, introduced with 80387 23
 FUCOM Unordered compare floating point values, introduced with 80387 23
 FWAIT Wait (opcode synonym for WAIT), introduced with 8087 12
 FXAM Examine floating-point, introduced with 8087 12
 FXCH Exchange register contents, introduced with 8087 12
 FXTRACT Extract exponent and significand, introduced with 8087 12
 FYL2XP1 Compute $y * \log_2(x + 1)$, introduced with 8087 12
 FYL2X Compute $y * \log_2 x$, introduced with 8087 12
 HLT Halt, introduced with 8086 7
 IDIV Signed divide, introduced with 8086, extended with 80386 8, 21
 IMUL Signed multiply, introduced with 8086, extended with 80186, 80386 8, 13, 21
 INC Increment by 1, introduced with 8086, extended with 80386 8, 21
 INS Input from port to string, introduced with 80186, extended with 80386 13, 21
 INTO Call to interrupt procedure if overflow, introduced with 8086 9
 INT Call to interrupt procedure, introduced with 8086 9

INVD Invalidate internal caches, introduced with 80486 25

INVLPG Invalidate [translation lookaside buffer \(TLB\)](#) entries, introduced with 80486 25

IN Input from port, introduced with 8086, extended with 80386 9, 21

IRET Interrupt return, introduced with 8086, extended with 80386 9, 21

JMP Jump, introduced with 8086, extended with 80386 9, 21

Jcc Jump if condition is met, introduced with 8086, extended with 80386 9, 21

LAHF Load status flags into AH register, introduced with 8086 7

LAR Load access rights byte, introduced with 80286, extended with 80386 17, 21

LDS Load DS with far pointer, introduced with 8086 8

LEAVE High level procedure exit, introduced with 80186, extended with 80386 13, 22

LEA Load effective address, introduced with 8086, extended with 80386 8, 22

LES Load ES with far pointer, introduced with 8086 8

LFS Load FS with far pointer, introduced with 80386 21

LGDT Load global descriptor table register, introduced with 80286 17

LGS Load GS with far pointer, introduced with 80386 21

LIDT Load interrupt descriptor table register, introduced with 80286 17

LLDT Load local descriptor table register, introduced with 80286 17

LMSW Load machine status word, introduced with 80286 17

LOCK Assert LOCK# signal prefix, introduced with 8086 7

LODS Load string, introduced with 8086, extended with 80386 8, 22

LOOP/LOOPcc Loop according to (E/R)CX counter, introduced with 8086, extended with 80386 9, 22

LSL Load segment limit, introduced with 80286, extended with 80386 17, 22

LSS Load SS with far pointer, introduced with 80386 21

LTR Load task register, introduced with 80286 17

MOVD Move doubleword, introduced with [MMX](#) 39

MOVQ Move quadword, introduced with [MMX](#) 39

MOVSX Move with sign-extension, introduced with [80386 22](#)

MOVS Move data from string to string, introduced with [8086](#), extended with [80386 8, 22](#)

MOVZX Move with zero-extend, introduced with [80386 22](#)

MOV Move, introduced with [8086](#), extended with [80386 7, 8, 22](#)

MUL Unsigned multiply, introduced with [8086](#), extended with [80386 8, 22](#)

NEG Two's complement negation, introduced with [8086](#), extended with [80386 8, 22](#)

NOP No operation, introduced with [8086 7](#)

NOT One's complement negation, logical NOT, introduced with [8086](#), extended with [80386 8, 22](#)

OR Logical inclusive OR, introduced with [8086](#), extended with [80386 8, 22](#)

OUTS Output string to port, introduced with [80186](#), extended with [80386 13, 22](#)

OUT Output to port, introduced with [8086](#), extended with [80386 9, 22](#)

PACKSSDW Pack doublewords with signed saturation, introduced with [MMX 39](#)

PACKSSWB Pack words with signed saturation, introduced with [MMX 39](#)

PACKUSWB Pack words with unsigned saturation, introduced with [MMX 39](#)

PADDB Add packed byte integers, introduced with [MMX 39](#)

PADD Add packed doubleword integers, introduced with [MMX 39](#)

PADDQ Add packed quadword integers, introduced with [MMX 39](#)

PADDSB Add packed signed byte integers with signed saturation, introduced with [MMX 39](#)

PADDSW Add packed signed word integers with signed saturation, introduced with [MMX 39](#)

PADDUSB Add packed unsigned byte integers with unsigned saturation, introduced with [MMX 39](#)

PADDUSW Add packed unsigned word integers with unsigned saturation, introduced with [MMX 39](#)

PADDW Add packed word integers, introduced with [MMX 39](#)

PANDN Logical AND NOT, introduced with [MMX 39](#)

PAND Logical AND, introduced with [MMX 39](#)

PCMPEQB Compare packed bytes for equal, introduced with [MMX 39](#)

PCMPEQD Compare packed doublewords for equal, introduced with [MMX 39](#)

PCMPEQW Compare packed words for equal, introduced with [MMX 39](#)

PCMPGTB Compare packed signed bytes for greater than, introduced with [MMX 39](#)

PCMPGTD Compare packed signed doublewords for greater than, introduced with [MMX 39](#)

PCMPGTW Compare packed signed words for greater than, introduced with [MMX 39](#)

PDRAD Shift packed doublewords right arithmetic, introduced with [MMX 39](#)

PDRAQ Shift packed quadwords right arithmetic, introduced with [MMX 39](#)

PDRAW Shift packed words right arithmetic, introduced with [MMX 39](#)

PDRLD Shift packed doublewords right logical, introduced with [MMX 39](#)

PDRLQ Shift packed quadwords right logical, introduced with [MMX 39](#)

PDRLW Shift packed words right logical, introduced with [MMX 39](#)

PMADDWD Multiply and add packed integers, introduced with [MMX 39](#)

PMULHW Multiply packed signed integers and store high result, introduced with [MMX 39](#)

PMULLW Multiply packed signed integers and store low result, introduced with [MMX 39](#)

POPA Pop all general-purpose registers, introduced with [80186](#), extended with [80386 13, 22](#)

POPF Pop stack into FLAGS register, introduced with [8086](#), extended with [80386 9, 22](#)

POP Pop a value from the stack, introduced with [8086](#), extended with [80386 9, 22](#)

POR Bitwise logical OR, introduced with [MMX 39](#)

PSLLD Shift packed doublewords left logical, introduced with [MMX 39](#)

PSLLQ Shift packed quadwords left logical, introduced with [MMX 39](#)

PSLLW Shift packed words left logical, introduced with [MMX 39](#)

PSUBB Subtract packed byte integers, introduced with [MMX 40](#)

PSUBD Subtract packed doubleword integers, introduced with [MMX 40](#)

PSUBSB Subtract packed signed bytes with signed saturation, introduced with [MMX 40](#)

PSUBSW Subtract packed signed words with signed saturation, introduced with [MMX 40](#)

PSUBUSB Subtract packed unsigned bytes with unsigned saturation, introduced with [MMX 40](#)

PSUBUSW Subtract packed unsigned words with unsigned saturation, introduced with [MMX 40](#)

PSUBW Subtract packed word integers, introduced with [MMX 40](#)

PUNPCKHBW Unpack high bytes, introduced with [MMX 40](#)

PUNPCKHDQ Unpack high doublewords, introduced with [MMX 40](#)

PUNPCKHWD Unpack high words, introduced with [MMX 40](#)

PUNPCKLBW Unpack low bytes, introduced with [MMX 40](#)

PUNPCKLDQ Unpack low doublewords, introduced with [MMX 40](#)

PUNPCKLWD Unpack low words, introduced with [MMX 40](#)

PUSHA Push all general-purpose registers, introduced with [80186](#), extended with [80386 13, 22](#)

PUSHF Push FLAGS register onto the stack, introduced with [8086](#), extended with [80386 9, 22](#)

PUSH Push data onto the stack, introduced with [8086](#), extended with [80186, 80386 9, 13, 22](#)

PXOR Logical exclusive OR, introduced with [MMX 40](#)

RCL Rotate left through carry, introduced with [8086](#), extended with [80186, 80386 8, 13, 22](#)

RCR Rotate right through carry, introduced with [8086](#), extended with [80186, 80386 8, 13, 22](#)

RDMSR Read from model specific register, introduced with [MSR 33](#)

RDPMC Read performance-monitoring counters, introduced with [PMC 37](#)

RDTSR Read time-stamp counter, introduced with [TSC 35](#)

REPcc Repeat string operation prefix, introduced with [8086](#), extended with [80386 9, 22](#)

RET Return from procedure, introduced with [8086 9](#)

ROL Rotate left, introduced with [8086](#), extended with [80186, 80386 8, 13, 22](#)

ROR Rotate right, introduced with [8086](#), extended with [80186, 80386 8, 13, 22](#)

RSM Resume from system management mode, introduced with [RSM 27](#)

SAHF Store AH into flags, introduced with [8086 7](#)

SAL Shift arithmetically left, introduced with [8086](#), extended with [80186](#), [80386 8, 13, 22](#)

SAR Shift arithmetically right, introduced with [8086](#), extended with [80186](#), [80386 8, 13, 22](#)

SBB Integer subtraction with borrow, introduced with [8086](#), extended with [80386 8, 22](#)

SCAS Scan string, introduced with [8086](#), extended with [80386 8, 22](#)

SETcc Set byte on condition, introduced with [80386 22](#)

SGDT Store global descriptor table register, introduced with [80286](#), extended with [80386 17, 22](#)

SHLD Double precision shift left, introduced with [80386 22](#)

SHL Shift left, introduced with [8086](#), extended with [80186](#), [80386 8, 13, 22](#)

SHRD Double precision shift right, introduced with [80386 22](#)

SHR Shift right, introduced with [8086](#), extended with [80186](#), [80386 8, 13, 22](#)

SIDT Store interrupt descriptor table register, introduced with [80286](#), extended with [80386 17, 22](#)

SLDT Store local descriptor table register, introduced with [80286 17](#)

SMSW Store machine status word, introduced with [80286](#), extended with [80386 17, 22](#)

STC Set carry flag, introduced with [8086 9](#)

STD Set direction flag, introduced with [8086 9](#)

STI Set interrupt flag, introduced with [8086 9](#)

STOS Store string, introduced with [8086](#), extended with [80386 8, 22](#)

STR Store task register, introduced with [80286 17](#)

SUB Subtract, introduced with [8086](#), extended with [80386 8, 22](#)

TEST Logical compare, introduced with [8086](#), extended with [80386 9, 22](#)

VERR Verify a segment for reading, introduced with [80286 17](#)

VERW Verify a segment for writing, introduced with [80286 17](#)

WAIT Wait, introduced with [8086 7, 55](#)

WBINVD Write back and invalidate cache, introduced with [80486](#) 25

WRMSR Write to model specific register, introduced with [MSR](#) 33

XADD Exchange and add, introduced with [80486](#) 25

XCHG Exchange register/memory with register, introduced with [8086](#), extended with [80386](#) 7, 8, 22

XLAT Table look-up translation, introduced with [8086](#), extended with [80386](#) 8, 22

XOR Logical exclusive OR, introduced with [8086](#), extended with [80386](#) 8, 22

D Code Chunks

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