Introduction

The Digital Clock Manager (DCM) primitive in Xilinx FPGA parts is used to implement delay locked loop, digital frequency synthesizer, digital phase shifter, or a digital spread spectrum. The digital clock manager module is a wrapper around the DCM primitive which allows it to be used in the EDK tool suite.

For more information regarding DCM features, see the Users Guide of the various FPGA device families at http://support.xilinx.com.

Features

- Wrapper around the FPGA architecture DCM primitive; provides full support for use with the EDK design tools
- Supports both active high and active low reset
- Configurable BUFG insertion

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	Spartan®-3A/3A DSP, Spartan-3, Spartan-3E, Automotive Spartan 3/3E/3A/3A DSP, Virtex®-4 /4Q/4QV, Virtex-5/5fx/	
Version of Core	dcm_module	v1.00d
Resources Used		
	Min	Max
Slices	N/A	N/A
LUTs	0	1
FFs	3	3
Block RAMs	0	0
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 11.4 or later	
Verification	ModelSim PE/SE 6.4b or later	
Simulation	ModelSim PE/SE 6.4b or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Functional Description

The Digital Clock Manager (DCM) is shown in the block diagram in Figure 1.
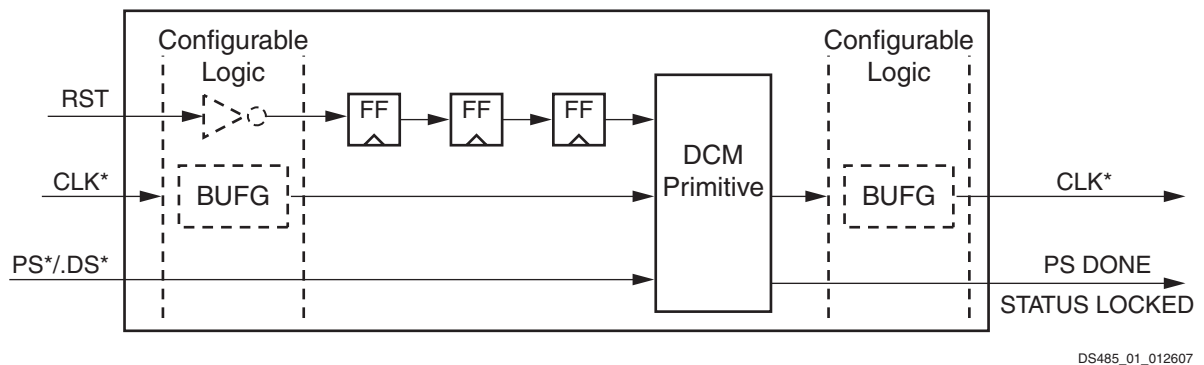

DS485_01_012607

Figure 1: **DCM Module Block Diagram**

DCM Module Parameters

The associated MPD (Microprocessor Peripheral Definition) file contains a list of the parameter of the peripheral that are fixed at FPGA configuration time. The parameters are described in Table 1.

Table 1: **MPD Parameters**

Parameter Name	Feature Description	Allowable Values	Default	Type
C_DFS_FREQUENCY_MODE	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	"LOW"	string
C_DLL_FREQUENCY_MODE	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	"LOW"	string
C_DUTY_CYCLE_CORRECTION	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	true	boolean
C_CLKIN_DIVIDE_BY_2	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	false	boolean
C_CLK_FEEDBACK	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	"1X"	string
C_CLKOUT_PHASE_SHIFT	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	"NONE"	string
C_DSS_MODE	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	"NONE"	string
C_STARTUP_WAIT	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	false	boolean
C_PHASE_SHIFT	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	0	integer
C_CLKFX_MULTIPLY	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	4	integer
C_CLKFX_DIVIDE	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	1	integer

www.xilinx.com

Table 1: **MPD Parameters** *(Cont'd)*

Parameter Name	Feature Description	Allowable Values	Default	Type
C_CLKDV_DIVIDE	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	2.0	real
C_CLKIN_PERIOD	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	41.66666	real
C_DESKEW_ADJUST	This parameter passes the value to the equivalent attribute of DCM.	Same as primitive	"SYSTEM_SYNCHRONOUS"	string
C_CLKIN_BUF	If C_CLKIN_BUF is true, a BUFG is inserted; otherwise, CLKIN signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLKFB_BUF	If C_CLKFB_BUF is true, a BUFG is inserted; otherwise, CLKFB signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLK0_BUF	If C_CLK0_BUF is true, a BUFG is inserted; otherwise, CLK0 signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLK90_BUF	If C_CLK90_BUF is true, a BUFG is inserted; otherwise, CLK90 signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLK180_BUF	If C_CLK180_BUF is true, a BUFG is inserted; otherwise, CLK180 signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLK270_BUF	If C_CLK270_BUF is true, a BUFG is inserted; otherwise, CLK270 signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLKDV_BUF	If C_CLKDV_BUF is true, a BUFG is inserted; otherwise, CLKDV signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLK2X_BUF	If C_CLK2X_BUF is true, a BUFG is inserted; otherwise, CLK2X signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLK2X180_BUF	If C_CLK2X180_BUF is true, a BUFG is inserted; otherwise, CLK2X180 signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_CLKFX_BUF	If C_CLKFX_BUF is true, a BUFG is inserted; otherwise, CLKFX signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean

Parameter Name	Feature Description	Allowable Values	Default	Type
C_CLKFX180_BUF	If C_CLKFX180_BUF is true, a BUFG is inserted; otherwise, CLKFX180 signal is connected to the equivalent pin of DCM directly.	True, False	false	boolean
C_EXT_RESET_HIGH	If C_EXT_RESET_HIGH = 0, an inverter is inserted for RST pin of DCM; otherwise, this RST is connected to the equivalent pin of DCM directly.	0, 1	1	integer
C_FAMILY	Target architecture family for design	spartan3, spartan3e, spartan3a, spartan3adsp, aspartan3, aspartan3e, aspartan3a, aspartan3adsp, virtex4, qvirtex4, qvvirtex4, virtex5, virtex5fx		string

Allowable Parameter Combinations

There are no restrictions on parameter combinations beyond those defined for the DCM primitive in the target FPGA architecture. Please refer to the user guide for the particular FPGA architecture.

DCM Module I/O Signals

The DCM Module I/O signals are listed and described in Table 2.

Table 2: Summary of DCM Module I/O

Signal	I/O	Initial State	Description
RST	I		If C_EXT_RESET_HIGH = 0, an inverter is inserted. Then three DFFs are inserted before this signal is connected to the equivalent pin of DCM.
CLKIN	I		If C_CLKIN_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLKFB	I		If C_CLKFB_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly
PSEN	I		Connect to the equivalent pin of DCM directly.
PSINCDEC	I		Connect to the equivalent pin of DCM directly.
PSCLK	I		Connect to the equivalent pin of DCM directly.
DSSEN	I		Connect to the equivalent pin of DCM directly.
CLK0	O	Same as primitive	If C_CLKIN_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.

www.xilinx.com

Table 2: **Summary of DCM Module I/O** *(Cont'd)*

Signal	I/O	Initial State	Description
CLK90	O	Same as primitive	If C_CLK90_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLK180	O	Same as primitive	If C_CLK180_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLK270	O	Same as primitive	If C_CLK270_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLKDV	O	Same as primitive	If C_CLKDV_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLK2X	O	Same as primitive	If C_CLKFX_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLK2X180	O	Same as primitive	If C_CLK2X180_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLKFX	O	Same as primitive	If C_CLKFX_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
CLKFX180	O	Same as primitive	If C_CLKFX180_BUF = true, a BUFG is inserted; otherwise, this signal is connected to the equivalent pin of DCM directly.
STATUS	O	Same as primitive	Connect to the equivalent pin of DCM directly.
LOCKED	O	Same as primitive	Connect to the equivalent pin of DCM directly.
PSDONE	O	Same as primitive	Connect to the equivalent pin of DCM directly.

DCM Module Register Descriptions

Not Applicable.

DCM Module Interrupt Descriptions

Not Applicable.

Design Implementation

Design Tools

The DCM Module design is hand written.

To see the synthesis tool used for this device, go to the Synthesis field of the LogiCORE Facts table. The EDIF netlist output from XST is then input to the Xilinx Alliance tool suite for actual device implementation.

Target Technology

The target technology is an FPGA listed in the Supported Device Family field of the LogiCORE IP Facts table.

Device Utilization and Performance Benchmarks

The device utilization depends on DCM and BUFG primitive resources of the targeted device. See the respective FPGA family user guide for details on DCM and BUFG primitive performance and available resources.

Specification Exceptions

Not applicable.

Reference Documents

None.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/28/03	1.0	Revision History added to document.
12/19/03	1.1	Added LogiCORE Facts table. Reformatted to current Xilinx template.
08/03/04	1.2	Corrected device utilization and architecture support. Removed old references to embedded tools. Corrected list of parameters. Corrected template
8/13/04	1.2.1	Updated for EDK 6.3. Reviewed and corrected trademark usage.
9/29/04	1.3	Corrected statement on when inverter is inserted based on C_EXT_RESET_HIGH parameter
4/2/05	1.4	Updated for EDK 7.1.1 SP1; updated supported device family listing.
7/18/05	1.5	Converted to new DS template.
12/2/05	1.6	Added Spartan®-3E to supported device families listing.
1/26/07	1.7	Added three DDFs to RST input in Figure 1. Added 2.5 as allowed value for C_CLKDV_DIVIDE parameter in MPD (Table 1).
11/4/07	1.8	Always set parameter FACTORY_JF to 0xF0F0 for Virtex®-4 and Virtex-5.
4/24/09	1.9	Replaced references to supported device families and tool name(s) with hyperlink to PDF file; converted to current DS template.
12/2/09	1.10	Updated for EDK 11.4 release.

www.xilinx.com

Notice of Disclaimer

Xilinx is providing this design, code, or information (collectively, the "Information") to you "**AS-IS**" with no warranty of any kind, express or implied. Xilinx makes no representation that the Information, or any particular implementation thereof, is free from any claims of infringement. You are responsible for obtaining any rights you may require for any implementation based on the Information. All specifications are subject to change without notice. XILINX EXPRESSLY DISCLAIMS ANY WARRANTY WHATSOEVER WITH RESPECT TO THE ADEQUACY OF THE INFORMATION OR ANY IMPLEMENTATION BASED THEREON, INCLUDING BUT NOT LIMITED TO ANY WARRANTIES OR REPRESENTATIONS THAT THIS IMPLEMENTATION IS FREE FROM CLAIMS OF INFRINGEMENT AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Except as stated herein, none of the Information may be copied, reproduced, distributed, republished, downloaded, displayed, posted, or transmitted in any form or by any means including, but not limited to, electronic, mechanical, photocopying, recording, or otherwise, without the prior written consent of Xilinx.