Digital Average Current Mode CCM Buck Control-to-Output Model

Introduction

Digital controllers are currently popular for use in various converter applications for design flexibility and also its capability to perform multiple functions in one chip on top of the controller regulation function, such as advanced protection, and also communication with other systems. Digital controllers have a few disadvantages such as, limited resolution (quantization error) of the ADC and PWM and also greater controller delay compared to analog controllers due to the inherent discrete time sampling nature of it. In this study, synchronous rectifier buck (SR-Buck) is used with average current mode control (ACMC). This control structure is highly suitable for implementation with digital controllers as it has highly suppressed LC resonance similar to peak current mode control (PCMC), while also compatible with the PWM module characteristic of the digital controller. Additionally, ACMC also allows for accurate average current regulation.

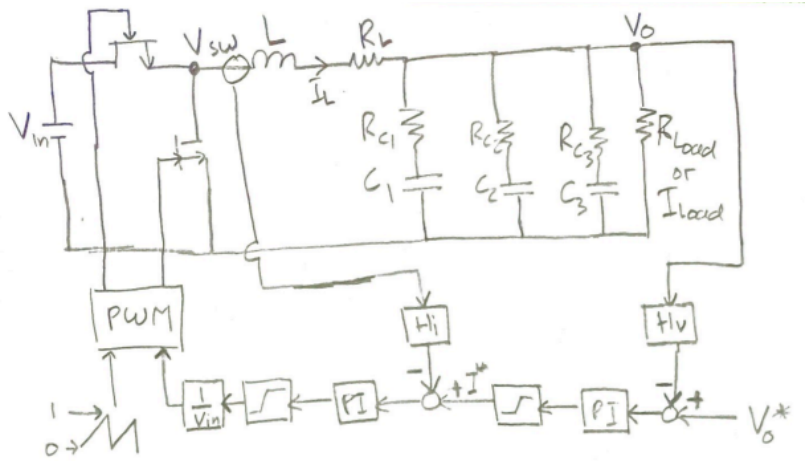
The focus of this paper are:

- Overall system modeling in a general controller block diagram approach
- Addressing the current feedback measurement issue,
- Modeling of the system delays
- Controller design using the presented model (inner I and outer V loop)
- Verification of the model performance using FRA approach

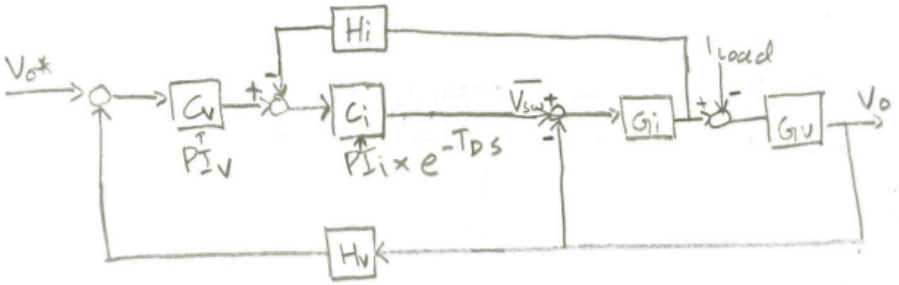
Overall buck converter model

Fig. 1 shows the overall schematic with the converter, controller, and the feedback circuits. The system is then simplified into control block diagrams as depicted in Fig. 2. In the system model, the PWM and half bridge switch are represented avg(Vsw) which is the average voltage of the Vsw node within one switching period.

→ Fig. 1. Overall system schematic



→ Fig. 2. Overall equivalent system block diagram of the CCM Buck converter



$$\overline{V_{sw}} = D * V_{in}$$

The converter passives are modeled as Gi and Gv for the “current model” and “voltage model”. The current model is used to represent the inductor behavior with inductor voltage ($V_L = \overline{V_{sw}} - V_o$) as the input and inductor current as the output. The output voltage model is then fed by the inductor current to regulate the output voltage. Inductor current and output voltage measurement circuit characteristics are represented as Hi and Hv respectively which can be simplified as a first order plus time delay (FOPTD) model as shown in Eq. XX and Eq. XX. Finally, the open loop transfer function can be written as Eq. XX.

$H_i(s) = \exp(-sT_{d,i})/(s/\omega_{bw,i} + 1)$

$H_v(s) = \exp(-sT_{d,v})/(s/\omega_{bw,v} + 1)$

$G_i(s) = 1/(sL + R_L)$

Model with I_{load}

=> $G_v(s) = (sRc_1C_1 + 1)/sC_1 \ // \ (sRc_2C_2 + 1)/sC_2 \ // \ (sRc_3C_3 + 1)/sC_3$

Model with R_{load}

=> $G_v(s) = (sRc_1C_1 + 1)/sC_1 \ // \ (sRc_2C_2 + 1)/sC_2 \ // \ (sRc_3C_3 + 1)/sC_3 \ // \ R_{load}$

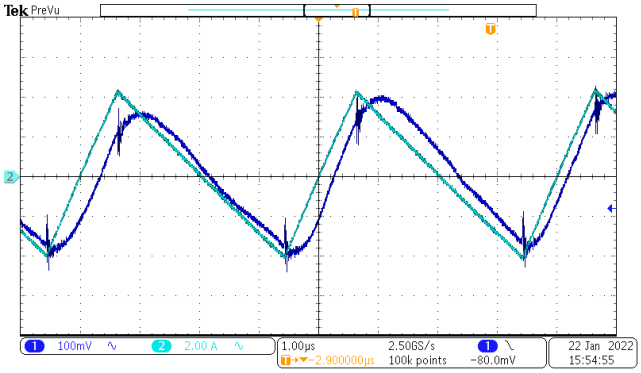
$Open\_Loop\_TF = C_v(s)C_i(s)G_i(s)G_v(s)H_v(s)/(1 + C_i(s)G_i(s)H_i(s) + G_i(s)G_v(s))$

Inductor average current measurement and system delays

It is common for digital controllers to use triangular PWM carrier waveforms and perform the measurement sampling once for each PWM period at the PWM = 0 or PWM = PEAK to avoid switching noise from corrupting the measurement. Unfortunately, in high switching frequency (>50kHz), the sensor delay is going to be quite significant and it skews the measurement timing, causing significant error to the measurement result. Furthermore, the triangular shape (non-linear with discontinuity) of the current waveform is also difficult for the shunt amplifier to closely track the actual current waveform precisely.

Shunt resistor with 1mΩ resistance and current shunt amplifier INA180A2 with 210kHz bandwidth and 50x gain were used for inductor current sensing. Fig. 3 shows the measurement waveform from the shunt amplifier output compared to the high bandwidth scope probe(Tektronix TCP0020, >50MHz 20A.rms) at steady-state. Despite very stable current measurement by scope probe , the shunt amplifier output shows some inconsistent distortion. Thus, the standard single measurement sampling per period will result in poor controller performance.

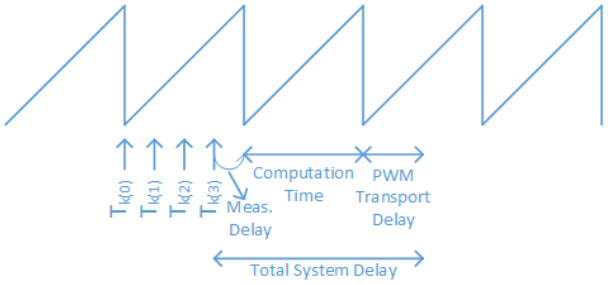
→ Fig. 3. Measured current shunt amplifier compared to high bandwidth scope probe



In this paper, sawtooth PWM carrier was used due to the limitation on HRPWM implementation in the MCU. Average current is measured by taking the average of **four samples** obtained at Tk(0), Tk(1), Tk(2), and Tk(3) within one PWM period as shown in Fig. 4. Using this method, accurate average measurement and improved noise robustness were obtained.

The delay introduced by the controller needs to be accurately accounted for, as it causes phase erosion to the control loop frequency response. Where it can be detrimental to the system stability and transient performance. The system delays consisted mainly of measurement delay, computation delay, and PWM transport delay. The total delay can be obtained using Eq. XX.

→ Fig. 4. Timing arrangement and delays on the digitally controlled converter



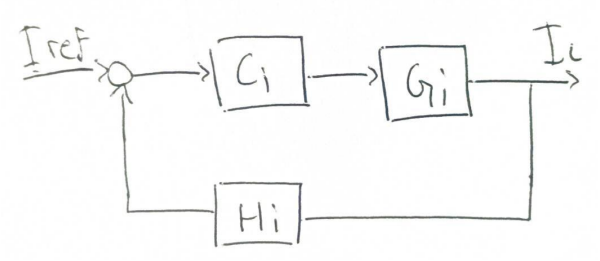
$T_{d,sys}$ = meas delay + computation time delay + PWM transport delay

$T_{d,sys}$ = 0.25Tsw + Tsw + 0.5Tsw = 1.75Tsw

Controller design

In ACMC control structure, two controllers are used simultaneously, the inner current loop controller and outer voltage loop controller. The inner loop controller is designed using the simplified control system loop as shown in Fig. 5. In this paper, PI controller is used and the controller constant can be calculated using Eq. XX through Eq. XX.

→ Fig. 5. Simplified inner current loop model



$C_i(s) = (sK_{pi} + K_{ii})/s$

$C_i(s) = K_{pi}(s + Z_i)/s$; $K_{ii} = K_{pi}*Z_i$

$Z_i = 180 - \phi_{Mi} - \arg[\exp(-j\omega*Td)/(j\omega)*G_i(j\omega)*H_i(j\omega)]$

$K_{pi} = 1/\text{mag}[\exp(-j\omega*T_{d,sys})*(j\omega + Z_i)/(j\omega)*Gi(j\omega)*Hi(j\omega)]$

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$C_v(s) = (sK_{pv} + K_{iv})/s$

$C_v(s) = K_{pv}(s + Z_v)/s$; $K_{iv} = K_{pv}*Z_v$

$Z_v = 180 - \phi_{Mv} - \arg[1/(j\omega)*C_i(j\omega)*G_i(j\omega)*G_v(j\omega)*H_v(j\omega)/(1 + C_i(j\omega)G_i(j\omega)H_i(j\omega) + G_i(j\omega)G_v(j\omega))]$

$K_{pv} = 1/\text{mag}[(j\omega + Z_v)/(j\omega)*C_i(j\omega)G_i(j\omega)G_v(j\omega)H_v(j\omega)/(1 + C_i(j\omega)G_i(j\omega)H_i(j\omega) + G_i(j\omega)G_v(j\omega))]$

As a rule of thumb, (1) phase margin >40deg is generally recommended for both inner and outer loop, and (2) the crossover frequency of the inner loop can be placed at Fsw/20 and cross over frequency of the outer loop can be placed at <=20% the inner loop crossover frequency. The inner loop cross over frequency is relatively lower than the one using analog controllers, due to the phase erosion caused by the sampling and computation delays which then limits the crossover frequency to attain a reasonable phase margin. The overall converter parameter is depicted in table 1.

→ Table 1. Converter parameter

Parameters	Value
Inductor	4.7uH
Output Electrolytic Capacitor	220uF, ESR 0.18Ω
Output Ceramic Cap (2 Parallel)	10uF X7R (7uF @ 14V), ESR 2.5mΩ
MOSFET	PANJIT PSMQC038 N10LS2 (100V, 3.8mOhm)
Fswitching // Fsampling	250 kHz // 250 kHz
Vin	48V
Vout	14V
Kpi, Kii	0.44164 and 7697
Kpv, Kiv	1.39213 and 40575

Bode plot of the analytical model compared to simulation and experimental measurement

Experimental measurement was obtained using DIY software FRA library implemented in the DSP. The software FRA algorithm extracts the frequency response from 1 second long measurement, and to ensure the converter is in steady-state, 0.5 second dwelling time is added prior to Fourier computation.

The FRA measurement can be implemented with two approaches, mixer based analog signal processing combined with high bit-rate low sampling rate ADC, or using high sampling rate ADC with the digital signal processing. The former has the advantage of high dynamic range but it requires a specific analog signal processing. The latter has limited dynamic range, however it does not require any additional circuitry for this measurement. Thus making the latter to be suitable for implementation in MCU.

$Ay(\omega) = 1/(\pi T) * \text{Integral } [y \cos(\omega t)]\, dt, \quad \text{from 0 to T}$
$By(\omega) = 1/(\pi T) * \text{Integral } [y \sin(\omega t)]\, dt, \quad \text{from 0 to T}$
$Ax(\omega) = 1/(\pi T) * \text{Integral } [x \cos(\omega t)]\, dt, \quad \text{from 0 to T}$
$Bx(\omega) = 1/(\pi T) * \text{Integral } [x \sin(\omega t)]\, dt, \quad \text{from 0 to T}$

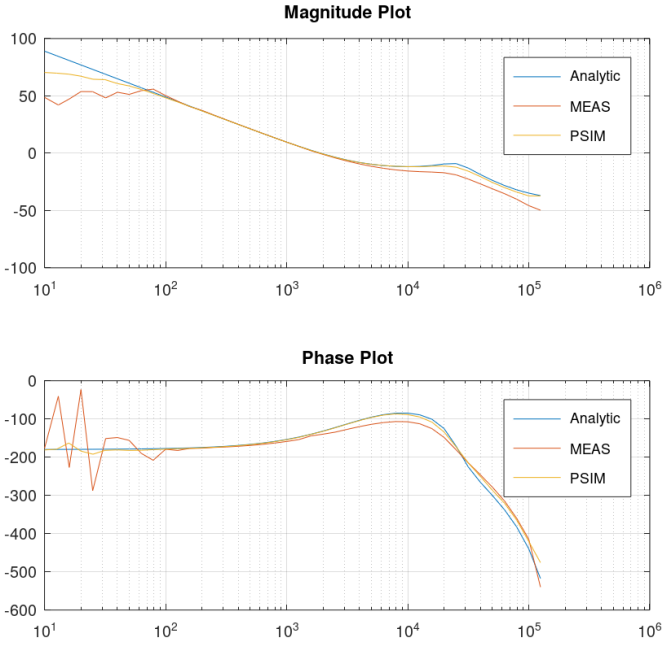
The FRA is designed based on the Fourier series as shown in Eq. XX. In the discrete time implementation, the integral is changed into a sigma operator. Due to the ratiometric nature of the mag and phase formula, the constant multiplier of $(1/\pi T)$ and dt can be removed. Thus, the discrete algorithm implementation can be described as Eq. XX. The gain and phase of the system can be obtained by Eq. XX after the integration(summing) period ended.

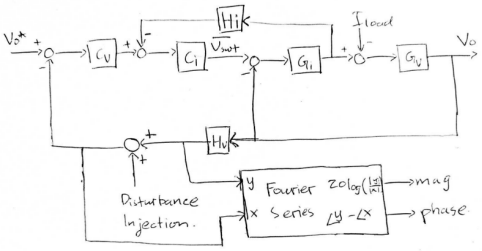
$Ay(\omega) = \text{Sigma } [y \cos(\omega k)], \quad \text{from k = 0 to k = 1s}$
$By(\omega) = \text{Sigma } [y \sin(\omega k)], \quad \text{from k = 0 to k = 1s}$
$Ax(\omega) = \text{Sigma } [x \cos(\omega k)], \quad \text{from k = 0 to k = 1s}$
$Bx(\omega) = \text{Sigma } [x \sin(\omega k)], \quad \text{from k = 0 to k = 1s}$

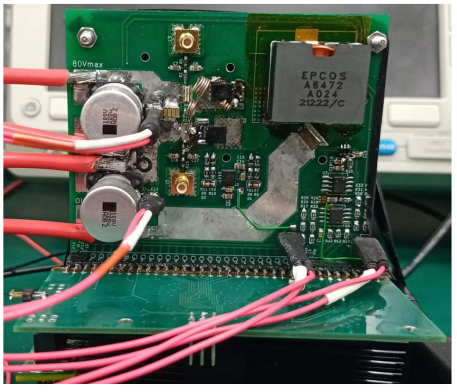
$GAIN = 20*\log10[\sqrt{((Ay^2+By^2)/(Ax^2+Bx^2))}]$
$PHASE = \arctan2(By/Ay) - \arctan2(Bx/Ax)$

The dynamic range of this method can be approximated by Eq. below. Since four samples per switching period were also performed on the voltage measurement, the effective bit-rate of this method also increased to four times (4x4096).

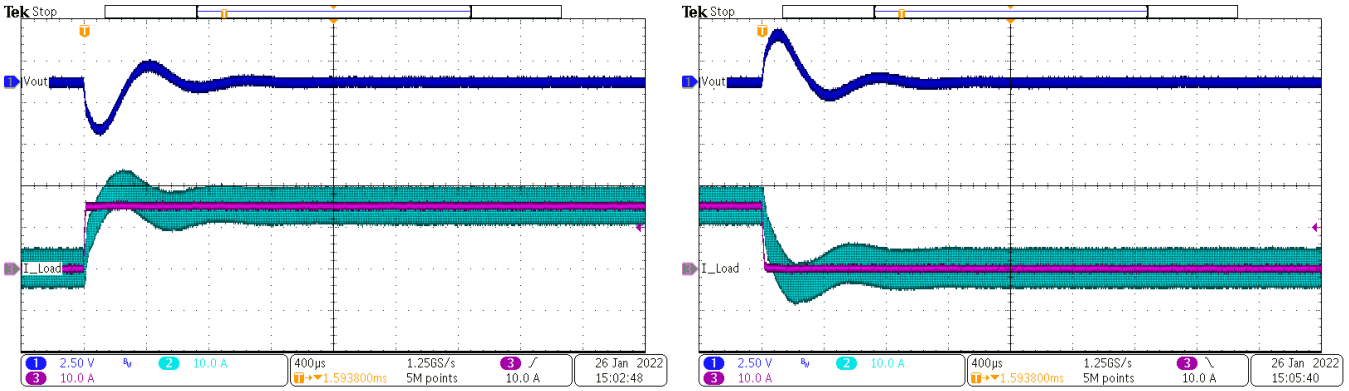
dynamic range (dB) = ± 20*log10[injection level (peak-peak) / DC measurement range * bitrate]
dynamic range (dB) = ± 20*log10[2/ 100 * 4 * 4096] ≅ ± 50.1 dB







Time domain waveform result



Reference/Good to read

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