Deciphering LLC charge mode controller implementation (NCP4390) and mixed-mode modelling using Qspice

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https://github.com/physicboy/QSPICE

Disclaimer

I am working for FSP-Technology and not affiliated to Onsemi or Qspice/Qorvo.

NCP4390 is a charge mode controller IC developed and manufactured by Onsemi. Currently, this IC is used in one of our design, and this presentation only presents the method I used to understand and built model of the IC in simulation.

Qspice is a Spice variants developed by Mike Engelhardt and teams at Marcus Aurelius Software LLC solely for Qorvo. This software is freely available from Qorvo website.

Materials presented contain no confidential information that belong to my past and current employer.

Introduction

- Direct frequency modulation vs Charge mode control
  - Direct frequency modulation (L6599 or UCC25600)
  - Charge mode control (NCP4390, UCC25660, UCC2564xx, HR1211, TEA9026, TEA2016/7)
- The need for modelling and simulation
  - Prototyping and hardware testing are time and cost intensive
  - Simulation helps to get closer to desirable result faster and cheaper
  - How to create a moderate complexity yet accurate IC model for simulation?
- What and why Qspice?
  - Free
  - Support C and Verilog modeling
  - Crazy fast

NCP4390 General Overview

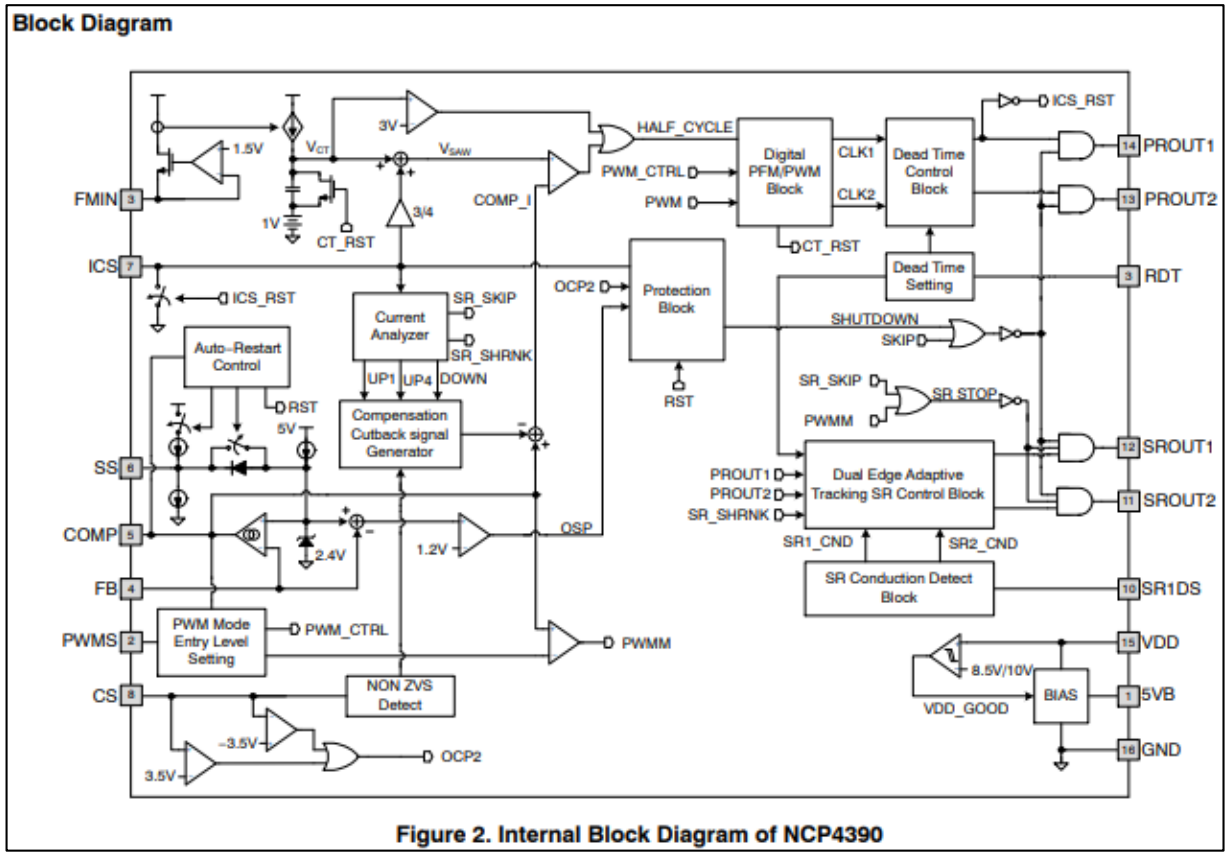


Figure 2. Internal Block Diagram of NCP4390

Note:

NCP4390 is implemented in mixed-mode fashion. Compensation, soft start, slope compensation, and charge mode control is implemented using analog comparator/OPA/OTA

The rest of the circuits is implemented using digital approach.

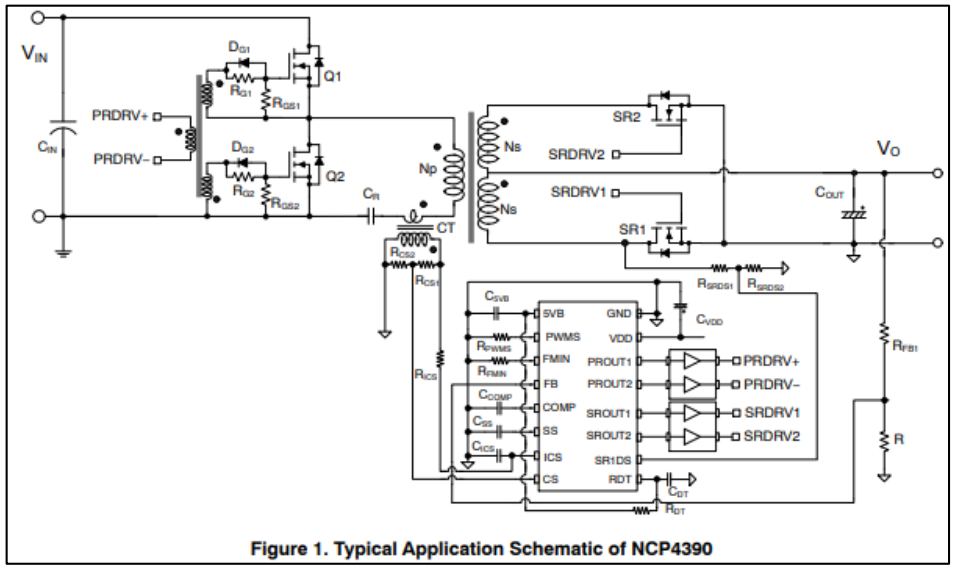
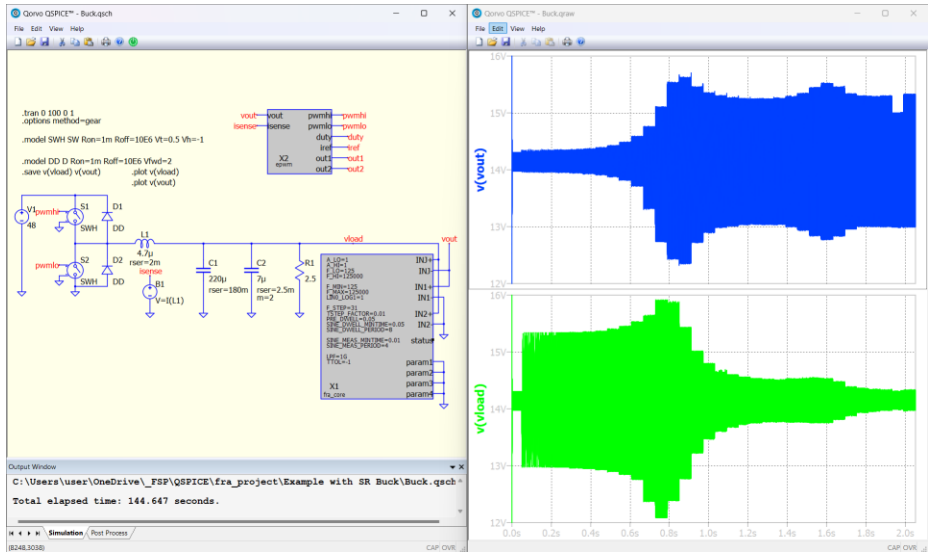
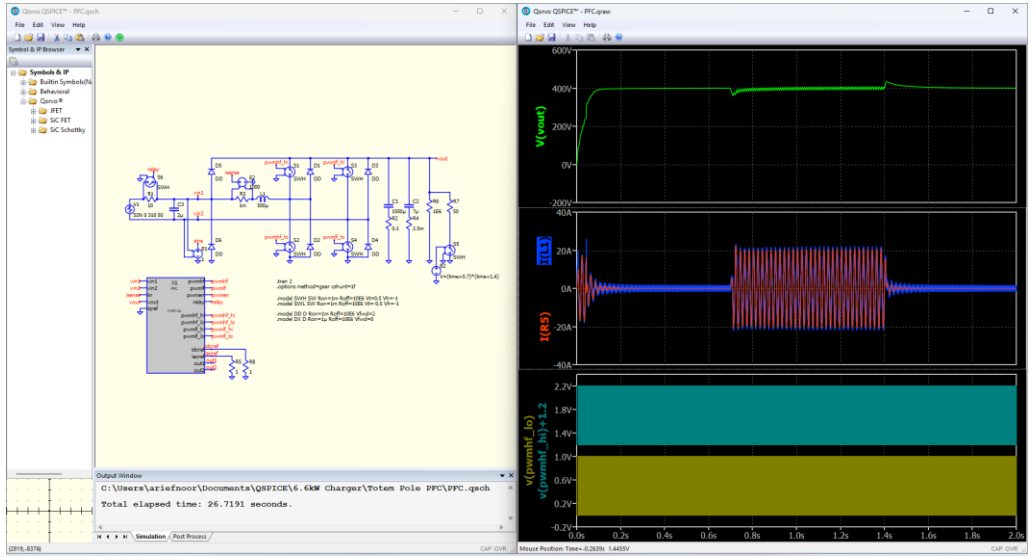


Figure 1. Typical Application Schematic of NCP4390

Hey Qspice!

Developed by Mike Engelhardt
For Qorvo





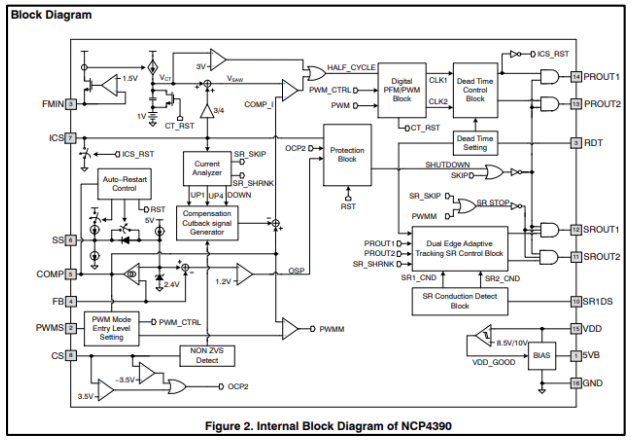
Primary features:

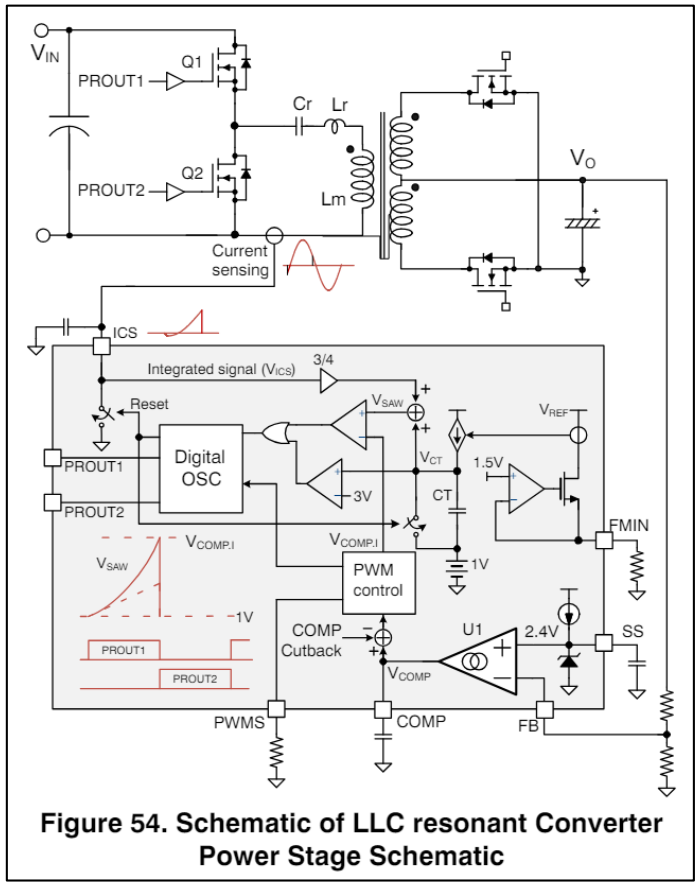
1. Free
2. The only spice with native ideal switch model
3. Native capability for instant discontinuity handling
4. Mixed mode simulation with C-block or Verilog support
5. Natively fast
6. Insanely fast, with C block timing control

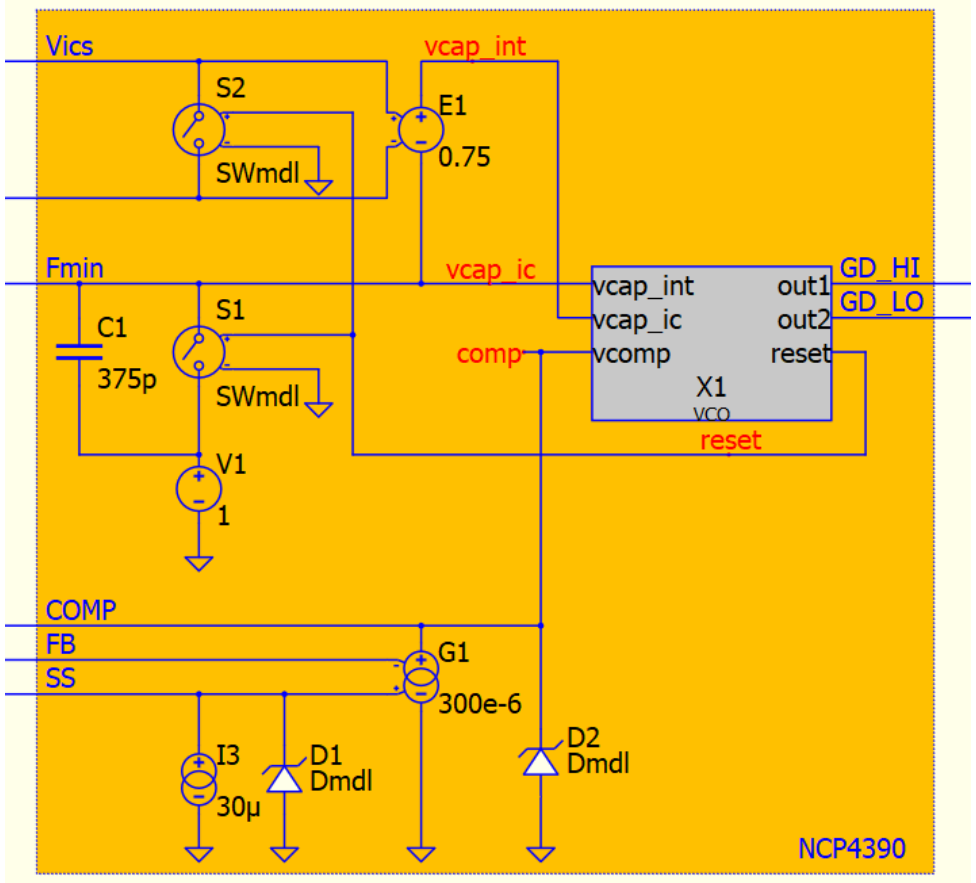
Modelling Approach

- Be clear about the goal: Controller performance evaluation
- Identify the critical IC functions towards the modelling goal:
  - Compensator,
  - Soft start,
  - Charge mode control implementation,
  - Voltage controlled oscillator,
  - Burst mode,
  - Not required: advanced protection, low power operation mode, SR controller,
- Start simple
- Evaluate each functions independently
- Combine all functions and test.

Controller Overall







https://github.com/physicboy/QSPICE/tree/main/NCP4390%20-%20VPEC

Compensation and Soft Start

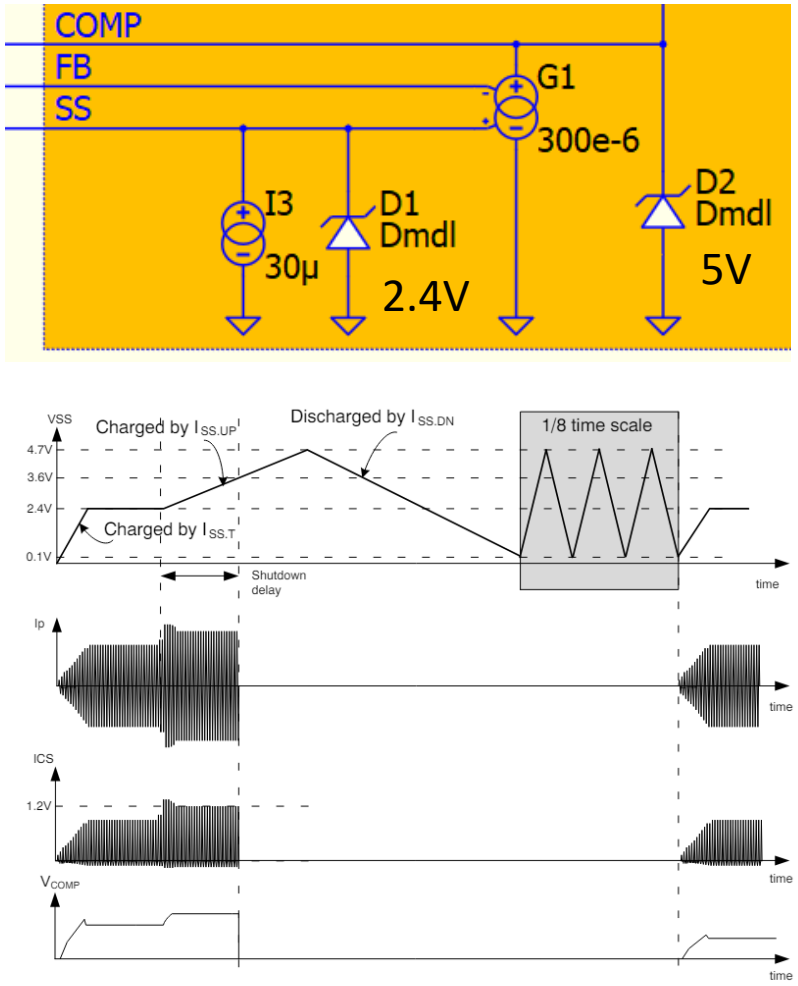


Figure 70. Auto Re−Start after Protection is Triggered

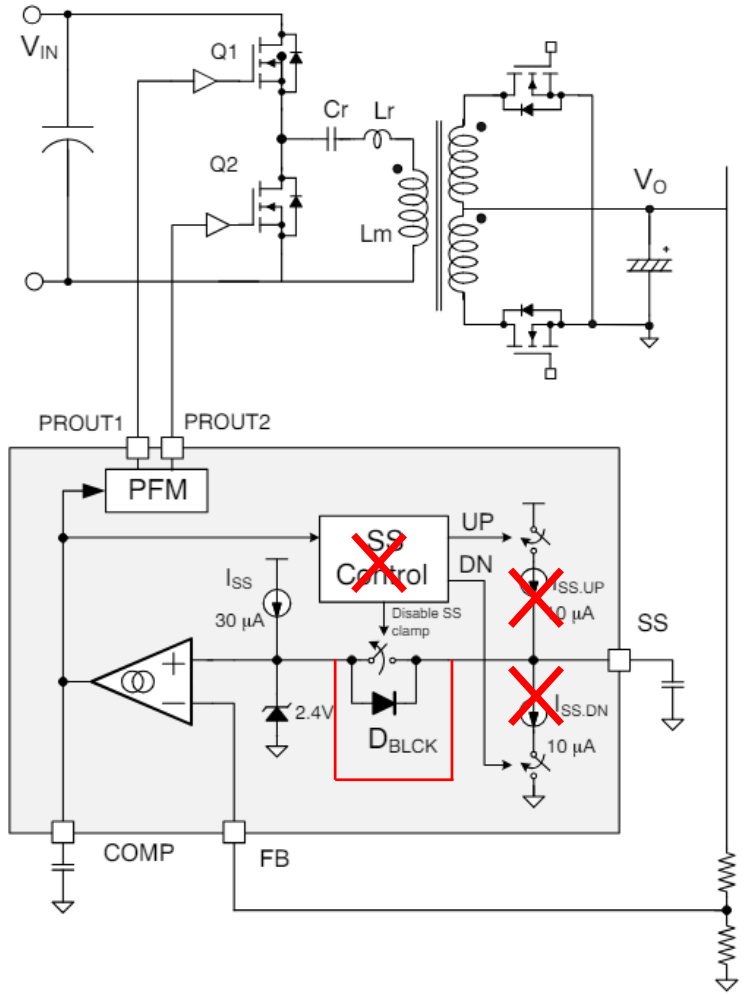


Figure 68. Schematic of Closed Loop Soft−Start

Charge Mode Controller Implementation

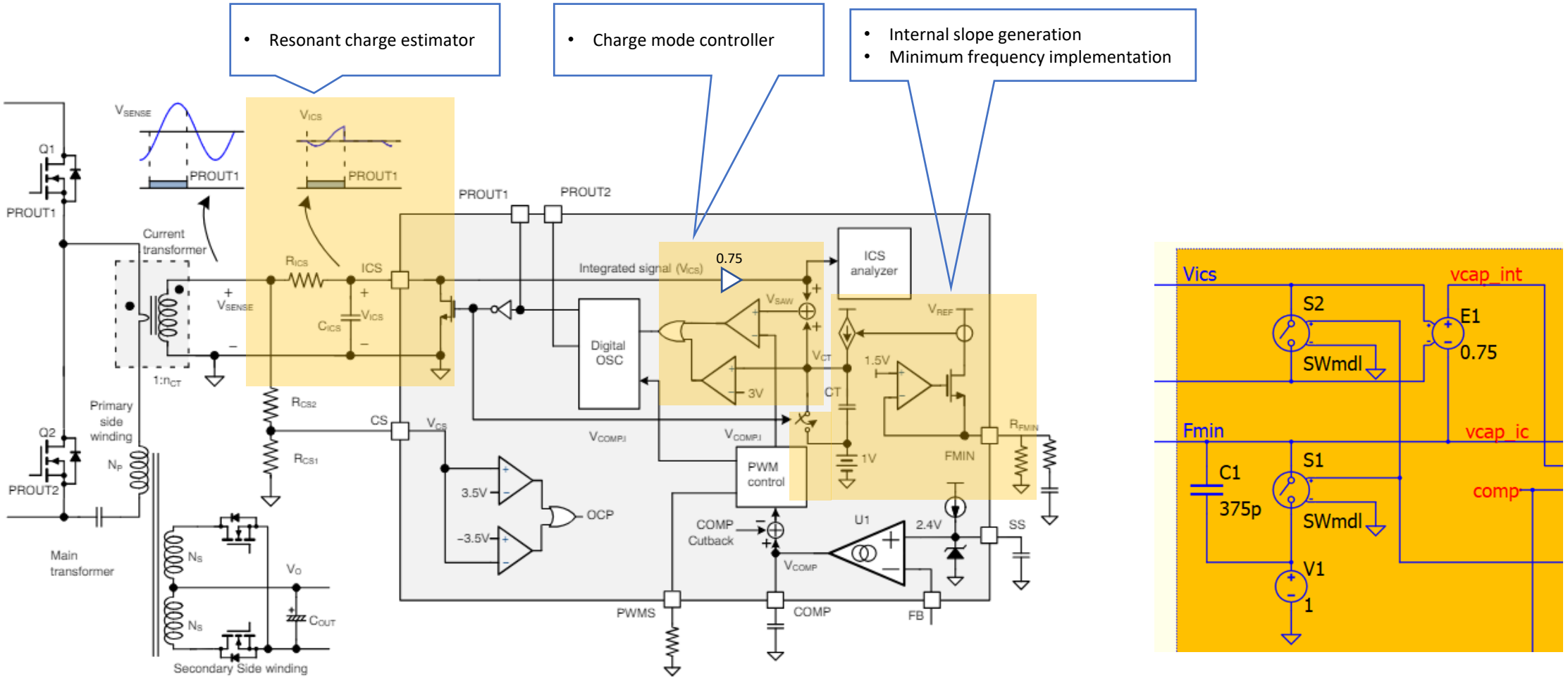
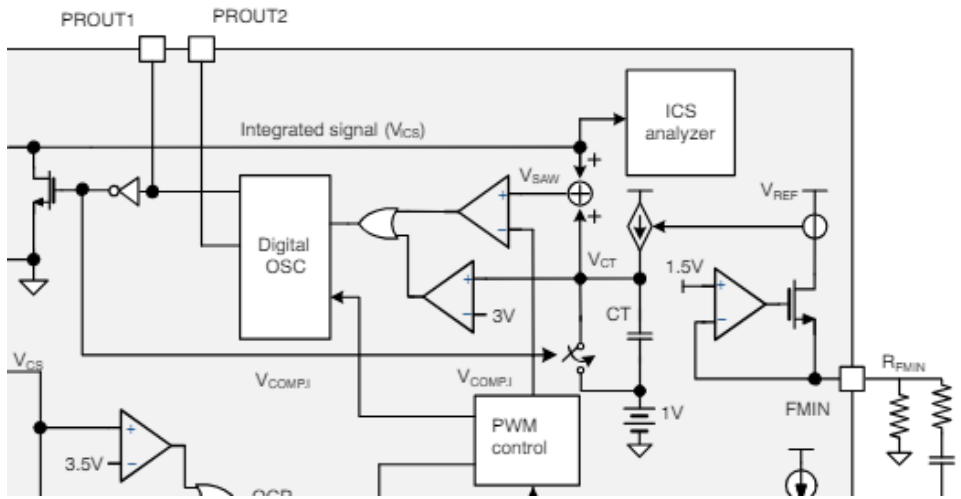


Figure 83. Basic Application Circuit for Current Sensing and Soft−Start

VCO and Burst-mode Implementation

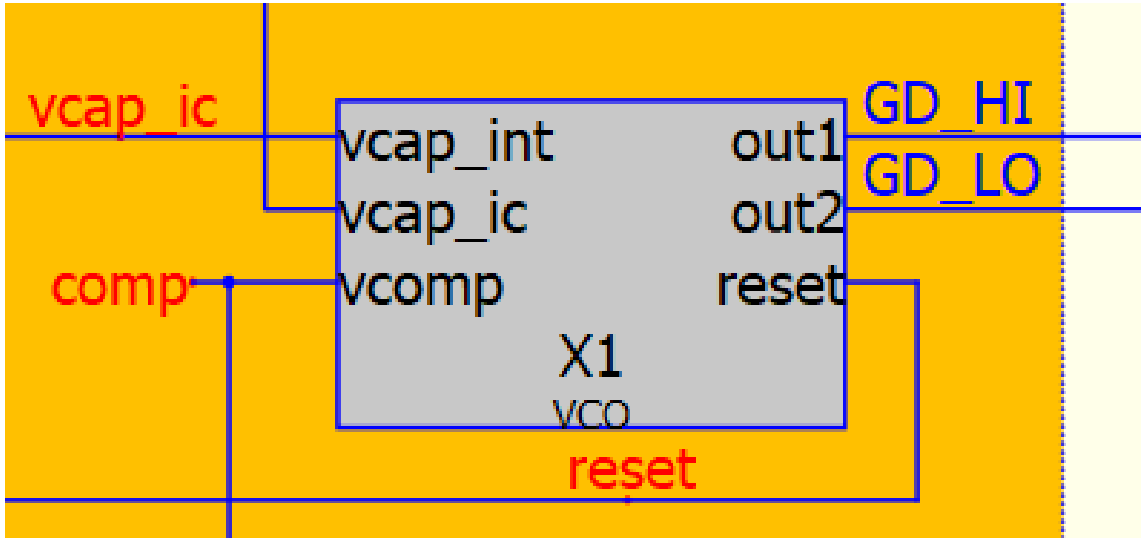
Initial information from datasheet face value:

1. it sense the internal slope to force minimum switching frequency by comparing with 3V
2. it measure the Vcomp
3. it senses the sum of charge and internal slope and compare it with Vcomp to turn off the Main power switch
4. Vcomp < 1.25V enter skip cycle (burst mode) Vcomp > 1.3V normal operation



Some of the deduced information:

1. VCO is digital asic with 40MHz clock
2. Output PWM signal is sync'd to 40MHz clock
3. Charge mode operation occurs only on half of the switching period (when upper MOSFET is on.
4. The lower MOSFET on-duration is mirror of the upper MOSFET. Implemented using up-down counter.
5. reset signal is generated based as an exact inverse of upper MOSFET signal. When device enter burst mode, reset signal is held active.
6. Deadtime setting is directly taken from datasheet



Dead-time Implementation

Table 1. DEAD TIME SETTING FOR PROUT AND SROUT

	C_{DT} = 180 pF		C_{DT} = 220 pF		C_{DT} = 270pF		C_{DT} = 330 pF		C_{DT} = 390 pF		C_{DT} = 470 pF		C_{DT} = 560 pF	
R_{DT}	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)	SROUT DT (ns)	PROUT DT (ns)
28 k	75	375	75	375	75	375	100	375	125	375	150	375	175	375
30 k	75	250	75	325	100	375	100	375	125	375	150	375	175	375
33 k	75	200	75	250	100	300	125	375	150	375	175	375	200	375
36 k	75	175	75	200	100	250	125	325	150	375	175	375	225	375
40 k	75	150	100	175	125	225	150	275	175	325	200	375	250	375
44 k	75	125	100	150	125	200	150	250	175	300	225	350	275	375
48 k	100	125	125	150	150	175	175	225	200	275	250	325	300	375
53 k	100	100	125	125	150	175	200	200	225	250	275	300	325	375
58 k	125	100	150	125	175	150	200	200	250	250	300	300	350	350
64 k	125	100	150	125	175	150	225	200	275	225	325	275	375	325
71 k	150	100	175	125	200	150	250	175	300	225	350	250	375	325
78 k	150	100	175	100	225	150	275	175	325	200	375	250	375	300
86 k	175	75	200	100	250	125	300	175	375	200	375	250	375	300
94 k	175	75	225	100	275	125	325	175	375	200	375	225	375	275
104 k	200	75	250	100	300	125	375	150	375	200	375	225	375	275
114 k	225	75	275	100	325	125	375	150	375	175	375	225	375	275
126 k	250	75	300	100	375	125	375	150	375	175	375	225	375	275
138 k	275	75	325	100	375	125	375	150	375	175	375	225	375	250
152 k	300	75	350	100	375	125	375	150	375	175	375	225	375	250

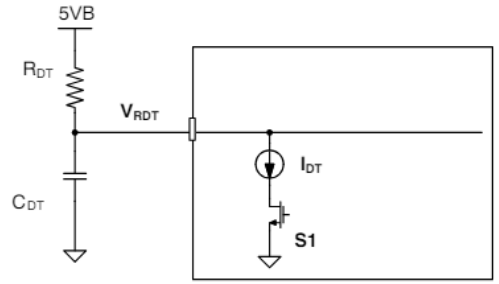


Figure 72. Internal Current Source for of RDT Pin

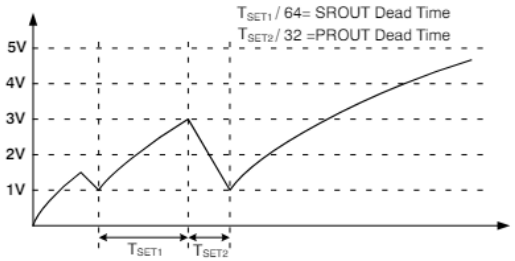
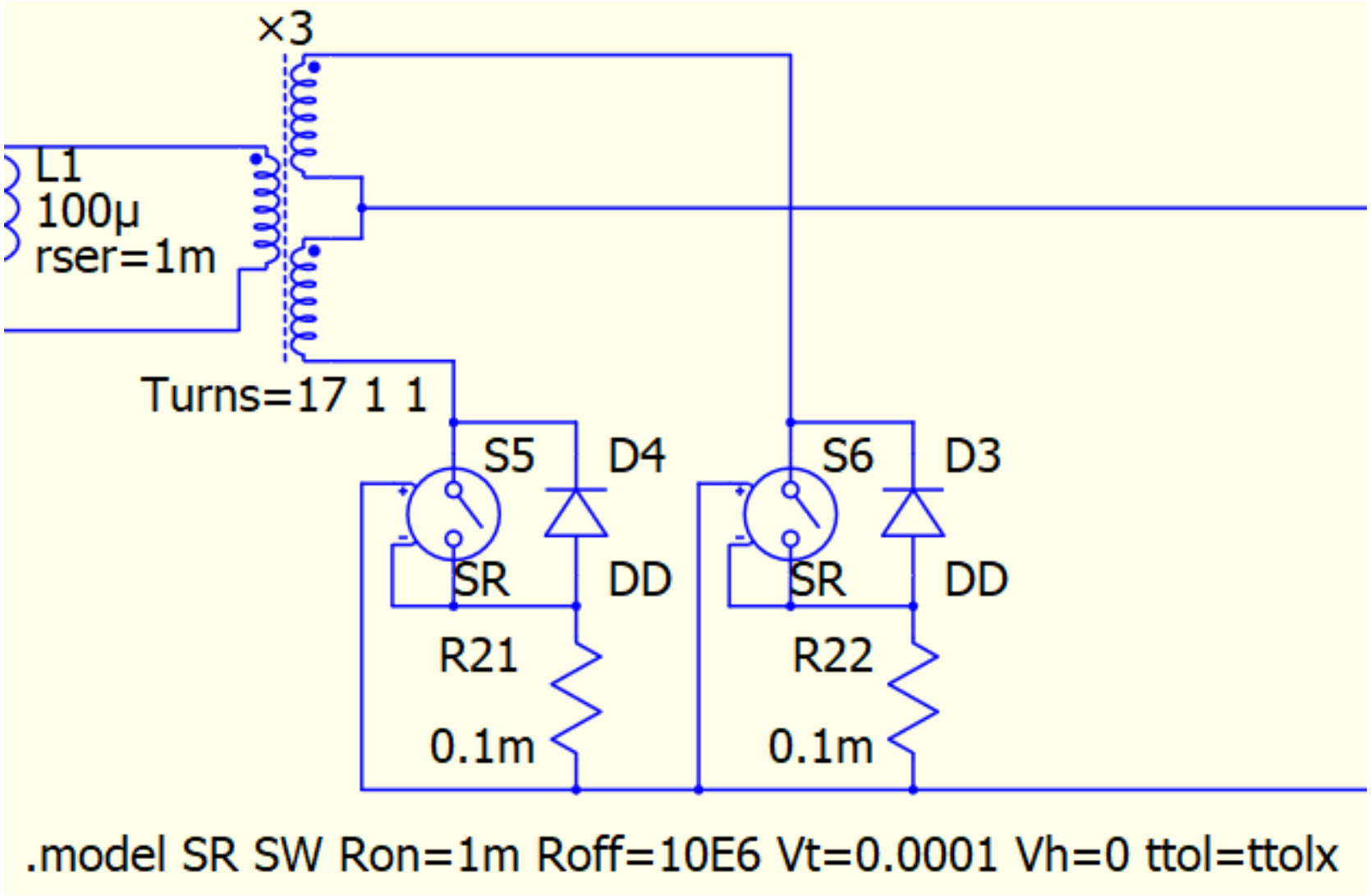


Figure 73. Multi−function Operation of RDT Pin

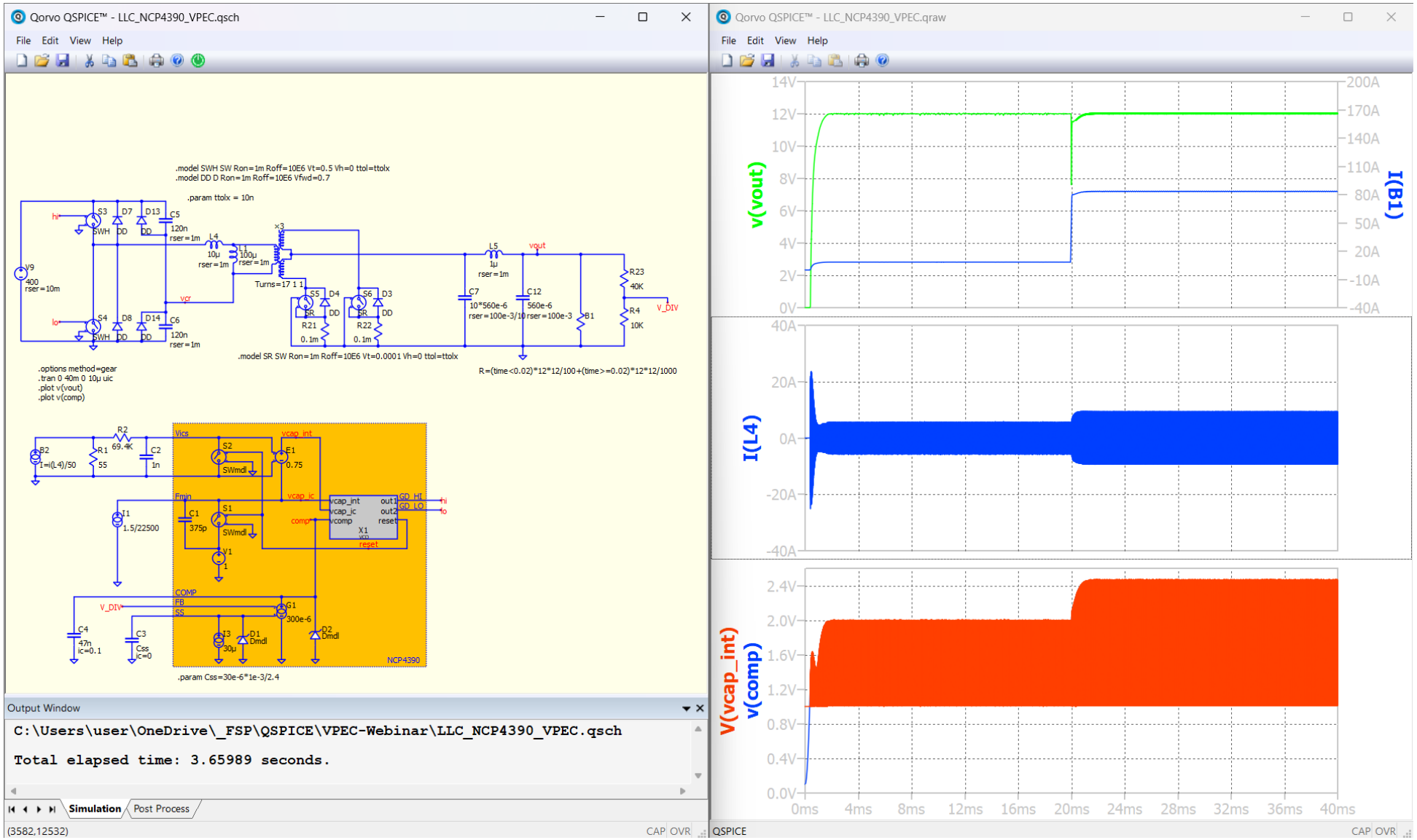
Practical Note:

1. Secondary side deadtime should be greater than primary side deadtime
2. In simulation, this

Simplified SR Implementation



Transient simulation result



Frequency Response Analysis simulation result