Chapter 4 – Software and Hardware tools used

4.1 SOFTWARE

4.1.1 Libero® Soc Design Suite

Libero® SoC Design Suite offers high productivity with its comprehensive, easy-to-learn, easy-to-adopt development tools for designing with Microsemi's PolarFire, IGLOO2, SmartFusion2, RTG4, SmartFusion, IGLOO, ProASIC3 and Fusion families. The suite integrates industry standard Synopsys Synplify Pro® synthesis and Mentor Graphics ModelSim® simulation with best-in-class constraints management, Programming & Debug Tools capabilities, and secures production programming support.

This software suite provided the main IDE for VHDL system development. The IDE being highly expansive in nature supports real –time debugging, code formatting etc. which proved to be highly integral to the programming tasks at hand. The IDE was meant to support both VHDL and Verilog development. Additionally the IDE supported Smart Design™ which is a feature typical to this design suite: which allows seamless programming of complex modules consisting of many small sub modules. These sub modules are available as basic drag and drop entities in the software. The complete software suite had a number of other tools (especially those developed by Microsemi) which allowed easier testing of the concerned sub modules by means of waveforms.

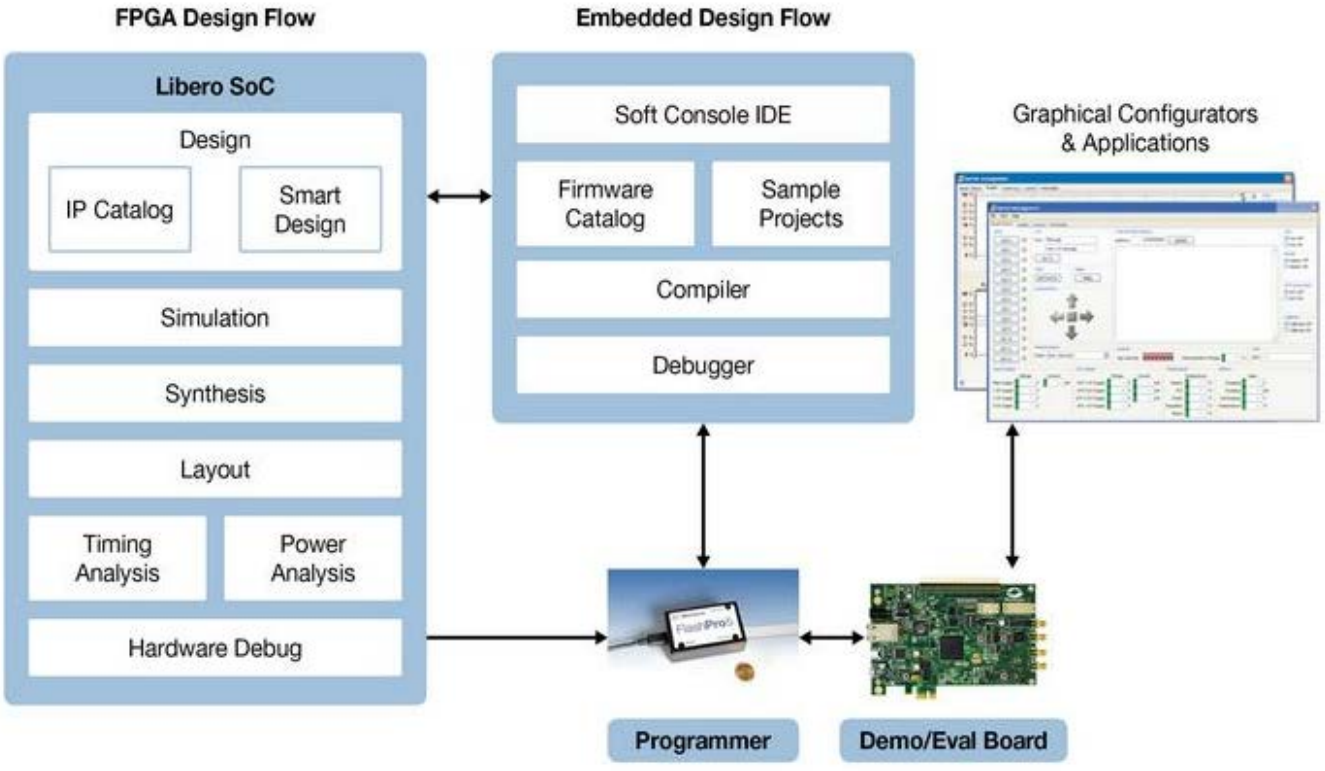

Figure 4.1.1 The FPGA design flow represented by means of usage of Libero SoC software

4.1.2 Xilinx ISE Design Suite

SE® design suite supports the Spartan®-6, Virtex®-6, and CoolRunner™ devices, as well as their previous generation families. ISE® design suite runs on Windows XP/7/Server and Linux operating systems. Additionally, ISE supports Spartan-6 devices on Windows 10. The significance of this software for interlock programming is the easy testing sequence it provides for even complex modules. The waveforms (random, toggle and pulse) sequences are easily generated by a few click of the mouse and a very large number of input test cases can be easily obtained.

4.2 HARDWARE

4.2.1 ProASIC3 Flash Family FPGAs

This was the main target FPGA onto which programs developed were loaded. Following is a brief summary of its features.

High Capacity

• 15 K to 1 M System Gates

• Up to 144 Kbits of True Dual-Port SRAM

• Up to 300 User I/Os

Reprogrammable Flash Technology

• 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process

• Instant On Level 0 Support

• Single-Chip Solution

• Retains Programmed Design when Powered Off

High Performance

• 350 MHz System Performance

• 3.3 V, 66 MHz 64-Bit PCI†

In-System Programming (ISP) and Security

• ISP Using On-Chip 128-Bit Advanced Encryption Standard

(AES) Decryption (except ARM®-enabled ProASIC®3 devices) via JTAG (IEEE 1532–compliant)†

• FlashLock® to Secure FPGA Contents

Low Power

• Core Voltage for Low Power

• Support for 1.5 V-Only Systems

• Low-Impedance Flash Switches

High-Performance Routing Hierarchy

• Segmented, Hierarchical Routing and Clock Structure

Advanced I/O

• 700 Mbps DDR, LVDS-Capable I/Os (A3P250 and above)

• 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operations

• Wide Range Power Supply Voltage Support per JESD8-B, Allowing I/Os to Operate from 2.7 V to 3.6 V

• Bank-Selectable I/O Voltages—up to 4 Banks per Chip • Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X† and LVCMOS 2.5 V / 5.0 V Input

• Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (A3P250 and above)

• I/O Registers on Input, Output, and Enable Paths

• Hot-Swappable and Cold Sparing I/Os‡

• Programmable Output Slew Rate† and Drive Strength

• Weak Pull-Up/-Down

• IEEE 1149.1 (JTAG) Boundary Scan Test

• Pin-Compatible Packages across the ProASIC3 Family

Clock Conditioning Circuit (CCC) and PLL†

• Six CCC Blocks, One with an Integrated PLL

• Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback

• Wide Input Frequency Range (1.5 MHz to 350 MHz)

Embedded Memory†

• 1 Kbit of FlashROM User Nonvolatile Memory

• SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM

Blocks (×1, ×2, ×4, ×9, and ×18 organizations)†

• True Dual-Port SRAM (except ×18)

ARM Processor Support in ProASIC3 FPGAs

• M1 ProASIC3 Devices—ARM®Cortex®-M1 Soft Processor Available with or without Debug.

4.2.2 M&SL Test JIG

The M&SL test jig is a state of the art device which lets a user test any VHDL logic uploaded to an FPGA in real time. The test jig used in this project is manufactured by RATO Communications (RACE) and supports testing of one FPGA board at a time. The test jig in consideration here provides three I/O lines. Each I/O has up to 62 individual switch I/Os which have two states (high/low) and can be controlled manually so that synthetic testing conditions can be created. The test jig supports up to 24 V DC supply with probe type inputs and also a standard plug and socket input. Each I/O on the test jig can be manually mapped by the user with the help of the mapping tables. Table below shows the I/O mapping for testing of module 5a:

I/O names in program	Corresponding I/O on test jig
AI 57	DI 1-1
DI 13	D1 1-2
DI 14	DI 1-3
DI 15	DI 1-4
DI 16	DI 1-5
DI 86	DI 1-6
DI 87	DI 1-7
DI 88	DI 1-8
DI 89	DI 1-9
DI 90	DI 1-10
DI 91	DI 1-11
DI 92	DI 1-12
DI 93	DI 1-13
DI 94	DI 1-14
DI 95	DI 1-15
DI 98	DI 1-16
DI 99	DI 1-17
Sense_Finger_error	DI 1-18
Y5_a	DO-1

- **DI 1 & DI 19 weren't mapped by the software because of redundancy in the logic where these pins were involved.**
- **To obtain pin reports and mappings done by Libero IDE, click on design flow, in the bottom click on export pin reports. After that in the work window click on project summary under that click on <project name> reports.**
- **The entire test jig works in active low or gives out inverted output.**