Chapter 7 – Recommendations and future work

The team after careful scrutiny and testing of the interlocks has proposed the following future course of steps and actions concerning the project.

- All modules should be tested by flashing the same on the ProAsic3L FPGA.
- Software simulation should be enhanced by introduction of more rigorous test benches. *Rigorous* here refers to complex inputs with more than one input making a transition at the same instant of time.
- All modules and sub modules should be simultaneously tested; this would open up more opportunities in the concept of pin and BUS multiplexing due to the large number of inputs (both analog and digital) involved.
- The same methodology and coding style should be followed throughout while developing similar such interlocks in VHDL.
- A similar convention of variable names should be used especially when referring to the same set of variables, parameters, predefined values and constants.
- As specified in the main list of interlocks, the memory organization (non –volatile) for constants should be done in a way so as to facilitate faster access and easier retrieval. Maximal usage of on-board ROM is encouraged in such cases.