IEEE-488 Common Commands

This subsystem contains commands and queries associated with the IEEE-488 standards:

*CLS - Clear status

*ESE <enable_value> - Event status enable

*ESR? - Event status register query

*IDN? - Instrument identification

*OPC - Set operation complete bit

*OPC? - Wait for current operation to complete

*OPT? - Show installed options

*PSC {0|1} - Power-on status clear

*RCL {0|1|2|3|4} - Recall instrument state

*RST - Reset instrument to factory defaults

*SAV {0|1|2|3|4} - Save instrument state

*SRE <enable_value> - Service request enable (enable bits in enable register of Status Byte Register group

*STB? - Read status byte

*TRG - Trigger command

*TST? - Self-test

*WAI - Wait for all pending operations to complete

Registers

Some of the IEEE-488 commands are associated with various registers in the instrument. These registers are described below.

Standard Event Register

The following table describes the Standard Event Register.

Bit Number	Bit Name	Decimal Value	Definition
0	Operation Complete	1	All commands before and including *OPC have been executed.
1	(not used)	2	(Reserved for future use)
2	Query Error	4	The instrument tried to read the output buffer but it was empty. Or, a new command line was received before a previous query has been read. Or, both the input and output buffers are full.
3	Device-Specific Error	8	A device-specific error, including a self-test error, calibration error or other device-specific error occurred. See Error Messages.
4	Execution Error	16	An execution error occurred. Error Messages
5	Command	32	A command syntax error occurred. Error Messages
6	(not used)	64	(Reserved for future use)
7	Power On	128	Power has been cycled since the last time the event register was read or cleared.

Status Byte Register

The following table describes the Status Byte Register.

Bit Number	Bit Name	Decimal Value	Definition
0	(not used)	1	(Reserved for future use)
1	(not used)	2	(Reserved for future use)
2	Error Queue	4	One or more errors in the Error Queue. Use SYSTem:ERRor? to read and delete errors.
3	Questionable Data Summary	8	One or more bits are set in the Questionable Data Register (bits must be enabled, see STATus:QUEStionable:ENABle).
4	Message Available	16	Data is available in the instrument's output buffer.
5	Standard Event Summary	32	One or more bits are set in the Standard Event Register (bits must be enabled, see *ESE).
6	Master Summary	64	One or more bits are set in the Status Byte Register and may generate a Request for Service (RQS). Bits must be enabled using *SRE.
7	Operation Register	128	One or more bits are set in the Operation Status Register. Bits are enabled using STATus:OPERation:ENABle.

*CLS

Clear Status Command. Clears the event registers in all register groups. Also clears the error queue.

Parameter	Typical Return
(none)	(none)

Clear event register bits and error queue:
*CLS

*ESE <enable_value>
*ESE?

Event Status Enable Command and Query. Enables bits in the enable register for the Standard Event Register group. The selected bits are then reported to bit 5 of the Status Byte Register.

Parameter	Typical Return
Decimal sum of the bits in the register (table below), default 0. For example, to enable bit 2 (value 4), bit 3 (value 8), and bit 7 (value 128), the decimal sum would be 140 (4 + 8 + 128). Default 0.	+48

Enable bit 4 (value 16) and bit 5 (value 32) in the enable register:
*ESE 48

- Use *PSC to control whether the Standard Event enable register is cleared at power on. For example, *PSC 0 preserves the enable register contents through power cycles.
- *CLS does not clear enable register, does clear event register.

*ESR?

Standard Event Status Register Query. Queries the event register for the Standard Event Register group. Register is read-only; bits not cleared when read.

Parameter	Typical Return
(none)	+24

Read the event register (bits 3 and 4 are set):
*ESR?

- Any or all conditions can be reported to the Standard Event summary bit through the enable register. To set the enable register mask, write a decimal value to the register using *ESE.
- Once a bit is set, it remains set until cleared by this query or *CLS.

*IDN?

Identification Query. Returns instrument's identification string.

Parameter	Typical Return
(none)	Agilent Technologies,33522B,XXXXXXXXXX,0.179-1.19-8.88-52-00

Return the instrument's identification string:
*IDN?

- Identification string contains four comma separated fields:
  - Manufacturer name
  - Model number
  - Serial number
  - Revision code
- Identification string is in the following format for the 33500 Series instruments:

  Agilent Technologies,[Model Number],[10-char Serial Number],A.aaa-B.bb-C.cc-DD-EE

  A.aaa = Firmware revision

  B.bb = Front panel FW revision

  C.cc = Power supply controller FW revision

  DD = FPGA revision

  EE = PCBA revision
- Identification string is in the following format for the 33600 Series instruments:

  Agilent Technologies,[Model Number],[Serial Number],A.aa.aa-B.bb-CC-DD-EE

  A.aa.aa = Firmware revision

  B.bb = Front panel FW revision

  CC = Main board revision

  DD = FPGA revision

  EE = PCBA revision

*OPC

Sets "Operation Complete" (bit 0) in the Standard Event register at the completion of the current operation.

Parameter	Typical Return
(none)	(none)

Set Operation Complete bit:
*OPC

- The purpose of this command is to synchronize your application with the instrument.
- Used in triggered sweep, triggered burst, list, or arbitrary waveform sequence modes to provide a way to poll or interrupt the computer when the *TRG or INITiate[:IMMediate] is complete.
- Other commands may be executed before Operation Complete bit is set.
- The difference between *OPC and *OPC? is that *OPC? returns "1" to the output buffer when the current operation completes. This means that no further commands can be sent after an *OPC? until it has responded. In this way an explicit polling loop can be avoided. That is, the IO driver will wait for the response.

*OPC?

Returns 1 to the output buffer after all pending commands complete.

Parameter	Typical Return
(none)	1

Return 1 when all previous commands complete:
*OPC?

- The purpose of this command is to synchronize your application with the instrument.
- Other commands cannot be executed until this command completes.
- The difference between *OPC and *OPC? is that *OPC? returns "1" to the output buffer when the current operation completes. This means that no further commands can be sent after an *OPC? until it has responded. In this way an explicit polling loop can be avoided. That is, the IO driver will wait for the response.

*OPT?

Returns a quoted string identifying any installed options.

Parameter	Typical Return
(none)	"0,MEM,SEC,EQP"

Returns installed options (example: standard timebase, extended memory, security, IQ player)
*OPT?

*PSC {0|1}
*PSC?

Power-On Status Clear. Enables (1) or disables (0) clearing of two specific registers at power on:

- Standard Event enable register (*ESE).
- Status Byte condition register (*SRE).
- Questionable Data Register
- Standard Operation Register

Parameter	Typical Return
{0|1},default 1	0 or 1

Disables power-on clearing of affected registers:
*PSC 0

- This setting is non-volatile through a power-cycle. If it therefore useful for GPIB connection as follows:

  ***PSC 0** to disable enable clearing
  ***ESE 128** to enable power-on event
  ***SRE 32** to enable a SRQ on std event

  This short program now provides a GPIB SRQ signal when the unit is turned on.

*RCL {0|1|2|3|4}
*SAV {0|1|2|3|4}

Recalls (*RCL) or saves (*SAV) instrument state in specified non-volatile location. Previously stored state in location is overwritten (no error is generated).

NOTE For 33600 Series instruments, the state files associated with *SAV and *RCL are saved in files called STATE_0.STA through STATE_4.STA. These files are located in the Settings directory of internal memory. You can manage these files using MEMory commands.

Parameter	Typical Return
{0|1|2|3|4}	(none)

Recall state from location 1:
*RCL 1

- The instrument has five non-volatile storage locations to store instrument states. Location 0 holds the instrument power down state. Use locations 1, 2, 3, and 4 to store other states. You can configure the instrument to recall the power-down state when power is restored (MEMory:STATe:RECall:AUTO).
- State storage "remembers" the selected function (including arbitrary waveforms), frequency, amplitude, DC offset, duty cycle, symmetry, as well as any modulation parameters in use. Also remembers front panel display state (DISPlay).
- When shipped from the factory, locations 1 through 4 are empty, and location 0 has power-on state.
- From the remote interface only, you can use location 0 to store a fifth instrument state (you cannot store to this location from the front panel). However, location 0 is overwritten when power is cycled.
- You can assign a user-defined name to each of locations 0 through 4.
- States stored in memory are not affected by *RST.
- If you delete an arbitrary waveform from non-volatile memory after storing the instrument state, the waveform data is lost and the instrument will not output the waveform when the state is recalled; it will output the built-in "exponential rise" instead.
- The front panel uses MMEMory subsystem for state storage.

*RST

Resets instrument to factory default state, independent of MEMory:STATe:RECall:AUTO setting.

Parameter	Typical Return
(none)	(none)

Reset the instrument:
*RST

- Does not affect stored instrument states, stored arbitrary waveforms, or I/O settings; these are stored in non-volatile memory.
- Aborts a sweep or burst in progress.

*SRE <enable_value>
*SRE?

Service Request Enable. This command enables bits in the enable register for the Status Byte Register group.

Parameter	Typical Return
Decimal sum of the bits in the register (table below), default 0. For example, to enable bit 2 (value 4), bit 3 (value 8), and bit 7 (value 128), the decimal sum would be 140 (4 + 8 + 128). Default 0.	+24

Enable bits 3 and 4 in the enable register:
*SRE 24

- To enable specific bits, specify the decimal value corresponding to the binary-weighted sum of the bits in the register. The selected bits are summarized in the "Master Summary" bit (bit 6) of the Status Byte Register. If any of the selected bits change from 0 to 1, the instrument generates a Service Request signal.
- *CLS clears the event register, but not the enable register.
- *PSC (power-on status clear) determines whether Status Byte enable register is cleared at power on. For example, *PSC 0 preserves the contents of the enable register through power cycles.
- Status Byte enable register is not cleared by *RST.

*STB?

Read Status Byte Query. This command queries the condition register for the Status Byte Register group.

Parameter	Typical Return
(none)	+40

Read condition register (with bits 3 and 5 set):
*STB?

- Similar to a Serial Poll, but processed like any other instrument command. Register is read-only; bits not cleared when read.
- Returns same result as a Serial Poll, but "Master Summary" bit (bit 6) is not cleared by *STB?.
- Power cycle or *RST clears all bits in condition register.
- Returns a decimal value that corresponds to the binary-weighted sum of all bits set in the register. For example, with bit 3 (value 8) and bit 5 (value 32) set (and corresponding bits enabled), the query returns +40.

*TRG

Trigger Command. Triggers a sweep, burst, arbitrary waveform advance, or LIST advance from the remote interface if the bus (software) trigger source is currently selected (TRIGger[1|2]:SOURce BUS).

Parameter	Typical Return
(none)	(none)

Send immediate trigger to initiate a burst:
SOUR1:BURS:MODE TRIG
BURS:MODE TRIG
TRIG:SOUR BUS
*TRG

*TST?

Self-Test Query. Performs a complete instrument self-test. If test fails, one or more error messages will provide additional information. Use SYSTem:ERRor? to read error queue.

Parameter	Typical Return
(none)	+0 (pass) or +1 (one or more tests failed)

Perform self-test:
*TST?

- A power-on self-test occurs when you turn on the instrument. This limited test assures you that the instrument is operational.
- A complete self-test (*TST?) takes approximately 15 seconds. If all tests pass, you have high confidence that the instrument is fully operational.
- Passing *TST? displays "Self-Test Passed" on the front panel. Otherwise, it displays "Self-Test Failed" and an error number. See Service and Repair - Introduction for instructions on contacting support or returning the instrument for service.

*WAI

Configures the instrument to wait for all pending operations to complete before executing any additional commands over the interface.

Parameter	Typical Return
(none)	(none)

Wait until all pending operations complete.
*WAI

- For example, you can use this with the *TRG command to ensure that the instrument is ready for a trigger:

  *TRG;*WAI;*TRG