	Performance event profiles Sqrt(A(1:LEN_1D)) + B .* C	(1:LEN_1D)	ARITH:DIVIDER_ACTIVE BACLEARS:ANY BR_INST_RETIRED:ALL_BRANCHES BR_INST_RETIRED:CONDITIONAL BR_INST_RETIRED:FAR_BRANCH BR_INST_RETIRED:NEAR_CALL BR_INST_RETIRED:NEAR_TAKEN BR_INST_RETIRED:NOT_TAKEN BR_MISP_RETIRED:ALL_BRANCHES BR_MISP_RETIRED:NEAR_CALL BR_MISP_RETIRED:NEAR_CALL CPU_CLK_THREAD_UNHALTED:ONE_THREAD_ACTIVE CPU_CLK_THREAD_UNHALTED:REF_XCLK CPU_CLK_THREAD_UNHALTED:REF_XCLK
2000 - 1.75 - 1.50 - 1.75 - 1.50 - 1.75 - 1.50 - 1.		Mary Mary Mary Mary Mary Mary Mary Mary	CPU_CLK_THREAD_UNHALTED:RINGO_TRANS CPU_CLK_THREAD_UNHALTED:THREAD_P CYCLE_ACTIVITY:CYCLES_L1D_MISS CYCLE_ACTIVITY:CYCLES_L2_MISS CYCLE_ACTIVITY:CYCLES_L3_MISS CYCLE_ACTIVITY:CYCLES_MEM_ANY CYCLE_ACTIVITY:STALLS_L1D_MISS CYCLE_ACTIVITY:STALLS_L2_MISS CYCLE_ACTIVITY:STALLS_L2_MISS CYCLE_ACTIVITY:STALLS_L3_MISS CYCLE_ACTIVITY:STALLS_L3_MISS CYCLE_ACTIVITY:STALLS_TOTAL DSB2MITE_SWITCHES:PENALTY_CYCLES DTLB_LOAD_MISSES:MISS_CAUSES_A_WALK DTLB_LOAD_MISSES:STLB_HIT DTLB_LOAD_MISSES:WALK_ACTIVE DTLB_LOAD_MISSES:WALK_COMPLETED
0.025 - 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 - 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 0.025 - 0.02			DTLB_LOAD_MISSES:WALK_COMPLETED_1G DTLB_LOAD_MISSES:WALK_COMPLETED_4K DTLB_LOAD_MISSES:WALK_PENDING DTLB_STORE_MISSES:MISS_CAUSES_A_WALK DTLB_STORE_MISSES:WALK_ACTIVE DTLB_STORE_MISSES:WALK_COMPLETED DTLB_STORE_MISSES:WALK_COMPLETED DTLB_STORE_MISSES:WALK_COMPLETED_1G DTLB_STORE_MISSES:WALK_COMPLETED_2M_4M DTLB_STORE_MISSES:WALK_COMPLETED_4K DTLB_STORE_MISSES:WALK_PENDING EPT:WALK_PENDING EXE_ACTIVITY:1_PORTS_UTIL EXE_ACTIVITY:3_PORTS_UTIL EXE_ACTIVITY:4_PORTS_UTIL
10000 - 60 - 4000 - 1000 - 100			EXE_ACTIVITY:BOUND_ON_STORES EXE_ACTIVITY:EXE_BOUND_0_PORTS FP_ARITH_INST_RETIRED:128B_PACKED_DOUBLE FP_ARITH_INST_RETIRED:128B_PACKED_SINGLE FP_ARITH_INST_RETIRED:256B_PACKED_DOUBLE FP_ARITH_INST_RETIRED:256B_PACKED_SINGLE FP_ARITH_INST_RETIRED:SCALAR_DOUBLE FP_ARITH_INST_RETIRED:SCALAR_SINGLE FP_ASSIST:ANY FRONTEND_RETIRED:DSB_MISS FRONTEND_RETIRED:ITLB_MISS FRONTEND_RETIRED:L11_MISS FRONTEND_RETIRED:L2_MISS HLE_RETIRED:ABORTED HLE_RETIRED:ABORTED_EVENTS
-0.025			HLE_RETIRED:ABORTED_MEMTYPE HLE_RETIRED:ABORTED_UNFRIENDLY HLE_RETIRED:COMMIT HLE_RETIRED:START HW_INTERRUPTS:RECEIVED ICACHE_16B:IFDATA_STALL ICACHE_64B:IFTAG_HIT ICACHE_64B:IFTAG_STALL IDQ:ALL_DSB_CYCLES_4_UOPS IDQ:ALL_DSB_CYCLES_ANY_UOPS IDQ:ALL_MITE_CYCLES_ANY_UOPS IDQ:DSB_UOPS IDQ:DSB_UOPS_CYCLES
4000 - 2000 - 15000 - 2000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 10000 - 25000 - 2			IDQ:MITE_UOPS IDQ:MITE_UOPS_CYCLES IDQ:MS_DSB_UOPS_CYCLES IDQ:MS_MITE_UOPS IDQ:MS_MITE_UOPS IDQ:MS_WITCHES IDQ:MS_UOPS IDQ:MS_UOPS IDQ:MS_UOPS_CYCLES IDQ_UOPS_NOT_DELIVERED:CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_O_UOPS_DELIV_CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_IE_1_UOPS_DELIV_CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_LE_1_UOPS_DELIV_CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_LE_2_UOPS_DELIV_CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_LE_3_UOPS_DELIV_CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_LE_3_UOPS_DELIV_CORE IDQ_UOPS_NOT_DELIVERED:CYCLES_LE_3_UOPS_DELIV_CORE INT_MISC:CLEAR_RESTEER_CYCLES INT_MISC:RECOVERY_CYCLES
100 - 0.050 - 0.025 - 0.0250.050 - 100			INT_MISC:RECOVERY_CYCLES_ANY ITLB:ITLB_FLUSH ITLB_MISSES:MISS_CAUSES_A_WALK ITLB_MISSES:MALK_COMPLETED ITLB_MISSES:WALK_COMPLETED_1G ITLB_MISSES:WALK_COMPLETED_2M_4M ITLB_MISSES:WALK_COMPLETED_4K ITLB_MISSES:WALK_PENDING L1D_PEND_MISS:PB_FULL L1D_PEND_MISS:PENDING L1D_PEND_MISS:PENDING_CYCLES L1D_PEND_MISS:PENDING_CYCLES_ANY L1D:REPLACEMENT L2_LINES_IN:ALL L2_LINES_OUT:NON_SILENT
2000 - 1000 - 2000 - 1000 - 2000 - 1000 - 2000 - 1000 - 2000 - 1000 - 2000 - 1000 - 2000 - 1000 - 2000 - 1000 - 2000 - 2000 - 1000 - 20			L2_LINES_OUT:USELESS_HWPF L2_LINES_OUT:USELESS_HWPREF L2_RQSTS:ALL_CODE_RD L2_RQSTS:ALL_DEMAND_DATA_RD L2_RQSTS:ALL_DEMAND_MISS L2_RQSTS:ALL_DEMAND_REFERENCES L2_RQSTS:ALL_PF L2_RQSTS:ALL_RFO L2_RQSTS:CODE_RD_HIT L2_RQSTS:CODE_RD_MISS L2_RQSTS:DEMAND_DATA_RD_HIT L2_RQSTS:DEMAND_DATA_RD_MISS L2_RQSTS:PF_HIT L2_RQSTS:PF_HIT L2_RQSTS:PF_MISS L2_RQSTS:PF_MISS L2_RQSTS:REFERENCES
0e+00 - 1500 - 1000 - 1000 - 80000 - 80000 - 1000 - 0.025 - 0.			L2_RQSTS:RFO_HIT L2_RQSTS:RFO_MISS L2_TRANS:L2_WB LD_BLOCKS:NO_SR LD_BLOCKS_PARTIAL:ADDRESS_ALIAS LD_BLOCKS:STORE_FORWARD LOAD_HIT_PRE:SW_PF LONGEST_LAT_CACHE:MISS LONGEST_LAT_CACHE:REFERENCE LSD:CYCLES_4_UOPS LSD:CYCLES_ACTIVE LSD:UOPS MACHINE_CLEARS:COUNT MACHINE_CLEARS:MEMORY_ORDERING MACHINE_CLEARS:SMC MEM_INST_RETIRED:ALL_LOADS
16000 - 15000 - 15000 - 10000			MEM_INST_RETIRED:ALL_STORES MEM_INST_RETIRED:SPLIT_LOADS MEM_INST_RETIRED:SPLIT_STORES MEM_INST_RETIRED:STLB_MISS_LOADS MEM_INST_RETIRED:STLB_MISS_STORES MEM_LOAD_L3_HIT_RETIRED:XSNP_HIT MEM_LOAD_L3_HIT_RETIRED:XSNP_HITM MEM_LOAD_L3_HIT_RETIRED:XSNP_MISS MEM_LOAD_L3_HIT_RETIRED:XSNP_MISS MEM_LOAD_L3_HIT_RETIRED:XSNP_NONE MEM_LOAD_MISC_RETIRED:UC MEM_LOAD_RETIRED:L1_HIT MEM_LOAD_RETIRED:L1_HIT MEM_LOAD_RETIRED:L1_HIT MEM_LOAD_RETIRED:L2_HIT MEM_LOAD_RETIRED:L2_HIT MEM_LOAD_RETIRED:L2_HIT MEM_LOAD_RETIRED:L2_HIT
0 - 200 - 100 - 100 - 100 - 50 - 100 - 50 - 100 - 50 - 100 -		Maybanda Marahan Marah	MEM_LOAD_RETIRED:L3_HIT MEM_LOAD_RETIRED:L3_HISS OFFCORE_REQUESTS:ALL_DATA_RD OFFCORE_REQUESTS:ALL_REQUESTS OFFCORE_REQUESTS_BUFFER:SQ_FULL OFFCORE_REQUESTS:DEMAND_CODE_RD OFFCORE_REQUESTS:DEMAND_DATA_RD OFFCORE_REQUESTS:L3_MISS_DEMAND_DATA_RD OFFCORE_REQUESTS:L3_MISS_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:ALL_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:CYCLES_WITH_DEMAND_CODE_RD OFFCORE_REQUESTS_OUTSTANDING:CYCLES_WITH_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:CYCLES_WITH_DEMAND_RFO OFFCORE_REQUESTS_OUTSTANDING:CYCLES_WITH_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:CYCLES_WITH_L3_MISS_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:CYCLES_WITH_L3_MISS_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:DEMAND_CODE_RD OFFCORE_REQUESTS_OUTSTANDING:DEMAND_CODE_RD
8000 - 8000 - 20			OFFCORE_REQUESTS_OUTSTANDING:DEMAND_DATA_RD_GE_6 OFFCORE_REQUESTS_OUTSTANDING:L3_MISS_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:L3_MISS_DEMAND_DATA_RD OFFCORE_REQUESTS_OUTSTANDING:L3_MISS_DEMAND_DATA_RD_GE_6 OTHER_ASSISTS:ANY PARTIAL_RAT_STALLS:SCOREBOARD RESOURCE_STALLS:ANY RESOURCE_STALLS:SB ROB_MISC_EVENTS:LBR_INSERTS ROB_MISC_EVENTS:PAUSE_INST RS_EVENTS:EMPTY_CYCLES RS_EVENTS:EMPTY_END RTM_RETIRED:ABORTED_ RTM_RETIRED:ABORTED_MEM RTM_RETIRED:ABORTED_MEM RTM_RETIRED:ABORTED_MEMTYPE
			RTM_RETIRED:ABORTED_UNFRIENDLY RTM_RETIRED:COMMIT RTM_RETIRED:START SQ_MISC:SPLIT_LOCK SW_PREFETCH_ACCESS:NTA SW_PREFETCH_ACCESS:PREFETCHW SW_PREFETCH_ACCESS:T0 SW_PREFETCH_ACCESS:T1_T2 TLB_FLUSH:DTLB_THREAD TLB_FLUSH:STLB_ANY TX_EXEC:MISC1 TX_EXEC:MISC2 TX_EXEC:MISC3 TX_EXEC:MISC4 TX_EXEC:MISC5 TX_MEM:ABORT_CAPACITY
0.005 - 0.025 - 0.005 - 0.025			TX_MEM:ABORT_CONFLICT TX_MEM:ABORT_HLE_ELISION_BUFFER_FULL TX_MEM:ABORT_HLE_ELISION_BUFFER_MISMATCH TX_MEM:ABORT_HLE_ELISION_BUFFER_NOT_EMPTY TX_MEM:ABORT_HLE_ELISION_BUFFER_UNSUPPORTED_ALIGNMENT TX_MEM:ABORT_HLE_STORE_TO_ELIDED_LOCK UOPS_DISPATCHED_PORT:PORT_0 UOPS_DISPATCHED_PORT:PORT_1 UOPS_DISPATCHED_PORT:PORT_2 UOPS_DISPATCHED_PORT:PORT_3 UOPS_DISPATCHED_PORT:PORT_4 UOPS_DISPATCHED_PORT:PORT_5 UOPS_DISPATCHED_PORT:PORT_6 UOPS_DISPATCHED_PORT:PORT_7 UOPS_EXECUTED:CORE UOPS_EXECUTED:CORE_CYCLES_GE_1
2e+05- 150000- 1000000- 500000- 1000000- 500000- 1000000- 500000- 1000000- 500000- 6e+05- 4e+05- 2e+05- 1e+05- 2e+05- 1e+05- 1000000- 100000- 1000000- 10000- 10			UOPS_EXECUTED:CORE_CYCLES_GE_2 UOPS_EXECUTED:CORE_CYCLES_GE_3 UOPS_EXECUTED:CORE_CYCLES_GE_4 UOPS_EXECUTED:CORE_CYCLES_NONE UOPS_EXECUTED:STALL_CYCLES UOPS_EXECUTED:THREAD UOPS_EXECUTED:THREAD_CYCLES_GE_1 UOPS_EXECUTED:THREAD_CYCLES_GE_2 UOPS_EXECUTED:THREAD_CYCLES_GE_3 UOPS_EXECUTED:THREAD_CYCLES_GE_4 UOPS_EXECUTED:THREAD_CYCLES_GE_4 UOPS_EXECUTED:THREAD_CYCLES_GE_4 UOPS_ISSUED:ANY UOPS_ISSUED:SLOW_LEA UOPS_ISSUED:STALL_CYCLES UOPS_ISSUED:VECTOR_WIDTH_MISMATCH UOPS_RETIRED:RETIRE_SLOTS
750000 - 500000 - 250000 - 0 - 9e+05 - 6e+05 - 3e+05 - 0e+00 -	e+00 1e+07 2e+07 Retired instructions (INST_RE		UOPS_RETIRED:STALL_CYCLES UOPS_RETIRED:TOTAL_CYCLES