ELE532
Digital HARDWARE

Final Examination
Examiner: S. G. Zaky
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Time: Two and a half hours

No aids allowed

This paper has FOUR questions
All questions are of equal value

1. [15 Marks]

a) Repeaters are often introduced on a long line on an IC to divide the line into shorter sections.

- Give at least two reasons why this may be necessary.
- Is the same thing needed for long lines on a printed-circuit board? Why?

b) The delay t_d and risetime t_r for a line of length d connecting two points on an IC may be approximated by

$$t_d = 0.4\, d^2RC$$

$$t_r = d^2RC$$

where R and C are the line resistance and capacitance per unit length. Two clock lines on this IC are 20 mm long each and have $RC = 1.5 \times 10^{-17}$ s/μm^2.

- Calculate the timing jitter on each line assuming that noise is limited to a maximum of ± 10% of the signal swing.
- What is the maximum clock skew between these two lines?

c) It is proposed to divide each of the clock lines of bart (*b*) into n sections using repeaters. Each repeater introduces a delay in the range 50 to 150 ps.

- Find a suitable value for n to minimize clock skew.

2. [15 Marks]

A 15 mm×15mm integrated circuit has a power supply voltage of 3.3 V, and a clock frequency of 300 MHz. Each gate switches every three clock cycles and drives a capacitive load of 150 fF, on average. A gate completes switching in about a third of a clock cycle.

a) Compute the average supply current per gate.

- Estimate, with explanation, a suitable value for the current waveform factor k_i.
- Based on the symbiotic capacitance of neighbouring gates, compute the voltage variation ΔV experienced by individual gates during switching.

b) Additional bypass capacitance can be provided using the oxide layer as the dielectric, at 5 fF/μm^2.

- Estimate chip area per gate that needs to be dedicated to bypass capacitance to limit ΔV to 0.15 V.
- Assuming that each gate occupies 200 μm^2, how many gates can this chip accommodate?
- What other approaches would you consider to reduce or eliminate the area used to provide bypass capacitors?

3. [15Marks]

a) When IBM researchers announced that they have successfully used copper for the metallization layer in CMOS ICs, this was regarded as a breakthrough that would lead to significant improvements in performance.

- Discuss at least two aspects of digital IC design that would be impacted when aluminum is replaced by copper.

b) Ball Grid Array is an expensive technology. Yet, it is widely used in high-performance ICs.

- Give at least two reasons why BGA can improve the electrical performance of a digital system.

c) Having signals with a short risetime is one of the factors that make it possible to design fast circuits.

- Give at least three reasons why you may want to deliberately increase the risetime of a logic signal.

d) Ground connections provide the return path for signal and power supply current.

- Why are ground connections implemented in the form of a ground plane?
- What are the trade-offs in deciding how close to the ground plane signal lines should be?

4. [15 Marks]

Link AB in the figure below has a characteristic impedance of 75 Ω. It is driven by a matched driver at point A and connected to a matched receiver at point B. As a result of a layout error, an unterminated 75-Ω line is connected to this link at point C. Propagation delays on various line segments are as shown in the figure.

a) Let V_{CD} and V_{DC} be the waves travelling from C to D and from D to C, respectively.

- Complete the table below for the first 12 ns following a 0-to-3 V transition at point A. (Copy the table in your answer book.)
- Plot the voltage waveforms at points A, C, B, and D during the same period.
- What is the steady-state voltage at these points?

Time (ns)	0	2	4	6	8	10	12
V_{CD}							
V_{DC}							
V_C							
V_D							

b) The link from A to B is used to transmit information at the rate of 250 MHz.

- What is the worst-case intersymbol interference?