ECE-451 VLSI SYSTEMS SPRING 2001

Final Exam. April 20. 2001
(Total Points: 100)

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**Student Name:** _____

**Student Number:** _____

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**Course:** ECE-451. VLSI Systems

**Instructor:** Farid N. Najm

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This exam is open book, open notes. Time limit is 2.5 hours. Check for a total of 6 problems on 10 pages. Notice that the problems do not have equal weight. Write your work and all your answers on these sheets and use the back of a page if you need more space. Good luck!

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**Reminders:**

- 1 msec=$10^{-3}$ sec, 1 $\mu$sec=$10^{-6}$ sec, 1 nsec=$10^{-9}$ sec, 1 pF=$10^{-12}$F, and 1 fF=$10^{-15}$ F.
- Unless specified otherwise, you may assume that, for a MOSFET, $\lambda = 0$ and $\gamma = 0$.

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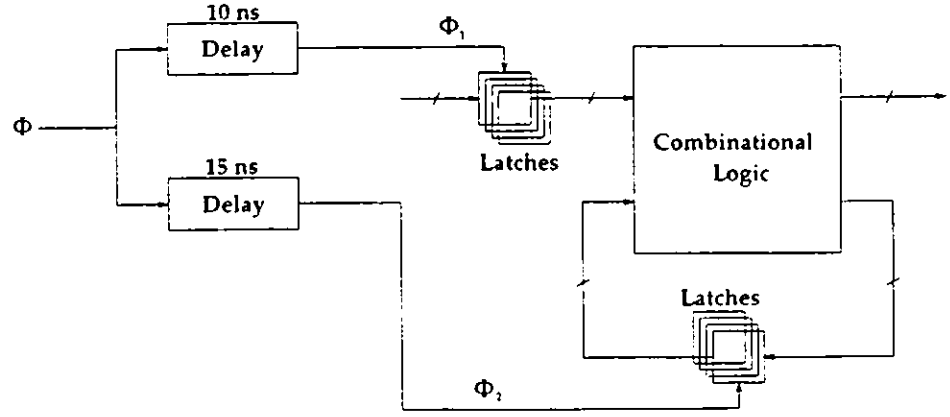
(Do not write in this area)

| Problem: | 1 | 2 | 3 | 4 | 5 | 6 | Total |
|---|---|---|---|---|---|---|---|
| Maximum: | 15 | 10 | 20 | 20 | 15 | 20 | 100 |
| Score: | | | | | | | |

1. (15 points) A single-transistor DRAM cell with a total storage capacitance of 10 fF is refreshed at a frequency of 1 MHz and operates on a 5 V power supply. The *read* circuitry is designed to detect if the voltage stored in the cell at the start of the read operation was less than or greater than $V_{dd}/2$. Due to processing variations, the cell leakage current when it is storing a logic 1 (i.e., 5 V) is known to be *uniformly distributed* between 10 nA and 40 nA. You may neglect leakage when the cell is storing a logic 0. Give a rough estimate of the *cell yield*, i.e., the expected percentage of cells that will work reliably.

2. (10 points) Consider the following block diagram of a sequential logic circuit in which the delay of the combinational logic block is 30 ns $\leq \tau_C \leq$ 95 ns. The latches are all **transparent** and are active (i.e., transparent) on the high clock signal. You may assume that the latches all have zero setup time, zero hold time, and zero delay. You may also assume that the inputs to the latches driven by $\Phi_1$ change only at the same time at which $\Phi_1$ goes high.



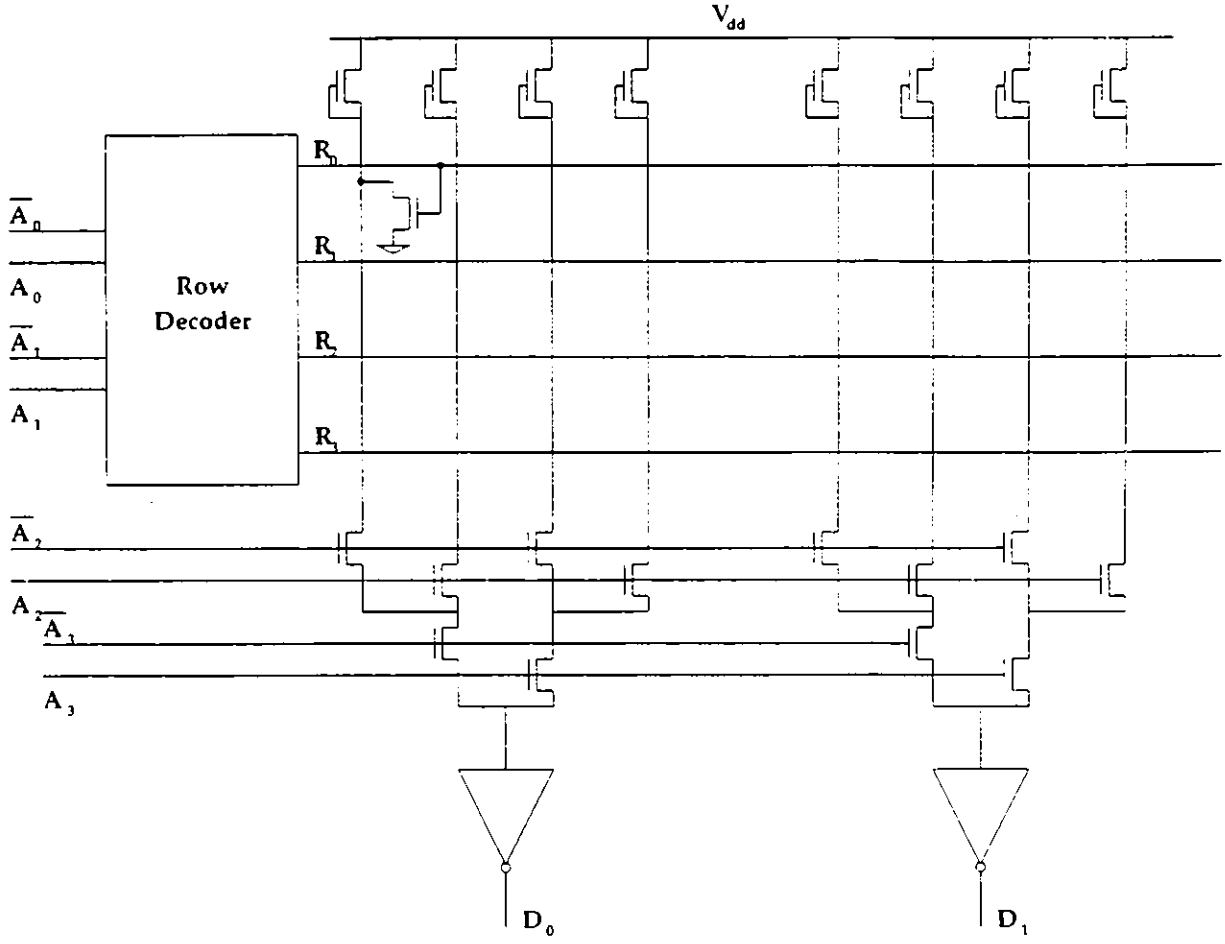

2.1 (5 points) Find the maximum clock frequency for which this circuit will work reliably.

2.2 (5 points) Find the maximum clock duty cycle for which this circuit will work reliably.

3. (20 points) This is an incomplete design of a static ROM, in which the row decoder is a static NOR-based design. For illustration, one cell of the array is shown already programmed.

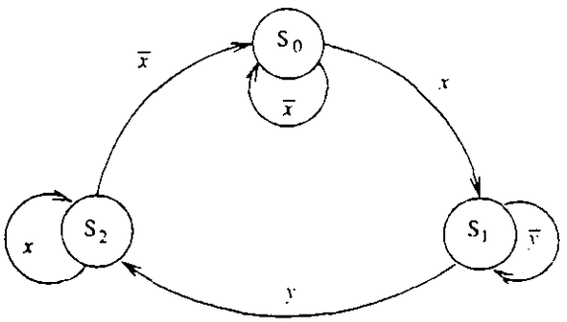
   3.1 (15 points) Complete the programming of the NOR ROM array in order to implement the memory map shown in the table below.

   3.2 (5 points) Show how the row decoder is to be designed so as to be consistent with your design.




| $[A_3A_2A_1A_0] =$ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $D_0 =$ | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| $D_1 =$ | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |

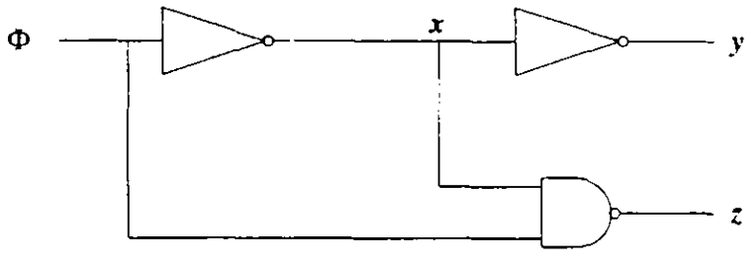
4. (20 points) We want to design a controller that implements the following state diagram. The controller has two input logic signals $x$ and $y$ and has one output logic signal $z$. The controller has three states as shown, and $z$ is required to be 1 when in state $S_2$ and 0 otherwise. We want to use the 1-hot encoding $S_0 = 001$, $S_1 = 010$, and $S_2 = 100$. Show an implementation of this controller using logic gates and D flip-flops.



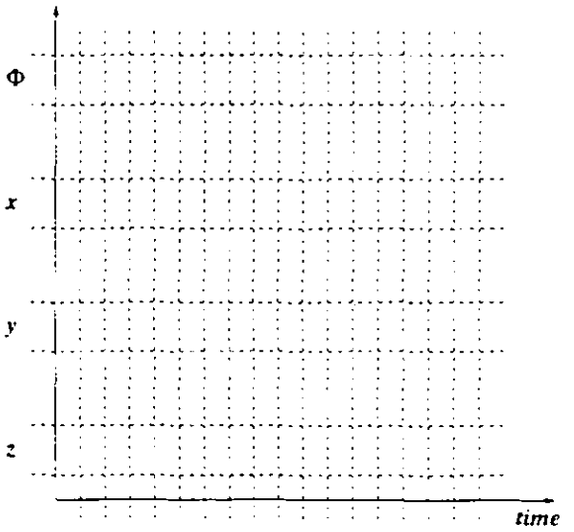
5. (15 points) Simplify the following PLA personality matrix by exploring the possibility of removing redundant rows. Show your work and explain your reasoning.

| | | | | | |
|---|---|---|---|---|---|
| 1 | 0 | 2 | | 1 | 1 |
| 2 | 0 | 0 | | 1 | 0 |
| 1 | 2 | 1 | | 1 | 1 |
| 2 | 2 | 0 | | 0 | 1 |

6. (20 points) In the following circuit, every logic gate has a *rising delay* of $\Delta_R = 1$ nsec (this is the gate delay when its output rises; it is *not* the rise-time) and a *falling delay* of $\Delta_F = 2$ nsec (this is the gate delay when its output falls; it is *not* the fall-time). In addition, the inverters have an *inertial delay* of $\Delta_I = 0.5$ nsec, and the NAND gate has $\Delta_I = 1.5$ nsec. You are also given that the input signal $\Phi$ is a 250 MHz clock with a 50% duty cycle. Assume all rise and fall times are zero.




6.1 (10 points) Using the grid at the right, show a plot of the signals $\Phi$, $x$, $y$, and $z$. Make sure to mark the time axis with time units.




6.2 (10 points) If every inverter has an output capacitance of 10 fF and the NAND gate has an output capacitance of 20 fF, find the average power dissipation of the whole circuit. You are given that $V_{dd} = 5$ V, and you may assume that the power consumed by a logic gate is due only to charging and discharging of its output capacitance.