University of Toronto

Faculty of Applied Science and Engineering

Final Examination

December 18, 2001

Duration: 2.5 hours

ECE435F - Digital Electronics
Examiner - J. Long

ANSWER ALL QUESTIONS ON THIS PAPER. USE EXTRA BOOKLETS IF NECESSARY. STATE ALL ASSUMPTIONS.

1. Formula sheet is allowed (single yellow sheet).
2. Calculator type is restricted (no programmable calculators).
3. Note that all questions are NOT weighted equally.
4. For all problems, assume the following transistor parameters unless otherwise specified:

NMOS: $V_{Tn} = 0.5V$, $k_n = \mu_n C_{ox} = 21\mu A/V^2$, $\lambda = 0$, $m_j = 0.5$, $\phi_j = 0.7$, $C_{ox} = 1fF/\mu m^2$, $C_{j0} = 1.8e\text{-}4F/m^2$, $C_{jsw0} = 5e\text{-}10F/m$, $C_{ov} = 0.33C_g$

PMOS: $V_{Tp} = -0.5V$, $k_p = \mu_p C_{ox} = 6\mu A/V^2$, $\lambda = 0$ $m_j = 0.5$, $\phi_j = 0.7$, $C_{ox} = 1fF/\mu m^2$, $C_{j0} = 3.5e\text{-}4F/m^2$, $C_{jsw0} = 7e\text{-}10F/m$, $C_{ov} = 0.33C_g$

Last Name: _____

First Name: _____

Student#: _____

Question	Mark
1	
2	
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4	
5	
Total	

(maximum grade = 100)

1. For the master/slave D-type CMOS flip-flop shown in Fig. 1:

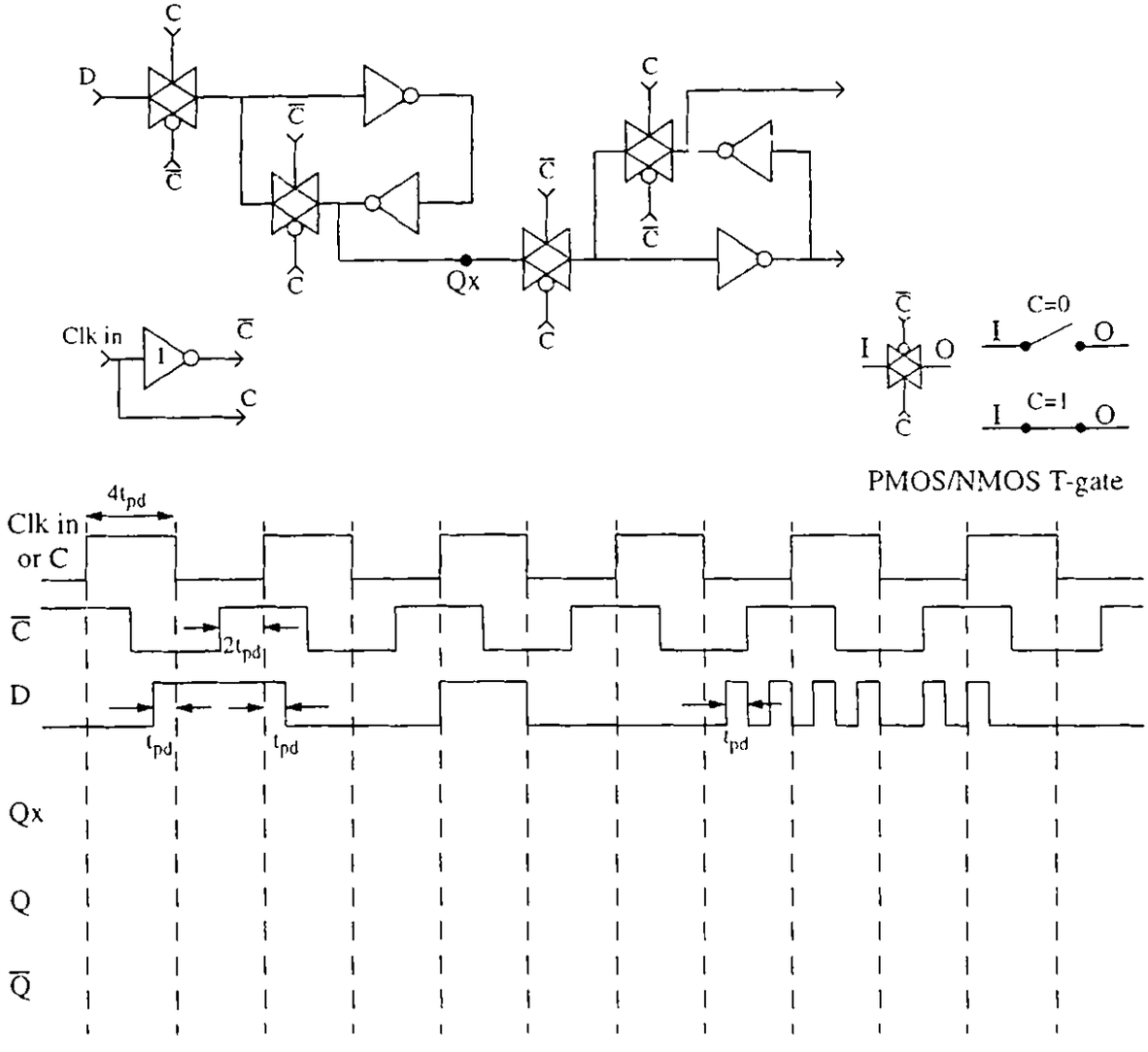

Figure 1: D-type flip-flop.

[5] a) Label outputs Q and $\overline{Q}$. Is the circuit triggered by the rising or falling edge of Clk in?

[10] b) Clock inverter #1 is heavily loaded and has a propagation delay time of 2tpd. Sketch the waveforms at node Qx, Q and $\overline{Q}$ in response to the Clk-in and D input waveforms of Fig. 1, assuming that all other inverters (except #1) and transmission gates have a propagation delay time of t_{pd}. Assume that the initial state of the flip-flop is Q=0, $\overline{Q}$=1.

[5] c) Assuming that all inverters and transmission gates have a loaded propagation delay time of t_{pd} , express the maximum clock frequency in toggle mode (i.e., for D connected to $\overline{Q}$) in terms of t_{pd}.

[5] d) Sketch the output waveforms at C and $\overline{C}$ of the clock generator shown in Fig. 2 assuming a square-wave input and loaded delay of t_{pd} for each gate. How would the flip-flop performance be improved if this clock generator were substituted for the clocking scheme shown in Fig. 1?

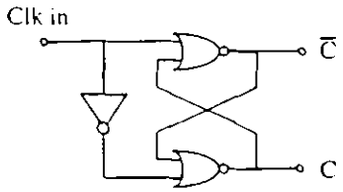

Figure 2: Clock generator.

[25] 2. Design a CMOS gate which implements the logic function $F = \overline{C(A+B+C) + (DEF)}$ with a worst case (unloaded) propagation delay of 100ps. Use a resistor approximation for the FET. Ignore the body effect, sidewall component and non-linearity of the diffusion capacitance. However, area component of the diffusion and gate-oxide (including overlap) capacitances must be accounted for. Assume that the S/D diffusion is Wx1μm, where W is the transistor width. Minimum gate length is 0.35μm.

3. A one-transistor DRAM cell is implemented using a polysilicon storage capacitor as shown in Fig. 3. Ignore parasitics for any portion of the layout outside the $6x6\mu m^2$ unit cell.

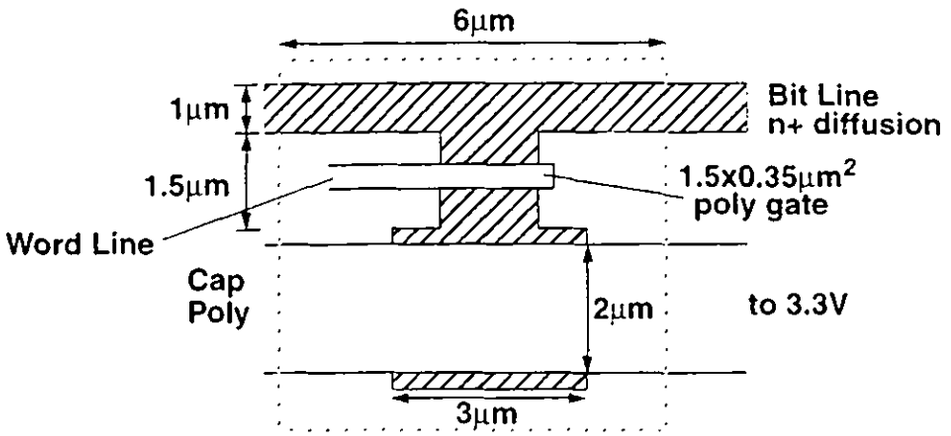

Figure 3: 1-T DRAM cell.

[5] a) Sketch the circuit schematic for the cell.

[5] b) Determine capacitances of the storage cap and bit line for the unit cell at zero bias. Assume $C_{ox} = 1fF/\mu m^2$ for the storage cap.

[5] c) Determine the stored charge when a "1" is written by applying 3.3V to the bit line and poly gate (i.e., word line), and when a "0" is written by grounding the bit line with 3.3V applied to the gate.

[5] d) What is the bit line voltage when reading a "1" and reading a "0"?

4. An ECL gate is shown below. Assuming that $\beta_F = 80$ and $V_{be} = 0.85V$, determine the following (please state all assumptions clearly).

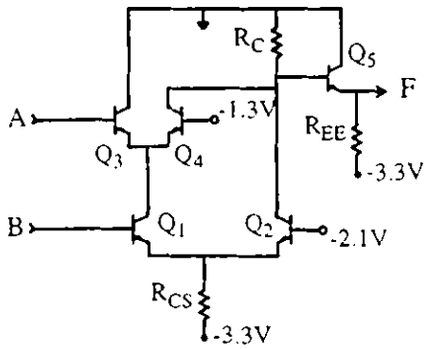

Figure 4: ECL gate.

[2] a) A Boolean expression for the output (F) in terms of inputs A and B.

[5] b) Values for resistors R_{CS} and R_C so that $V_{OH} = -0.85V$ and $V_{OL} = -1.85V$

[5] c) R_{EE} so that a series termination resistor of 33Ω will match the output to a 50Ω coaxial cable when the output is "0".

[3] d) What is the maximum power dissipated by this gate?

5. A CMOS gate is used to drive the interconnecting cable between two shelves of datacomm equipment in router, as shown below.

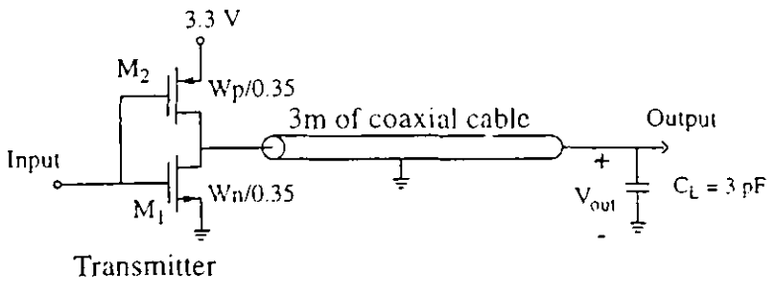

Figure 5: CMOS interface.

[3] a) Which termination is most appropriate for a CMOS gate: a series or parallel termination at the transmit end, or a series or parallel termination at the receive end of the cable? Why?

[8] b) Size the buffer to minimize the propagation delay time of the buffer, given that the cable has 0.4pF/m capacitance and power dissipation must be kept below 100mW.

[4] c) What is maximum rate of data transfer through the resulting link? Suggest a modification which could improve the data rate.