**Print:**
First Name:. ..... Last Name:. .....

Student Number:. .....

# University of Toronto
# Faculty of Applied Science and Engineering

Final Examination – December 1999

ECE352F – Computer Organization

Examiner – Paul Chow

1. There are 5 questions and **11** pages. Do **all** questions. The total number of marks is 100.
2. **ALL WORK IS TO BE DONE ON THESE SHEETS!** Use the back of the pages if you need more space. Be sure to indicate clearly if your work continues elsewhere.
3. Please put your final solution in the appropriate spaces. A big space **does not** necessarily mean a long answer is required.
4. **No calculators or other computing devices allowed.**
5. **Paper Type D** – You may use a VHDL reference manual.
6. Place your student card on your desk

| | |
|---|---|
| 1 [20] | |
| 2 [20] | |
| 3 [15] | |
| 4 [20] | |
| 5 [25] | |
| Total [100] | |



1. The sum and carry bits of a full adder circuit are defined by the following equations:

$$S_i = \overline{x}_i\overline{y}_i c_i + \overline{x}_i y_i \overline{c}_i + x_i\overline{y}_i\overline{c}_i + x_i y_i c_i$$

$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$

[4 marks] (a) For a carry lookahead adder, what are the expressions for the *propagate* and *generate* functions $P_i$ and $G_i$?

$P_i =$

$G_i =$

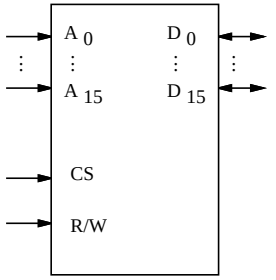
[4 marks] (b) What are the limitations of this scheme?

Question 1 continued...

[12 marks] (c) Using a diagram show how you would build a 16-bit adder using carry lookahead logic to minimize the delay, keeping in mind the limitations to this technique.



2. You have been asked to design a 1 megabyte (Mbyte) bank of static RAM using a number of 64K$\times$16 SRAM chips. The memory bus is to be 32-bits wide. The pinout for the memory chips is shown below:




[2 marks] (a) How many 64K$\times$16 memory chips are required to build the 1 Mbyte RAM bank?

Number of chips = _____

[2 marks] (b) How many address lines are needed for the 1 Mbyte RAM bank?

Number of address lines = _____

[2 marks] (c) One of the ways to characterize a memory is the bandwidth of the memory measured in Mbytes/s. This tells you the maximum rate that data can be transferred in or out of the memory. Assuming that the cycle time of the memory bank is 10 ns, what is the bandwidth of this memory bank? Explain how you arrived at your result.

Bandwidth (Mbytes/s) = _____

[2 marks] (d) Suggest how you could change the design of the memory bank to double the memory bandwidth while still using the same memory chips. Hint: This may require other changes in the system.

Question 2 continued...

[12 marks] (e) Show how to build the 32-bit bus, 1 Mbyte memory bank using the 64K×16 chips. If you need extra logic, assume that you have some PAL chips available to program. Give the logic equations that describe the logic to be programmed into the PAL. Provide enough information so that the design could be passed to a junior engineer who would implement the design.



3. (a) A processor has a 16 Kbyte, 2-way set-associative cache. Each block in the cache is 32-bytes. Addresses are 32 bits. Assume that a word is a byte.

[3 marks] i. How many bits are there in the tag, set, and word fields?

# tag bits = ____

# set bits = ____

# word bits = ____

[2 marks] ii. How many tag comparators are needed? How many bits are in each comparator? Explain.

# tag comparators = ____

# bits/comparator = ____

[10 marks] (b) Assume that you have a 2-way, set-associative cache with 8 words in the cache. The cache uses an LRU replacement policy. Complete the table below showing the addresses stored in the cache as the following sequence of addresses is accessed:

```
 4  5  6  7  8  9 11  5  6  9
 5  6  9 13 17 18 19 20 24 28
20 25 26 11 28 25 27
```

| | Set 0 | Set 1 |
|---|---|---|
| 0 | | |
| 1 | | |
| 2 | | |
| 3 | | |

What is the total number of cache misses assuming the cache was empty at the start?

# cache misses = ____

[7 marks] 4. (a) Show how a page table is used to convert a virtual address to a physical memory address.



Question 4 continued...

[7 marks] (b) Why is a TLB necessary? Show how a TLB is used to do the address translation.

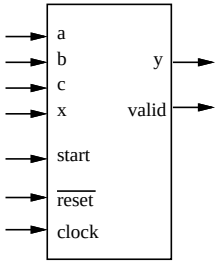
[6 marks] (c) In a multi-user system, virtual memory provides a mechanism for protecting one user process from another user process. Explain.

5. Your first project as design engineer at a new ASIC design house is to build a **pipelined** hardware unit to compute the function:

$$y = |ax^2| + |bx| + c$$

This means that on every rising clock edge you can accept a new set of inputs for $a$, $b$, $c$, and $x$. Note that the expression uses the absolute values of the first two terms in the expression. You have adder/subtractors and multipliers available in your library of function blocks.

The signals on the chip are shown below:




The asynchronous **reset** signal resets the circuit when it is set low. The **start** signal is set high for the first set of valid inputs.

[2 marks] (a) What is the use of the **valid** signal at the output? Hint: You may want to do the next part of the question first.



Question 5 continued...

[8 marks] (b) Draw a block-level diagram of your circuit. Clearly show all functional units and registers required. Minimize the latency of your circuit. Latency is measured as the number of cycles from input to output.

[2 marks] (c) What is the latency of your circuit in clock cycles?

latency =

[2 marks] (d) Assuming that the multipliers take 20 ns and the adders take 5 ns, what is the minimum clock period for your circuit?

clock period =

Question 5 continued...

[11 marks] (e) Write a VHDL program for your circuit assuming that all datapaths are 16-bits wide using 2's complement numbers. You need not be overly concerned with syntax. Grading will be based mostly on the structure of your program, how it corresponds to your block diagram, and the efficiency of your hardware utilization.