University of Toronto

Faculty of Applied Science and Engineering

Department of Electrical and Computer Engineering

FINAL EXAMINATION, APRIL 2001

Third Year - Program: Electrical Engineering

ECE 331S - ELECTRONIC CIRCUITS

Exam Type: D

Examiner: Anas A. Hamoui

❑ **INSTRUCTIONS/NOTES:**

- A BJT Aid Sheet and a MOSFET Aid Sheet are attached.
- Four double-sided OR eight single-sided 8.5"x11" additional aid sheets are allowed. These aid-sheets must be **hand-written**.
- All types of calculators are permitted.
- **Answer all questions in the space provided on the exam pages.** You may use the back of the sheet to continue your answers. Underline your answers.
- For full credit, you must show the **steps** you followed to answer the questions and you must clearly indicate the **units** in your answers.
- State any assumptions you find *necessary* to complete your answers.
- Write your last name on the top of ALL pages following this sheet.

Name: _____ **Student ID:** _____

Question	Mark
1	/25
2	/25
3	/25
4	/25
Total	/100

DEVICE PARAMETERS

❑ **MOSFET Parameters:**

For a MOSFET in the saturation region and having $L = 0.5\mu m$:

	NMOS Transistor	PMOS Transistor
V_t	0.6 V	0.65 V
λ	0.25 V^{-1}	0.40 V^{-1}
μC_{ox}	200 $\mu A/V^2$	50 $\mu A/V^2$
C_{ox}	5 $fF/\mu m^2$	5 $fF/\mu m^2$
$L_{ov}C_{ox}$	0.625 $fF/\mu m$	0.625 $fF/\mu m$

❑ **BJT Parameters:**

	npn Transistor	pnp Transistor
$\lvert V_{BEon}\rvert$	0.7 V	0.7 V
$\lvert V_{CEsat}\rvert$	0.3 V	0.3 V
$\beta = h_{fe}$	120	50
C_μ	5 fF	15 fF
r_x	400 Ω	200 Ω
$\lvert V_A\rvert$	35 V	30 V
V_T	25 mV	25 mV

❑ **Note:** $1\ fF = 10^{-3}\ pF = 10^{-15}\ F$

Specifications

I_{ref} = 50 μA

$W_1 = W_2$ = 128 μm

$W_3 = W_4$ = 8 μm

W_5 = 16 μm

$W_6 = W_7$ = 64 μm

W_8 = 16 μm

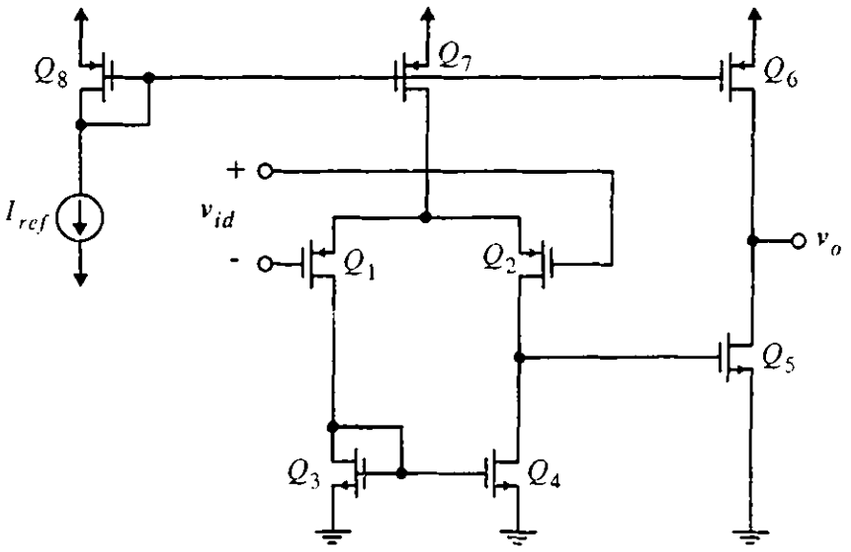

Fig. 1

Question 1: [25 marks]

Fig. 1 shows a popular architecture of CMOS op-amps known as the 2-stage configuration. The **first gain stage** consists of the differential pair Q_1-Q_2 which is actively loaded with the current mirror Q_3-Q_4. The **second gain stage** consists of the common-source amplifier Q_5 which is actively loaded with the current-source transistor Q_6. A reference bias current I_{ref} is replicated using the simple current mirror formed by Q_8-Q_7 and Q_8-Q_6 to provide the dc bias currents for the gain stages.

Assume all transistors are in saturation and have a channel length L = 0.5 μm. Furthermore, assume the current source I_{ref} is ideal. The MOSFET parameters are listed on page 2. Ignore the body effect. In the dc analysis, neglect the channel-length modulation effect.

Find the differential voltage gain v_o / v_{id}.

LAST NAME:

Answer Sheet for Question 1

Specifications

R_S = 10 $k\Omega$

R_L = 10 $k\Omega$

C_L = 0.75 pF

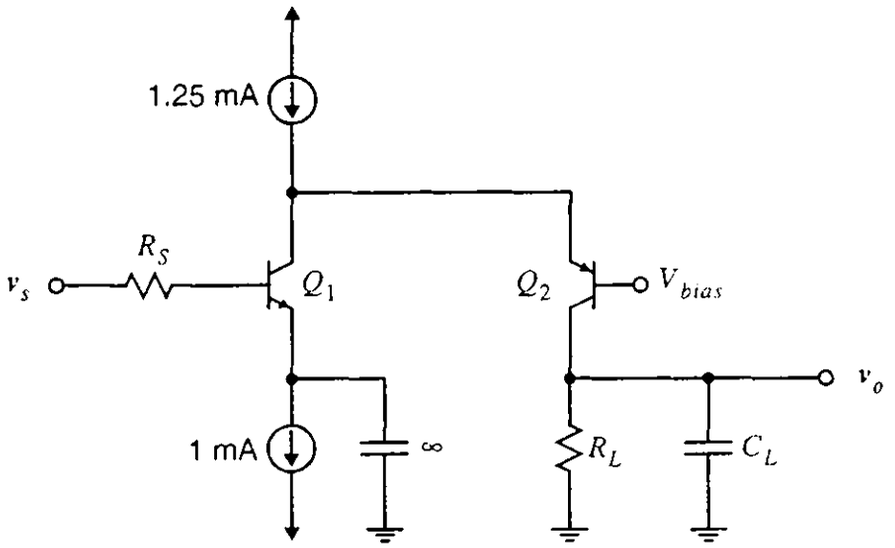

Fig. 2

Question 2: [25 marks]

In the folded-cascode amplifier circuit shown above, assume all transistors are biased in the active mode. Furthermore, assume the current sources are ideal. The BJT parameters are listed on page 2. The unity-gain bandwidths of Q_1 and Q_2 are f_{T1} = 15.5 GHz and f_{T2} = 245 MHz, respectively. To simplify the analysis, ignore the base resistance r_x and the output resistance r_o of Q_1 and Q_2. In the dc analysis, neglect the base current of every transistor.

a) Find the voltage gain v_o/v_s at midband frequencies.

b) Estimate:

i) the frequencies of the **two** lowest-frequency poles of the voltage transfer function.

ii) the gain-bandwidth product of the amplifier.

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Answer Sheet for Question 2

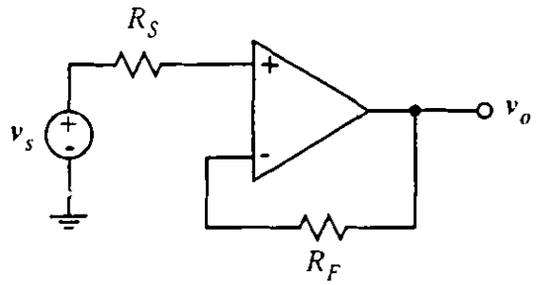

Fig. 3

Question 3: [25 marks]

a) In the series-shunt feedback amplifier circuit shown in **Fig. 3**, assume the signal source v_s has a zero dc component and the op-amp is ideal. Show that the dc voltage at the output is zero and find the small-signal closed-loop gain v_o/v_s.

b) The series-shunt feedback amplifier in Fig. 3 is implemented as shown in Fig. 4.
For the series-shunt feedback amplifier in **Fig. 4**, assume the signal source v_s has a zero dc component and the bias voltage level at the output is stabilized by feedback to about 0 V. The BJT and MOSFET parameters are listed on page 2. In the dc analysis, ignore the base current of every BJT. The incremental output resistances of current sources I_C and I_D are 60 $k\Omega$ and 35 $k\Omega$, respectively. Current source I_{bias} is assumed to be ideal.
Use feedback analysis to find:

- the feedback factor B
- the open-loop gain A
- the closed-loop gain $A_f \equiv v_o/v_s$
- the input resistance R_{in}
- the output resistance R_{out}

LAST NAME:

Specifications

$I_{bias} = 1\ mA$

$I_C = 0.5\ mA$

$I_D = 1\ mA$

$R_S = 5\ k\Omega$

$R_F = 5\ k\Omega$

$R_L = 2\ k\Omega$

$\left(\frac{W}{L}\right)_3 = \frac{80\mu m}{0.5\mu m}$

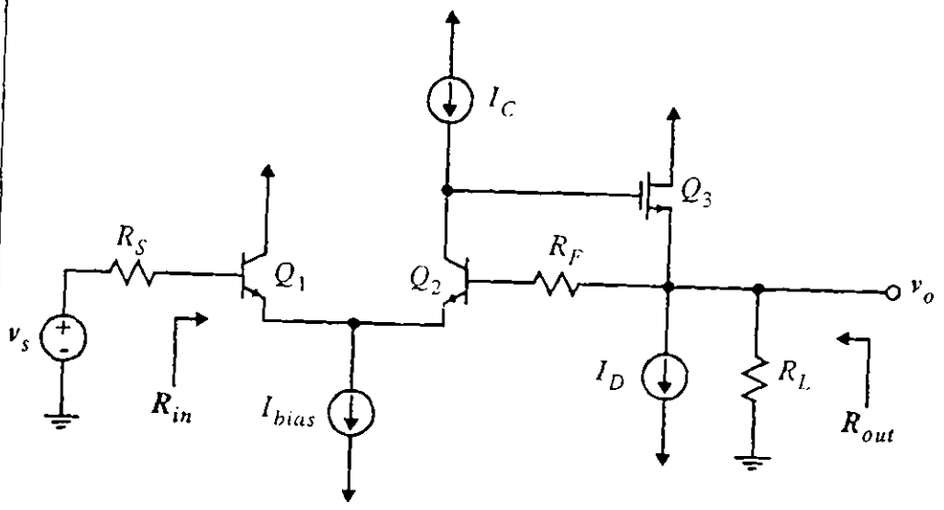

Fig. 4

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Answer Sheet for Question 3

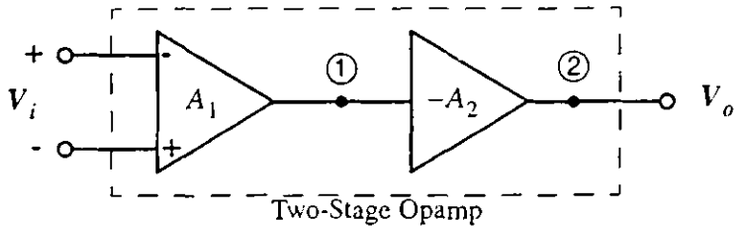


Fig. 5

Question 4: [25 marks]

Consider the two-stage op-amp shown in Fig. 5. The open-loop transfer function $A(s) = V_o(s)/V_i(s)$ has a dc gain of 80 dB and poles at $f_{p1} = 10^4$ Hz, $f_{p2} = 10^5$ Hz, and $f_{p3} = 10^6$ Hz. The **first pole (at f_{p1})** is formed at node 1 and the **second pole (at f_{p2})** is formed at node 2. The op-amp is connected in a negative-feedback loop via a feedback network whose feedback factor B is frequency independent.

a) Sketch the Bode plots for the magnitude and phase response of the open-loop transfer-function A. *Use the graph on page 12.*

b) Find the value of B for which a phase margin of 45^o is obtained and the corresponding gain margin.

c) It is required to compensate the op-amp so that it is stable with a phase margin of 45^o for a dc closed-loop gain of 20dB. Consider the following three compensation schemes:

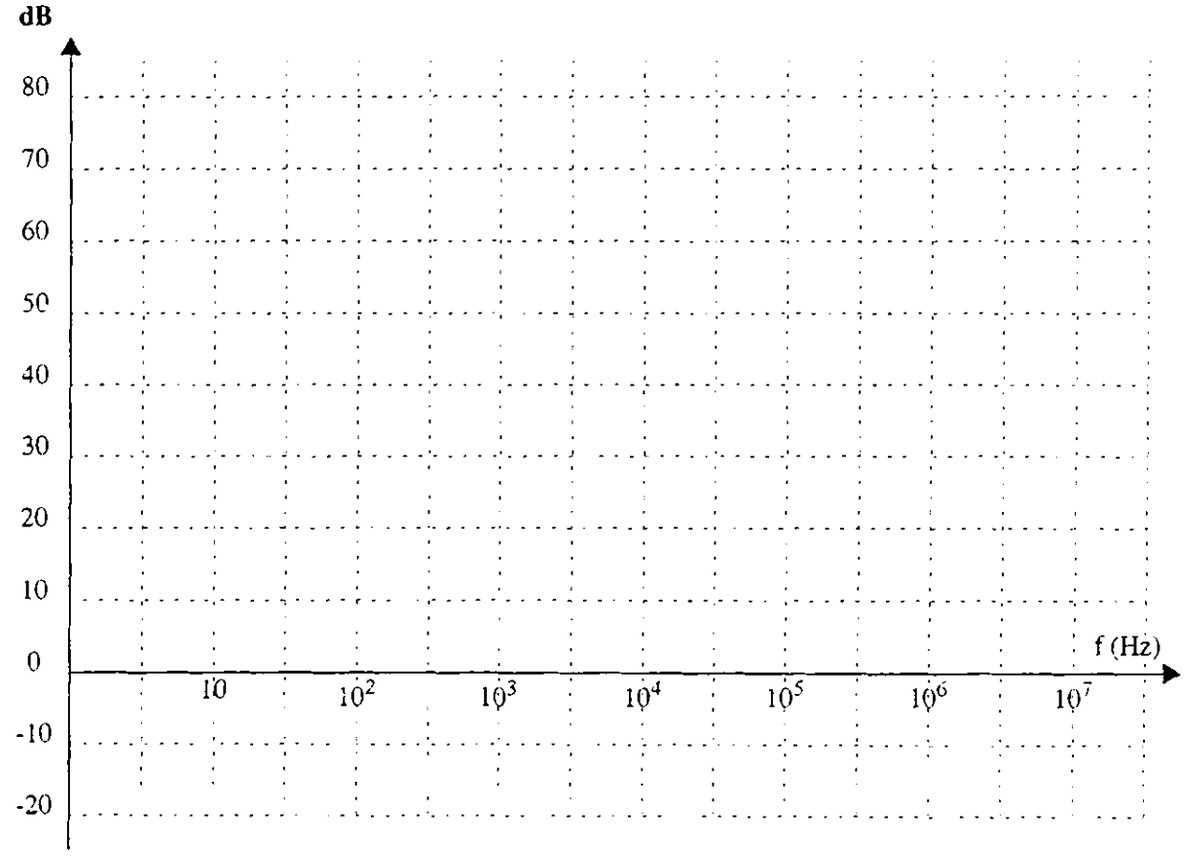
   i) **Compensation Scheme 1:** the op-amp is compensated by introducing a new dominant pole.
      - Find the frequency at which the new pole must be placed.
      - Sketch the Bode plots of the magnitude and phase response of the corresponding open-loop transfer-function and label it A'. *Use the graph on page 12.*

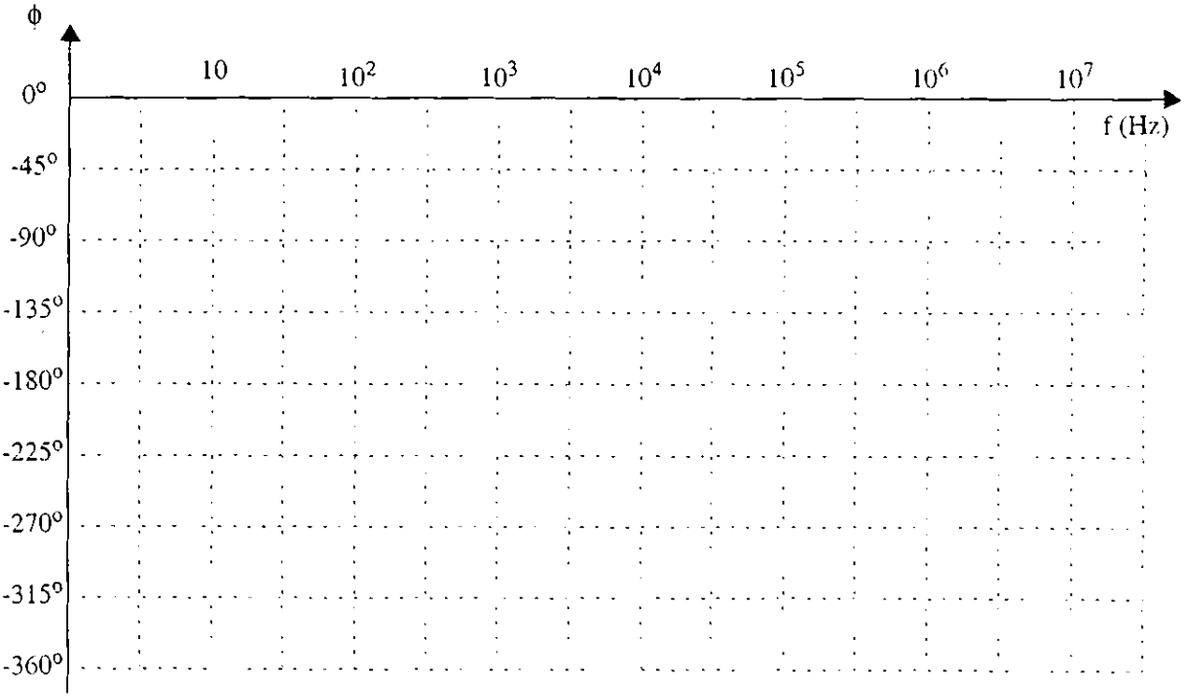
   ii) **Compensation Scheme 2:** the op-amp is compensated by placing an additional capacitance C_C at node 1 to reduce the frequency of the first pole. Assume the frequencies of the other poles remain unchanged.
      - Find the frequency to which the first pole must be shifted.
      - Find the factor by which the capacitance at node 1 must be increased.

iii) **Compensation Scheme 3:** the op-amp is to be compensated by connecting a compensating capacitor C_C between nodes 1 and 2.

- State whether a smaller or larger capacitance C_C would be required compared to the compensation scheme in part ii) above.
- State the effect of this frequency compensation scheme on the second-pole frequency and on the zeros of the open-loop transfer function.

Graph for Question 4





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Answer Sheet for Question 4

LAST NAME:

Additional Answer Sheet

Clearly indicate the question number for the questions you are answering on this sheet.

LAST NAME:

Additional Answer Sheet

Clearly indicate the question number for the questions you are answering on this sheet.

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Additional Graph for Rough Work

If you want this graph to be marked as part of Question 4, you MUST cross out the graph on page 12.