University of Toronto
Faculty of Applied Science and Engineering

Final Examination

December 20, 2001
Duration: 150 minutes

ECE334F - Digital Electronics
Examiners: Ali Sheikholeslami, Jianwen Zhu, and Rafik Guindi

ANSWER QUESTIONS ON THESE SHEETS, USING THE BACKS IF NECESSARY.

1. Calculator type is restricted (no programmable calculators).
2. Weight for each question is indicated in []. Attempt all questions, since a blank sheet will certainly get a zero.
3. Unless stated otherwise, for all problems, assume the following transistor parameters:

C_{ox} = 2 fF/μm^2, $C_{j\text{-}ave}$ = 0.4 fF/μm^2, $C_{jsw\text{-}ave}$ = 0.3 fF/μm

NMOS: V_{Tn0} = 0.6 V, $\mu_n C_{ox}$ = 90 $\mu A/V^2$, λ = 0, γ = 0 $V^{1/2}$

PMOS: V_{Tp0} = -0.6 V, $\mu_p C_{ox}$ = 30 $\mu A/V^2$, λ = 0, γ = 0 $V^{1/2}$

4. Happy Holidays.

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maximum grade = 100

Last Name: _____

First Name: _____

Student Number: _____

Lecture Section:

Ali Sheikholeslami ☐

Jianwen Zhu ☐

Rafik Guindi ☐

Question	Mark
1	
2	
3	
4	
5	
Total	

1. [15 marks] Circle T (for True) or F (for False) in statements below.

IMPORTANT NOTE: For each question, right answer gets "1", wrong answer gets "-1", no answer (no circle) gets "0".

T F Field oxide is often thinner than gate oxide in the same CMOS technology.

T F A 2-input NAND gate is designed to have the same worst-case rise and fall times. If the two inputs are shorted together, the resultant inverter will have a V_{TH} larger than $V_{DD}/2$.

T F A 2-input NOR gate is designed to have the same worst-case rise and fall times. The best-case fall time is smaller than the best-case rise time in this gate.

T F Consider a stack of n NMOS transistors in series, with the bottom transistor M_1 and the top transistor M_n. Assume all gates are at V_{DD}, the source of M_1 is at 0V, and the drain of M_n is at V_{DD}. The V_{DS} of M_i is larger than the V_{DS} of M_j if $i > j$, for all i & j.

T F Body effect causes the saturation current of an NMOS transistor to increase when its drain-to-source voltage is increased.

T F The voltage across a capacitor can jump instantaneously if one of its plates is floating.

T F As the input rise time decreases, the direct-path power consumption in a CMOS inverter becomes less significant compared to its dynamic power consumption.

T F The oscillation frequency of a ring oscillator made of identical inverters is linearly proportional to the number of inverters in the ring.

T F The dynamic power consumed in a ring oscillator made of three minimum-sized inverters is independent of the load capacitance it drives.

T F A chain of identical, minimum-sized, inverters could achieve an overall delay smaller than that of a single minimum-sized inverter (assuming both drive the same load capacitance).

T F SRAMs are generally faster than DRAMs because SRAMs allow simultaneous access to several wordlines.

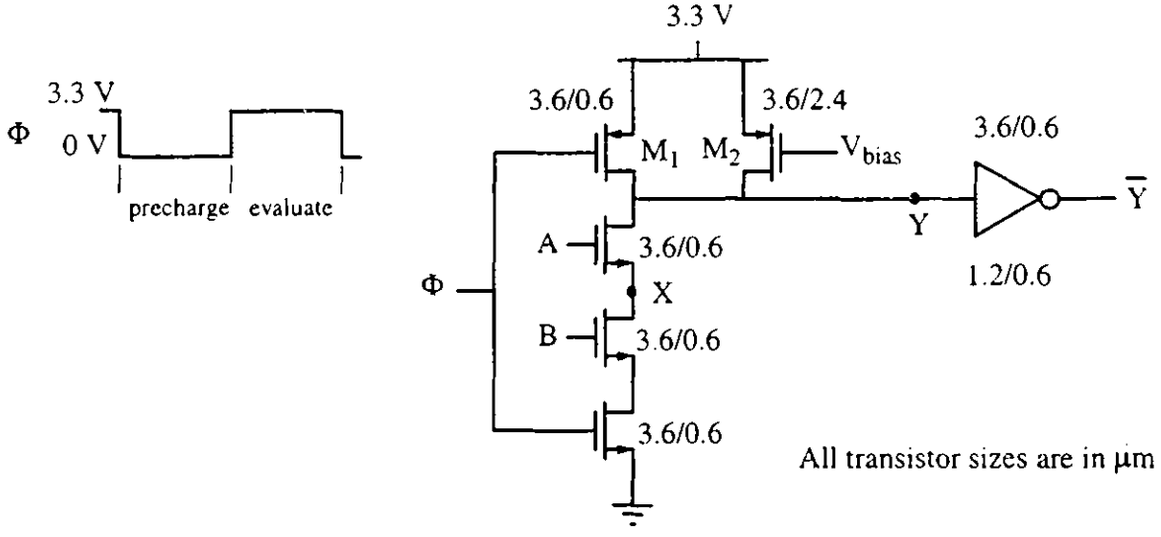
T F A preferred voltage value for the bottom plate of a cell capacitor in DRAM is $V_{DD}/2$.

T F The folded-bitline architecture is less sensitive to bitline coupling noise compared to the open-bitline architecture.

T F A read in DRAM must be followed by a write-back since read is destructive.

T F DRAM cells need to be periodically refreshed because the charge on the cell capacitor leaks through "the reverse-biased junction of the access transistors".

2. [25 marks] A "dynamic logic gate" is shown in the following figure. During the precharge phase of the clock Φ, node Y is precharged to V_{DD} through transistor M_1, while inputs A and B are maintained at 0 V. During the evaluation phase, logic values of A and B are applied. The voltage at node Y either stays at V_{DD} or drops in value depending on the logic combinations of inputs A and B. The voltage value of Y at the end of the evaluation phase determines the logic output of the gate. The function of transistor M_2 will be determined through the questions below.



(a) [4] Calculate the total parasitic capacitance at node X and at node Y. Assume M_1 and M_2 share one junction. Assume also that the NMOS transistors have shared junctions. The technology used is 0.6μm CMOS.

(b) [6] Given V_{bias} = 3.3V, find the voltage of node Y at the end of the evaluation phase for all different combinations of inputs. Substantiate the answers that you write in the table.

(V_{bias} = 3.3 V)

A	B	Voltage (Y)	why?
0 V	0 V		
0 V	3.3V		
3.3V	0 V		
3.3V	3.3V		

(c) [6] Repeat part (b) with V_{bias} = 0 V. Substantiate the answers that you write in the table.

(V_{bias} = 0V)

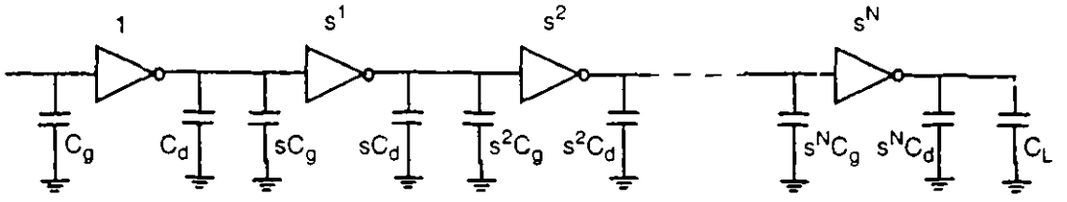
A	B	Voltage (Y)	why?
0 V	0 V		
0 V	3.3V		
3.3V	0 V		
3.3V	3.3V		

(d) [4] What is the advantage and the disadvantage of having transistor M_2 switched on? Your answers should fit in the space provided.

Advantage	Disadvantage

(e) [5] Will this circuit function properly if the output of the inverter ($\overline{Y}$) is directly connected to the gate of M_2 (V_{bias})? Explain in no more than two lines.

3. [20 marks] An inverter chain with N+1 stages is designed to minimize the delay in driving a load capacitance C_L. Assume the first stage is a minimum size inverter with equivalent driving resistance of R_{eq}, gate capacitance of C_g, and diffusion capacitance of C_d. Each inverter is a scaled version of its preceding stage.

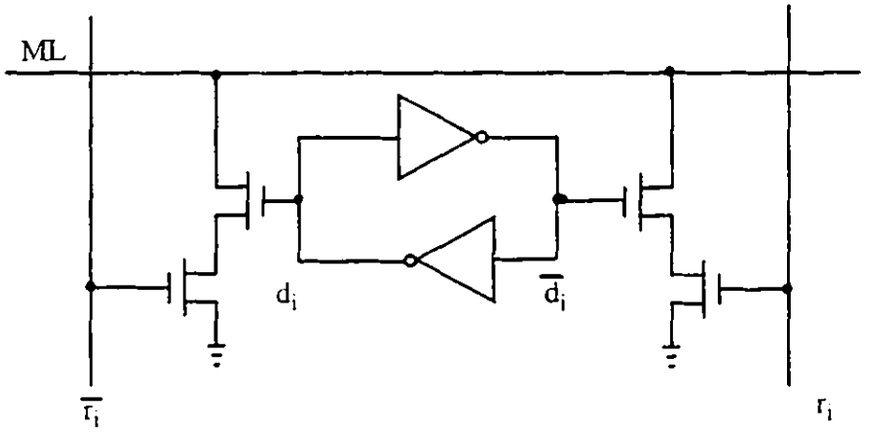


(a) [10] Derive a parametric equation that relates "s" to C_d and C_g. **Do not ignore C_d.**

(b) [6] Assuming C_L = 240fF, and the minimum size inverter has W_n = 0.75μm, W_p = 2.25μm, and $L_p = L_n$= 0.5μm, find the number of inverters in the chain and the scaling factor, s, to achieve the minimum delay. **Assume $C_d = 0$**. State any other assumptions you make.

(c) [4] Estimate the total delay for part (b). Assume $C_d = 0$.

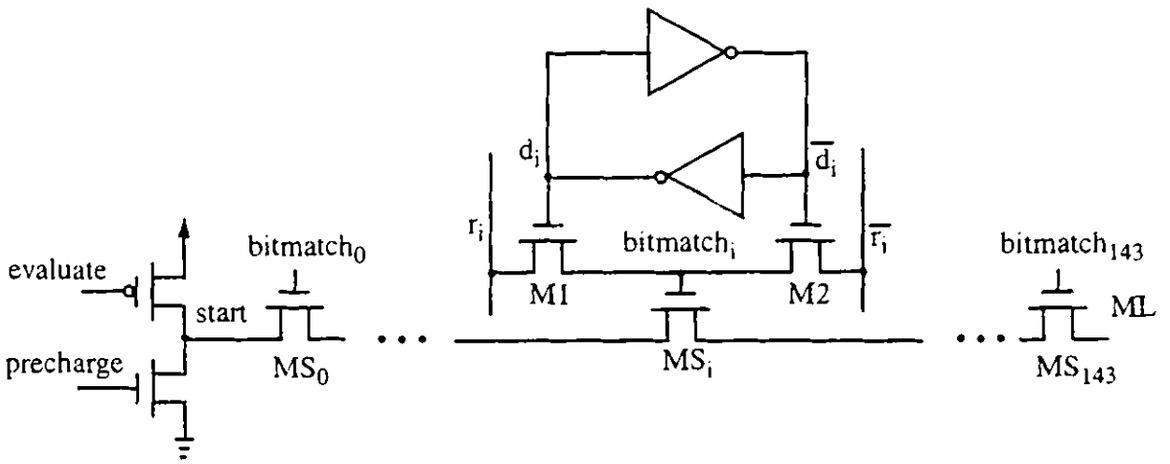
4. [20 marks] A NOR-based CAM, shown below without the SRAM access transistors, consists of a total of 256 words, each word being 144 bits. All NMOS transistors shown use $W_n = 1.0\mu m$, and minimum length $L_n = 0.5\mu m$.



(a) [8] Estimate the energy consumption in this CAM during a match operation that results in a single match. Assume the match operation begins and ends with $r_i = \overline{r_i} = 0V$. Assume $V_{DD} = 3.3V$. State any assumptions you make.

(b) [4] In case of a mismatch, approximate the **worst-case** 90%-to-10% fall time of the matchline.

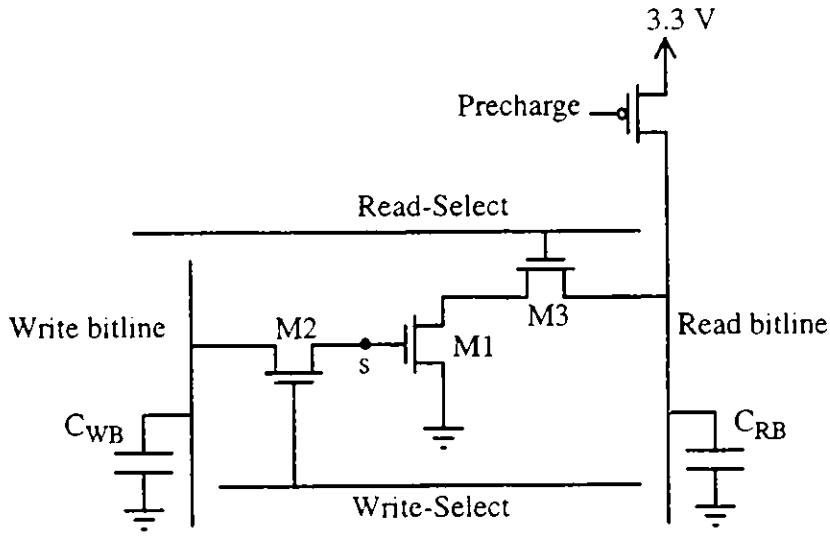
(c) [6] A NAND-based CAM is designed (as shown below) with a total of 256 words, each word having 144 bits. All NMOS transistors shown use $W_n = 1.0\mu m$ and minimum length $L_n = 0.5\mu m$.



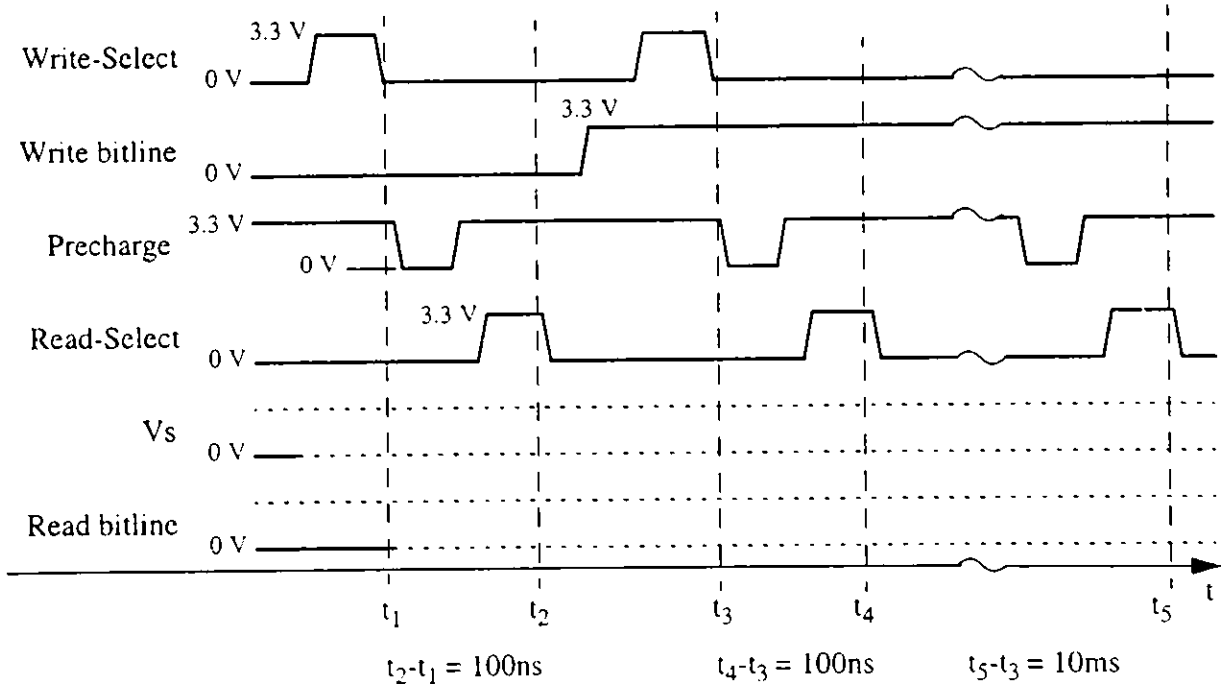
Assume all the MLs are precharged to ground during "precharge". Write an equation for the total energy dissipation in the CAM during "evaluate" if $d_i = r_i$ for $0 \le i \le (N-1)$ for all words stored in the CAM, and $d_N = \bar{r}_N$ (also for all words). State other assumptions you make.

(d) [2] What N minimizes the energy calculated in Part (d)?

5. [20 marks] The circuit shown is known as a three-transistor (3T) DRAM cell. The data is written through M2 on the gate capacitance of M1, assuming this gate capacitance dominates the total capacitance at node s. The stored data is read through M3. M1 has $(W/L)_1 = (25\mu m/0.6\mu m)$, and M2 and M3 have $(W/L)_{2,3} = (1.2\mu m/0.6\mu m)$. Assume the charge stored at node "s" leaks to ground at a steady current of 7.5 pA. Ignore body effect.



Study the following timing diagram and answer the following questions. You will be asked later to complete the missing waveforms for Vs and Read bitline.



(a) [2] What is the voltage at node s (Vs) at $t = t_1$?

(b) [2] What is Vs at $t = t_3$?

(c) [2] What is the voltage of the Read bitline (V_{RB}) at $t = t_2$?

(d) [2] What is V_{RB} at $t = t_4$.

(e) [5] Calculate Vs at $t = t_5$. Note that $t_5 - t_3 = 10$ms.

(f) [2] What is V_{RB} at $t = t_5$.

(g) [1] Is the readout operation destructive? (Yes / No)

(h) [1] Does the data in the cell need to be refreshed? (Yes / No)

(i) [3] Go back to the timing diagram, and draw the waveforms for the voltage Vs and the Read bitline. Clearly mark the voltage levels on the graph. Your waveforms must be consistent with your answers in parts (a) to (f) above.