Name: _____

University of Toronto

Faculty of Applied Science and Engineering

FINAL EXAMINATION, DECEMBER 2001

4th Year, Programs 5, 7

ECE534F, Integrated Circuit Engineering

Examiner: C.A.T. Salama

NO AIDS SHEETS ALLOWED; NON-PROGRAMMABLE CALCULATOR ALLOWED

(1) Answer all questions in the space provided on these sheets. **Do not unstaple sheets.**
(2) For bipolar transistors:

- NPN $\beta = 100$; $|V_{BE}| = 0.7V$; $|V_{CE}|_{sat} = 0.1V$; $r_o = \frac{100}{I_C}$
- PNP $\beta = 20$; $|V_{BE}| = 0.7V$; $|V_{CE}|_{sat} = 0.2V$; $r_o = \frac{100}{I_C}$

For all BJT's: $\frac{kT}{q} = 25mV$; $I_C = I_S\, e^{\frac{qV_{BE}}{kT}}$

(3) For MOSTs:

$$I_D = \frac{\mu CoZ}{2L}(V_G - V_T)^2;\ V_D \geq V_G - V_T$$

$$I_D = \frac{\mu CoZ}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right];\ V_D \leq V_G - V_T$$

- n channel $\mu Co = 20\ \mu A/V^2$; $V_T = +0.6V$; $r_O = \frac{5\times10^6 L}{I_D}$ (L in um, I_D in uA)
- p channel $\mu Co = 10\ \mu A/V^2$; $V_T = -0.6V$; $r_O = \frac{5\times10^6 L}{I_D}$ (L in um, I_D in uA)

Question	Maximum Mark*	Mark
1	12	
2	12	
3	18	
4	18	
TOTAL	60	

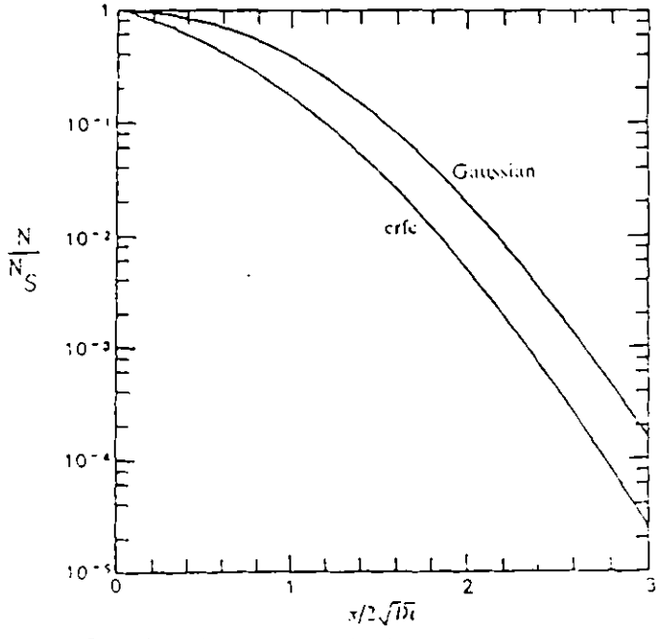
* Individual marks for each section are shown in [ ] brackets.

1. [6] (a) Design the diffusion process for the source and drain of an n-channel MOSFET given that:

- the required surface concentration = $10^{18}cm^{-3}$
- the required junction depth = 1um
- p-type substrate acceptor concentration = $5x10^{15}cm^{-3}$ boron
- deposition furnace temperature = 1000°C
- drive-in furnace temperature = 1100°C

Specify the deposition and drive-in times.
For Phosphorus

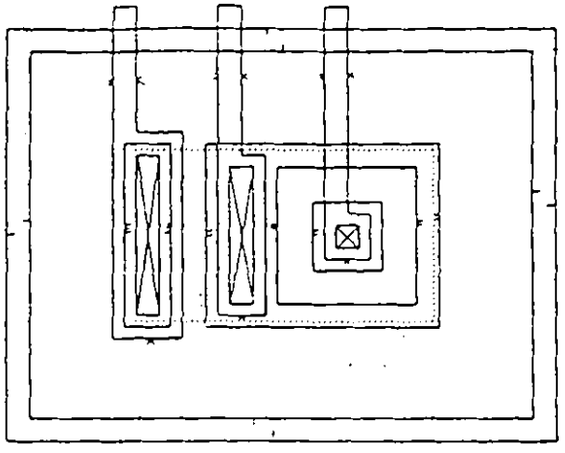
T(°C)	Solid Solubility	D cm^2/sec
1000	$3x10^{20}cm^{-3}$	$4x10^{-14}$
1100	$4x10^{20}cm^{-3}$	$81x10^{-14}$



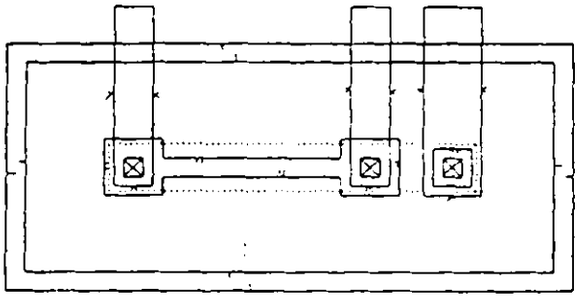
The diffusion functions: normalized concentration versus normalized distanc

erfc	N_s = const:	$Q(t) = -\frac{2}{\sqrt{\pi}}\sqrt{Dt}\,N_s$
Gaussian	Q = const;	$N_s(t) = -\frac{Q}{\sqrt{\pi Dt}}$

[3] (b) Consider the following layouts, identify in each case the component under consideration and draw a cross section for that particular component.



... buried layer
- isolation
= base
≡ emitter
x contact
> metal

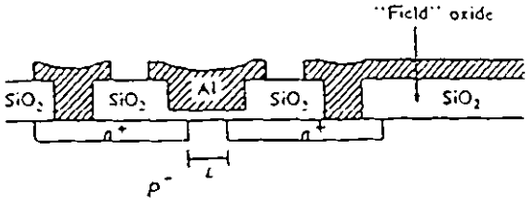


[3] (c) Are the following statements true or false?

	True	False
• Optical lithography can be used to define patterns below 0.1um.	☐	☐
• Ion implantation causes damage to the lattice of the semiconductor which must be annealed thermally.	☐	☐
• Silicon dioxide grown thermally on silicon passivates the semiconductor surface.	☐	☐
• The yield of an integrated circuit decreases exponentially with increasing area of the circuit.	☐	☐
• Bipolar IC technology requires junction isolation.	☐	☐
• Lateral pnp transistors can be used in the signal path without affecting the frequency performance of the circuit.	☐	☐

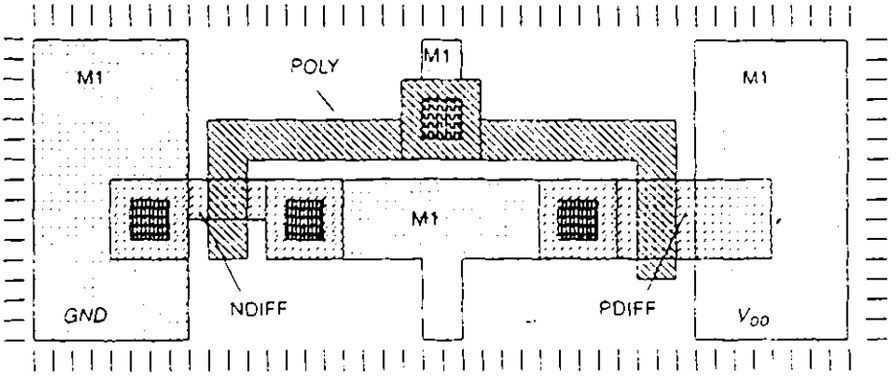
2. [4] (a) Consider the aluminum gate n-channel MOS transistor shown below. List three problems commonly encountered with this structure. What modifications to the process have been devised to solve these problems. Show the cross section of an optimized MOSFET including these modified features.

Problems



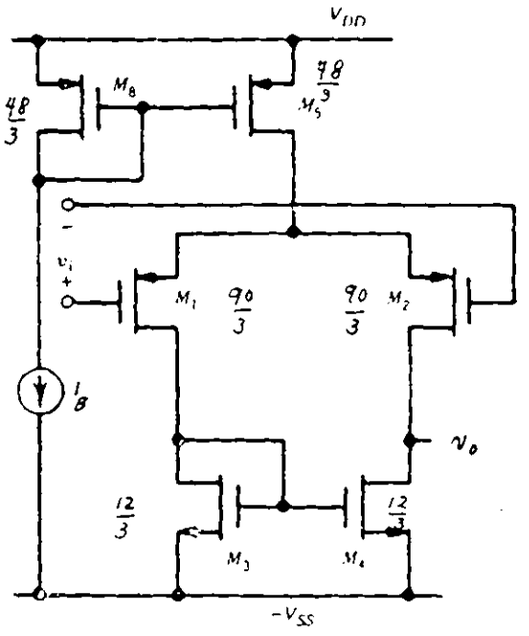
Process Modifications and Cross Section of Optimized MOSFET

[4] (b) The figure below shows a CMOS inverter layout containing several examples of either poor layout technique or design-rule violations. Find as many of these as possible and give a qualitative explanation of how each instance could be detrimental to the yield, functionality, or performance of the design. The layout is to scale and a one-lambda grid is provided in the figure.

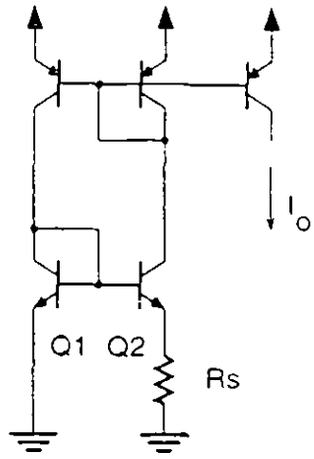


[4] (c) Consider the following CMOS differential amplifier:

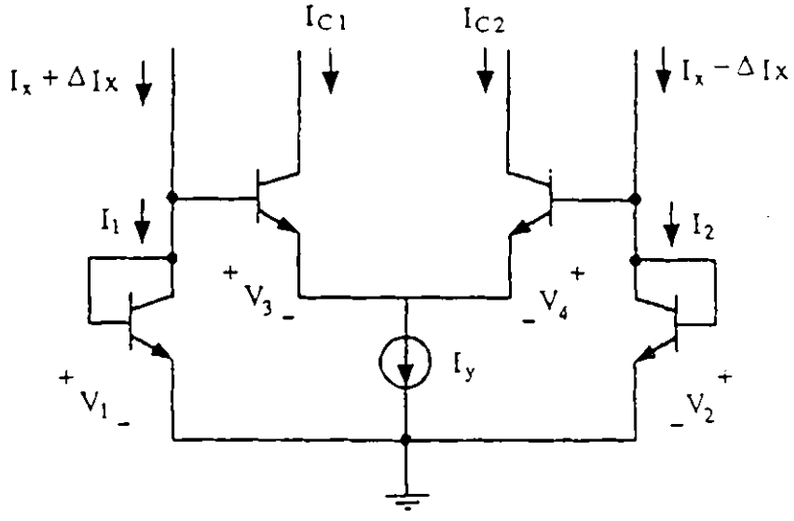
- Find an expression for the midband gain of the amplifier $A_{vo} = \frac{V_o}{V_i}$
- Calculate the gain for the specific case:
  $V_{DD} = 2.5V, V_{SS} = -2.5V$ and $I_B = 2.5uA$
- Suggest appropriate layout techniques to ensure that the amplifier is as perfectly balanced as possible.



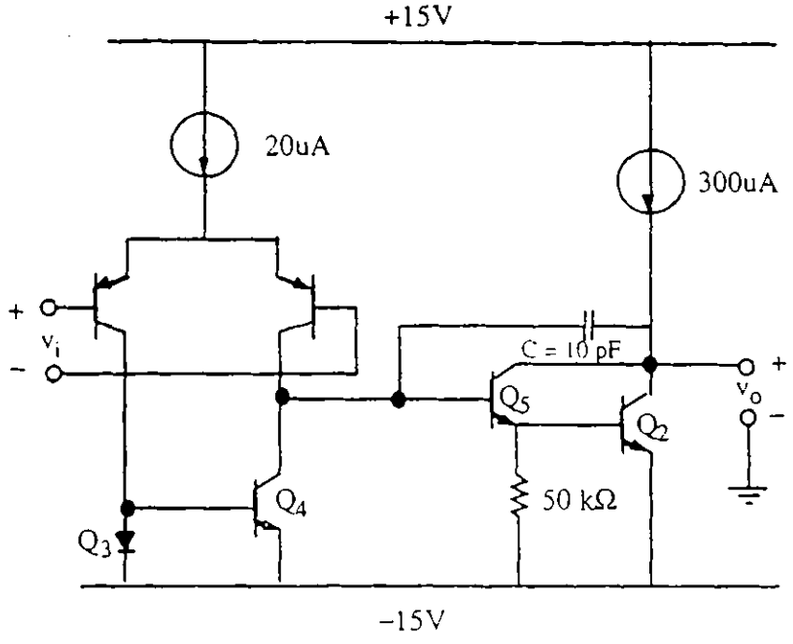
3. [4] (a) The following circuit is commonly used to generate an output current which is independent of supply voltage and is proportional to absolute temperature. Express the output current I_o in terms of the saturation currents I_{S1} and I_{S2} of Q_1 and Q_2 respectively and the resistor R_S.



[4] (b) The figure illustrates the principle of a proposed monolithic linearized two quadrant multiplier. Find (I_{C1} - I_{C2}) as a function of ΔI_x, I_x and I_y. Will this circuit work as a multiplier? Make any reasonable assumptions.



[10] (c) The circuit shown below represents the two input stages of an operational amplifier. Assuming the frequency response is dominated by a single pole, derive expressions for the midband gain A_{vo}, the unity gain bandwidth product w_u and the slew rate SR of the amplifier. Find numerical values for the midband gain, the unity gain bandwidth product and the slew rate.



$$A_{vo} = \frac{v_o}{v_i}$$

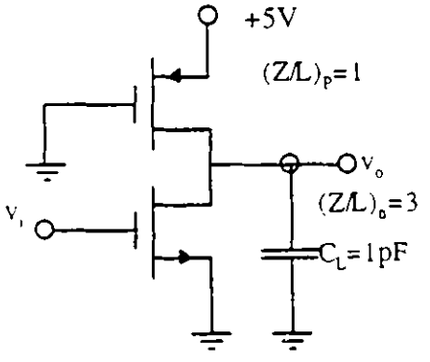
4. [6] (a) The CMOS gate configuration shown below is commonly used in memory address decoders. Derive:

a) Equations and numerical values for V_{OL}, V_{OH} and V_{LT} (where V_{LT} is the logic threshold voltage of the gate) associated with the transfer characteristics of the gate.

b) an equation for the delay associated with a low to high transition expressed in terms of the average current I_L from the supply, what is the numerical value of the delay.

c) an equation for the delay associated with a high to low transition expressed in terms of the on resistance R_{ON} of the n channel device, what is the numerical value of the delay

Use appropriate approximations.

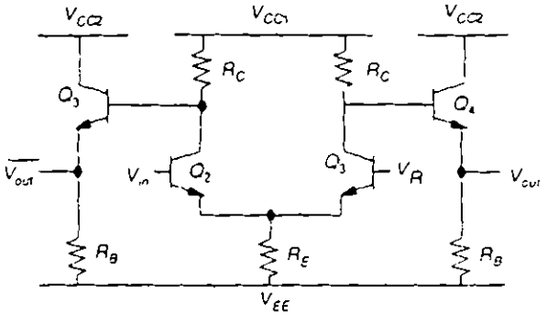


[6] (b) Consider the ECL circuit shown below. Let $V_{CC1}=V_{CC2}=0V$, $V_{EE}=-3.3V$, $R_E=400\Omega$, $V_{BE(on)}=0.7V$, $V_{CE(sat)}=0.1V$, $\beta_F=70$, and $V_R=-1.5V$.

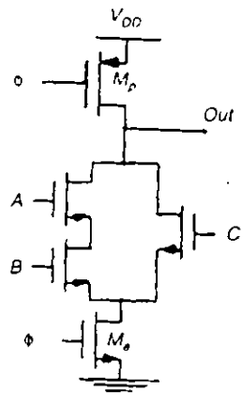
a) Calculate the values of resistors R_B and R_C such that $V_{OH}=-1V$ and $V_{OL}=-2V$ at V_{out}.

b) Find the static power consumption for: (i) $V_{in}=V_{OL}$ and (ii)$V_{in}=V_{OH}$.

c) How many isolation regions are required to implement the circuit?



[6] (c) Consider the following dynamic CMOS gate. Explain briefly the operation of the gate when Φ=0 (precharge) and when Φ=1 (evaluation). What is the logic function performed by the gate?



The following important properties are attributed to the gate, are they true or false:

True	False	
☐	☐	• The logic function is implemented by the NMOS pull-down network.
☐	☐	• The number of transistors is substantially lower than in the case of static CMOS implementation of the same function: N + 2 versus 2N.
☐	☐	• It is nonratioed.
☐	☐	• It only consumes dynamic power.
☐	☐	• Due to the reduced number of transistors per gate and the single-transistor load per fan-in, the load capacitance for this gate is substantially lower than for static CMOS. This results in faster switching speeds.