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ECE435F **Digital Integrated Circuits** **Final Exam**

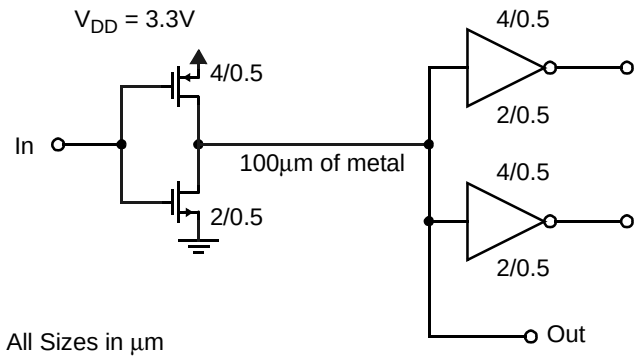
Unless otherwise stated either assume the following transistor parameters, or use the paramaters from the summary in the Appendix of Chapter 3 from the book:

- N-channel MOS transistors: $\mu_n C_{ox} = 190\ \mu A/V^2$, $V_{tn} = 0.6\ V$, $\gamma = 0.5\ V^{1/2}$, $r_{ds}(\Omega) = 9000L(\mu m)/I_D(mA)$ in active region, $C_j = 1.1 \times 10^{-3}\ pF/(\mu m)^2$, $C_{jSW} = 2.0 \times 10^{-4}\ pF/\mu m$, $C_{ox} = 4.5 \times 10^{-3}\ pF/(\mu m)^2$, and $C_{gs(overlap)} = C_{gd(overlap)} = 3.0 \times 10^{-4}\ pF/\mu m$
- P-channel MOS transistors: $\mu_p C_{ox} = 70\ \mu A/V^2$, $V_{tp} = -0.7\ V$, $\gamma = 0.6\ V^{1/2}$, $r_{ds}(\Omega) = 7000L(\mu m)/I_D(mA)$ in active region, $C_j = 1.3 \times 10^{-3}\ pF/(\mu m)^2$, $C_{jSW} = 2.5 \times 10^{-4}\ pF/\mu m$, $C_{ox} = 4.5 \times 10^{-3}\ pF/(\mu m)^2$, and $C_{gs(overlap)} = C_{gd(overlap)} = 3.0 \times 10^{-4}\ pF/\mu m$

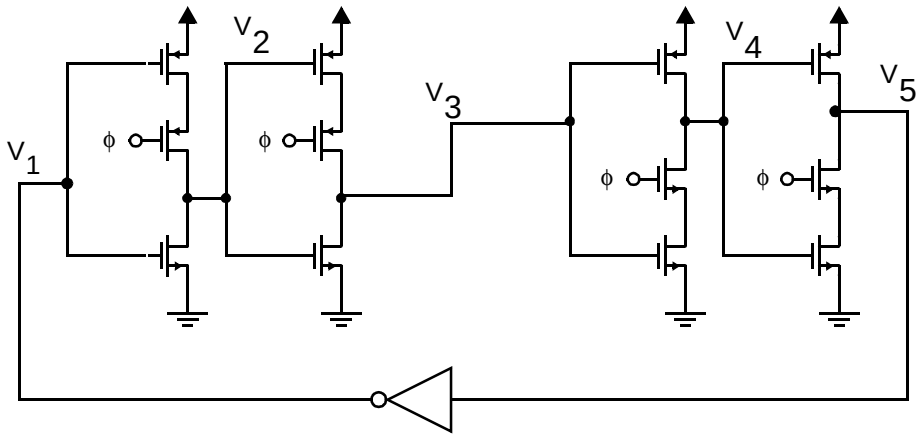
All questions are weighted equally.

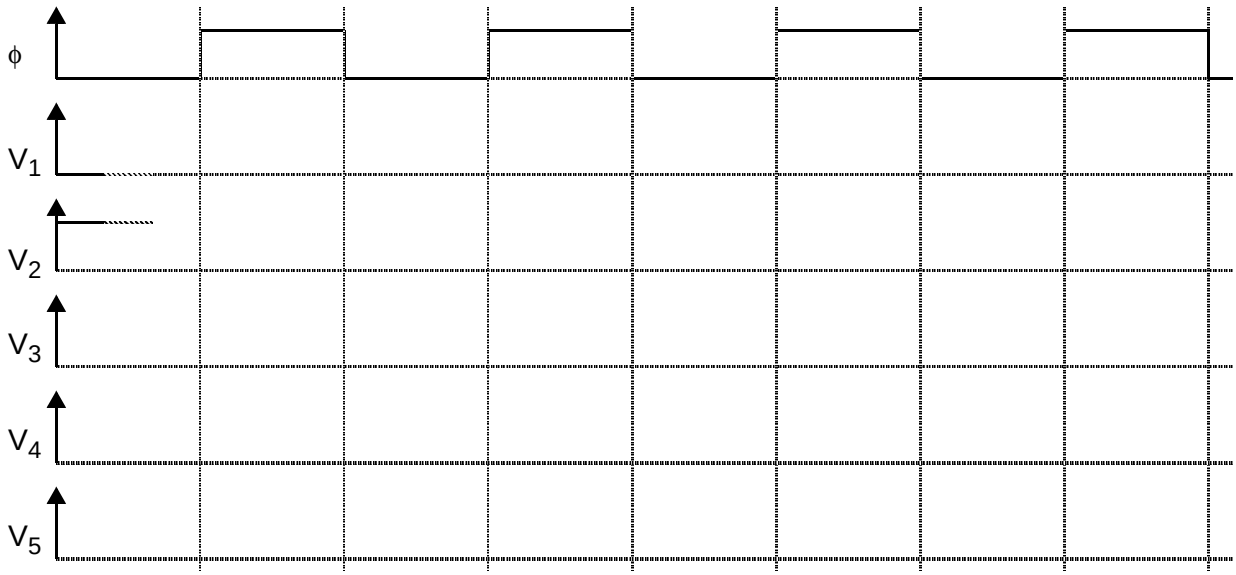
Supply answers on the attached pages only.

MAKE ALL DIAGRAMS AS NEAT AS POSSIBLE. GRADES WILL NOT BE GIVEN FOR ANSWERS THAT ARE NOT CLEARLY DISCERNIBLE. FOR EXAMPLE, CLEARLY SHOW n-ch. TRANSISTORS AS OPPOSED TO p-ch. TRANSISTORS, DEVICE SIZES, CONNECTING NODES, ETC.



1. A CMOS inverter is driving two identical inverters through a 100µm metal line that is 2µm wide and 1.0µm above the surface of the IC. The thickness of the metal is also 0.4µm. All the n-channel transistors are 2µm/0.5µm and the p-channel transistors are 4µm/0.5µm. Estimate the total load capacitance at the output of the first inverter. You may ignore junction capacitance, but do not ignore the fringing capacitance of the interconnect. What is the 70% rise time of the first inverter?





2. Fill in the timing diagrams with the appropriate waveforms assuming V_1 is initially a '0'. What function does the circuit realize?

3. Consider multiplying two 5-bit numbers where the multiplier is considered to be a positive number only and the binary equivalent to +25. The multiplicand is the two's complement equivalent to -3. Show step-by-step the process whereby the multiplication takes place. Be especially careful to use the necessary number of bits at each step.

4. Design a state-machine using sychronous design techniqes and D-type flip-flops only that continuously changes through the states: 000 100 110 111 000 100 110 111 000 and so on. Your design should be described hierarchically to the transistor level and should be based on using tranditional CMOS circuits. Transistor sizes are not necessary.