University of Toronto

Faculty of Applied Science and Engineering

Final Examination – December 2001

ECE352F – Computer Organization

Examiner – Z.G. Vranesic

Answer all questions. You may use personal textbooks, the lab manuals, your personal notes and lab book. Marks will be given for the quality of the solutions presented. Any code that you write has to be commented meaningfully.

1. [10 marks] The following program is supposed to find the smallest number in a list of n 8-bit numbers. The value n is sored in location N. Upon completion of the execution, the address of the smallest number is left in register $A2$, and the value of this number is in register $D1$. However, the program contains several errors. Find these errors and show how to correct them.

```
        MOVEA.L   #LIST,A0
        MOVE.L    #N,A1
        ADDA.L    A0,A1
        BSR       MIN
        .
        .
MIN     MOVEA.L   A0,A2
        MOVE.B    (A0)+,D1
LOOP    CMP.B     (A0)+,D1
        BLE       NEXT
        LEA       -(A0),A2
        MOVE.B    (A2),D1
NEXT    CMPA.L    A1,A0
        BLT       LOOP
        RTS
```

2. [15 marks] (*a*) Use the Booth algorithm to multiply the following numbers

$$1101101 \times 1011010$$

(*b*) Use the bit-pair recoding technique to perform the same multiplication.

3. [15 marks] Write a 68000 program to transform a 16-bit positive binary number into a 5-digit decimal number in which each digit of the number is coded in the binary-coded decimal (BCD) code. These BCD digit codes are to occupy the low-order 4 bits of five successive byte locations in the main memory. Use the conversion technique based on successive division by 10. This method is analogous to successive division by 2 when converting decimal-to-binary.

4. [20 marks] Consider a statement of the form

   IF A>B THEN action 1 ELSE action 2

   Write a sequence of assembly language instructions, first using branch instructions only, then using conditional instructions such as those available on the ARM processor. Use a generic form of instructions, rather than 68000 or ARM. Assume a simple two-stage pipeline comprising only the fetch and execute stages, and draw a diagram similar to the diagrams we used in the class to compare execution times for the two approaches.

5. [20 marks] A given computer has two input lines, I_1 and I_0, which are used to request interrupt service. It has to be able to service interrupt requests from 3 different I/O devices. There is a priority associated with each device such that

   priority of Dev3 > priority of Dev2 > priority of Dev1

   An interface circuit is needed to encode the incoming requests, *Req3*, *Req2* and *Req1*, onto the I_1 and I_0 lines so that these lines indicate the highest priority request that is active at a time. Thus, $I_1I_0 = 11$ denotes a request from Dev3, $I_1I_0 = 10$ denotes a request from Dev2, and $I_1I_0 = 01$ a request from Dev1. The state $I_1I_0 = 00$ indicates that there is no outstanding request. When multiple requests occur simultaneously, the circuit will forward the highest priority request. However, the circuit must not forward two consecutive requests from the same device if there are outstanding requests from the other two devices. This will ensure that the lowest priority device cannot be locked out by the repetitive requests from the two higher priority devices.

   Design the required circuit. Show its schematic diagram and write VHDL code that will implement it.

6. [10 marks] Give a **non-electronic** analogy of the cache concept used in computers. Think of something that would make sense to someone who knows nothing about computers.

7. [10 marks] Suppose that a complete computer is implemented on a single chip, so that the main memory can be accessed in one clock cycle just like registers. How would you change the architecture of the 68000 processor to make it suitable for this environment? Justify your answer.