Department of Electrical and Computer Engineering

ECE 342 – Digital Hardware

Final Examination
April 2001

Last Name: _____

First Name: _____

Student #: _____

Signature: _____

Duration: **2 hours**

Answer ALL questions on this test paper.
There is extra space at the end if you need it.

Examiners Report

1	_____	**/15**
2	_____	**/10**
3	_____	**/15**
4	_____	**/15**
5	_____	**/10**
6	_____	**/10**
Total	_____	**/75**

Question 1 – [15 marks]

a. In a 4-variable Boolean space consider the 2-cube A = x1x1. There is exactly one other cube, B, for which A * B = ∅:

   i. Give the cube B: _____

   ii. Is the following statement true or false: For every possible 2-cube, G, there exists exactly one other 2-cube, H, for which G * H = ∅.

   ANSWER (circle one): true or false

   iii. Prove or provide a counter example of the following statement: In an n-variable Boolean space, for each (n-1)-cube, K, there exists no other cube, L, for which K * L = ∅.

   ANSWER:

iv. Is the following statement true or false: In an n-variable Boolean space the number of (n-1)-cubes that exists is equal to n.

ANSWER (circle one): true or false

v. In a 4-variable Boolean space consider the cube A = x1x1. Define another cube, Z, such that Z # A = Z. How many cubes in total exist that satisfy this constraint?

ANSWER for Z: _____

ANSWER for total number of cubes: _____

vi. Consider a 4-variable Boolean space. For any cube 2-cube, G, how many other cubes, H, exist such that G # H generates multiple cubes?

ANSWER: _____

Question 2 – [10 marks]

i. Given the following prime implicants for a function, circle the essential prime implicants:

$f(x1, x2, x3, x4, x5, x6)$ = {0x11x0, 0x111x, 01x011, 0x110x, 101111}

ii. For a function, f, consider the following cover:

$f(x1, x2, x3, x4, x5, x6, x7)$ = {X101XX1, X1011X0, X1010X0, 1X0111X}

List the prime implicants of f. You can use the space on the next page for rough work if needed.

Prime implicants: _____

_____

_____

Give a minimal cover for f:

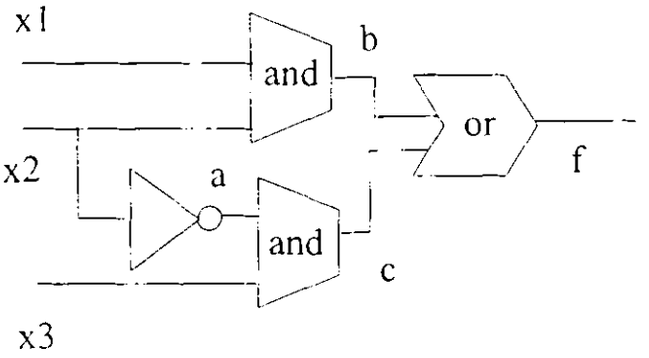
_____

_____

Rough Space for Deriving the Prime Implicants:

Question 3 – [15 marks]

a. Consider the circuit below:



Consider each of the stuck-at faults b/0, c/1 and f/0. For each of these faults, specify the values needed on wires a, b, c, and inputs x1, x2, x3 to test for the existence of each fault. List all of the test vectors that can test for each fault.

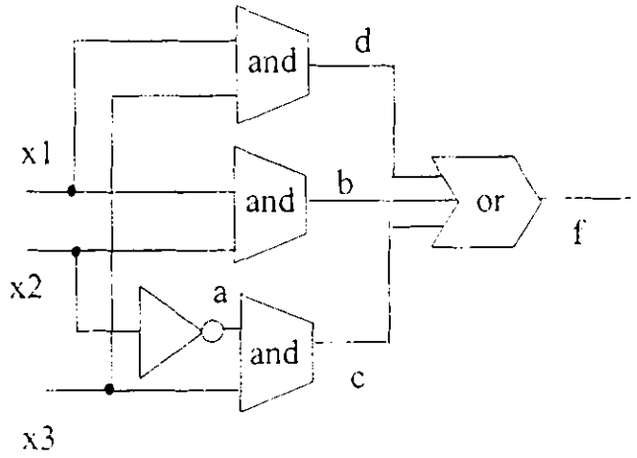
ANSWER:

b/0:

c/1:

f/0:

b. Consider the circuit below



What is the purpose of the topmost AND gate? Be as specific as possible.

ANSWER :

Consider each of the stuck-at faults d/1 and d/0. For each of these faults, specify the values needed on wires a, b, c, and inputs x1, x2, x3 to test for the existence of each fault. List all of the test vectors that can test for each fault.

ANSWER

d/1:

d/0:

Question 4 – [15 marks]

Design an asynchronous sequential circuit with two inputs C and T, and one output Q. If T =1 then Q should change whenever C changes, and if T = 0, then Q should remain stable. (This is like a T flip flop that is sensitive to both positive and negative clock edges.)

Give the corresponding state diagram. (Label the inputs as TC on the arcs in the diagram).
ANSWER:

Give the flow table
ANSWER:

Give the excitation (state assigned) table. (Label the present states y2y1 and next state Y2Y1).
ANSWER:

Give Boolean expressions for the next state and output variables. You may use the blank space on the nest space to derive your answers.
Boolean Expressions:

Give the corresponding circuit using only NAND gates and inverters.
Circuit:

Space for Rough Work for Deriving the Boolean Expressions:

Question 5 – [10 marks]

Reduce the following primitive flow table for an asynchronous sequential circuit to a state table with a minimal number of rows. Give a Mealy output table for the FSM. Show your work by giving the reduced flow table after state reduction based on output values (and next-state entries) but before merging of states, the merger diagram, and the reduced table after merging of states. Use the space on the following page for rough work if needed.

	x1x2	x1x2	x1x2	x1x2	Output
Present state	00	01	10	11	z
A	A	C	-	K	0
B	-	C	B	F	0
C	A	C	G	-	1
D	D	J	-	K	0
E	A	E	B	-	0
F	H	-	G	F	1
G	-	C	G	F	0
H	H	M	-	F	1
I	-	J	I	F	0
J	D	J	I	-	1
K	D	-	I	K	0
L	D	-	B	L	1
M	H	M	B	-	0

ANSWER for reduced flow table based on output values and next-state entries (before merging):

Merger diagram:

ANSWER for final reduced flow table after merging:

Question 6 – [10 marks]

i. In your VHDL code for several of the labs you instantiated a tri-state buffer connected to the M68K DTACK signal. Why is this buffer needed?

ANSWER:

ii. In the SRAM part of the processor lab the following statement of VHDL code (or something similar) appears:

```
srama(17 downto 0) <= address(18 downto 1) when m68k_master='1' else
  ( "000000000" & proc_addr( 8 downto 0 ) );
```

What is the purpose of this statement?

ANSWER:

iii. In the processor lab, the following statement of VHDL code (or something similar) appears:

```
saddress  <= ( "1" & R0( 7 downto 0 ) ) when ldstw='1' else
  ( "0" & PC( 7 downto 0 ) );
```

What is the purpose of this statement?

ANSWER:

iv. What is the purpose of wrapper.vhd and wrapper.acf?

ANSWER:

wrapper.vhd:

wrapper.acf:

Extra space. Use only if needed.

Extra space. Use only is needed.