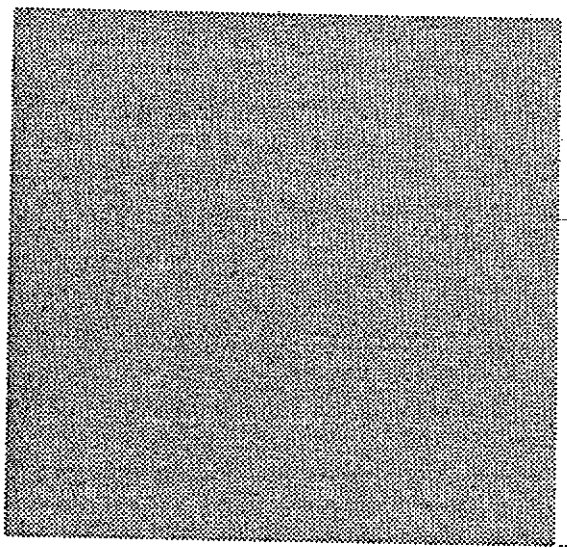
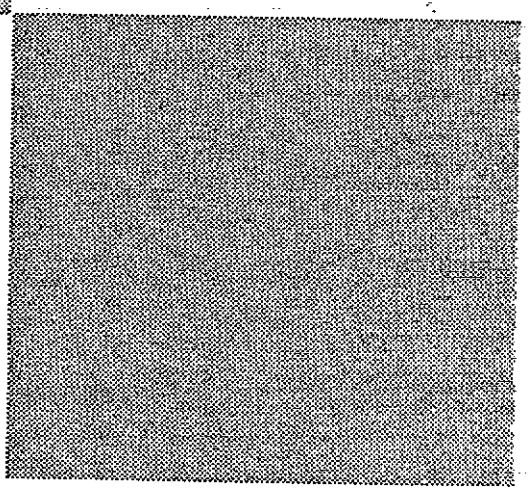
N93N8042/A



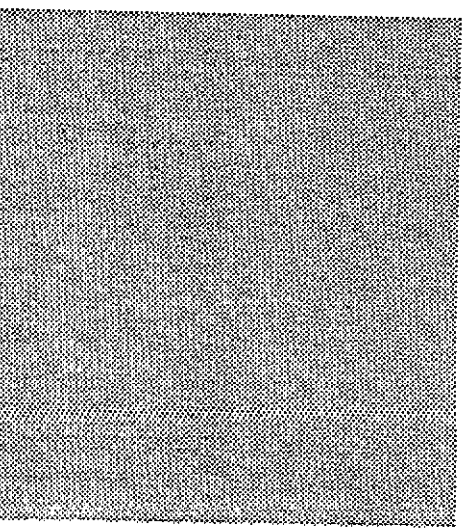
AT Keyboard Controller

Data Sheet

September 1991



P R E L I M I N A R Y



CHIPS

N93N8042/A
CHIPS AT Keyboard Controller

- IBM AT Compatible Keyboard Controller Software.
- Functional Equivalent to Intel 8042 UPI Controller.
- Fully Compatible with Chips and Technologies AT System BIOS Products.
- Supports Turbo switch and Turbo LED.
- Supports speeds from 6 Mhz to 12 Mhz.
- Clean-room Development Methodology protects against copyright infringement.
- Low Cost Manufacturing Solution.

Overview

The CHIPS AT Keyboard controller is a masked ROM/Microcontroller that is fully compatible with the IBM Keyboard controller software and Intel 8042 microcontroller. The CHIPS AT Keyboard controller software was developed using a clean-room methodology which ensures that the keyboard controller software does not infringe upon any applicable copyrights.

Functional Description

The CHIPS AT Keyboard controller is fabricated with an N-channel silicon-gate MOS process (NMOS). The controller has a 2Kx8 bit masked ROM for program memory, a 128x8 bit RAM for data memory, 18 I/O pins, an 8-bit timer/counter and clock generator on the chip. The microcontroller is designed to operate as a slave processor, which receives commands and data from the CPU, controls peripheral devices and transfers input data from peripheral devices to the CPU.

Related Publications

For more information on this device Please refer to the following material:

MBL8042H/B: Universal Peripheral Interface 8-bit Microcomputer; Fujitsu Microelectronics, Inc.

Ordering Information

CHIPS AT Keyboard Controller

Part # N93N8042/A, Ver. 2.14 (DIP)
Availability: June '91

Chips and Technologies, Inc.
3050 Zanker Road
San Jose, CA 95134

(408) 434-0600

PRODUCT OVERVIEW

The CHIPS AT Keyboard controller is a masked ROM/Microcontroller that is fully compatible with the IBM Keyboard controller software and Intel 8042 microcontroller. The CHIPS AT Keyboard controller software was developed using a clean-room methodology which ensures that the keyboard controller software does not infringe upon any applicable copyrights.

The CHIPS AT Keyboard controller is intended to be used in an AT compatible environment. The keyboard controller software performs four main functions:

- Respond to commands and data from the system.
- Collect/send serial data from/to the keyboard.
- Sense the turbo switch input.
- Control the turbo LED output.

Turbo Switch and Turbo LED

The CHIPS AT keyboard controller, when used in conjunction with a Chips and Technologies system BIOS, can support a Turbo switch and Turbo LED.

The Turbo switch is typically connected to the 8042 with a pull-up resistor on one side of the switch and the other side of the switch connected to ground. The pin the Turbo switch is connected to, and the interpretation of the state of the switch, is specified by the data byte of command A1 function 4.

The Turbo LED is typically connected to the 8042 through an open-collector inverter. The Turbo LED pin connection and output level is specified by the data byte of command A1 function 5.

The controller changes speed by emulating the <Ctrl><Alt><+> and <Ctrl><Alt><-> hot key sequences whenever there is a change of state of the Turbo Switch. The following six byte packet of scan codes are sent to the CPU to switch to high speed (<Ctrl>, <Alt>, and <+>):

Make 01Dh, 038h, 04Eh
Break 0CEh, 0B8h, 09Dh.

The following six byte packet of scan codes are sent to the CPU to switch to low speed (<Ctrl>, <Alt>, and <->):

Make 01Dh, 038h, 04Ah
Break 0CAh, 0B8h, 09Dh.

Data Transmission

Data bytes written directly to the keyboard return an ACK (FAh), or other appropriate response, which the 8042 then sends back to the system. The keyboard must respond within 20 milliseconds or a time-out error occurs. If the clock times out when the 8042 is sending the byte out to the keyboard, the 8042 sends a Resend (FEh) response to the system and sets the time-out bit in the 8042 Status Register. If the data byte gets sent correctly to the keyboard, but there is a time-out or parity error receiving the response, the 8042 sends a Resend (FEh) response back to the system and sets both the parity and time-out error flags in the 8042 Status Register.

Port I/O

The system writes or reads through I/O ports 60h and 64h. The 8042 will generate a keyboard interrupt (if enabled), and load I/O port 60 with the data byte, if any.

Table 1 - CHIPS AT Keyboard Controller Port I/O

Port	Description
60h Write	Data sent directly to keyboard/auxiliary device
60h Read	Data from 8042
64h Write	8042 commands
64h Read	8042 Status Register
	Bit 7 - Parity error 0 = no error 1 = error occurred
	Bit 6 - Receive time-out error 0 = no error 1 = error occurred
	Bit 5 - Transmit time-out Error 0 = no error 1 = error occurred
	Bit 4 - Inhibit switch 0 = keyboard is inhibited 1 = keyboard is not inhibited
	Bit 3 - Command/data 0 = last byte was data (Port 60) 1 = last byte was a command (Port 64)
	Bit 2 - System flag 0 = reset caused by power-on 1 = successful self-test
	Bit 1 - Input Buffer Full (cpu->8042) 0 = controller can accept data 1 = controller can't accept data
	Bit 0 - Output Buffer Full (8042->cpu) 0 = no data is available 1 = data is available at Port 60

Commands and Data from the System

Commands and data sent from the system to the CHIPS AT keyboard controller turn on the Input Buffer Full flag (IBF). The keyboard controller polls this flag to determine if any commands have come in from the system. When the IBF flag goes active, the keyboard controller reads the Command/Data flag (F1) to determine whether a data byte (I/O port 60 Write) or a command byte (I/O port 64 Write) has been sent. Data bytes are passed through directly to the keyboard.

Command	Description
20h	Read the 8042 Command Byte

Bit 7 - Reserved (0)
Bit 6 - Enable scan code translation:

0: Don't translate, pass through Set 2 scan codes.
1: Translate codes to Set 1

Bit 5 - AT/XT mode:

0: Translate codes like AT keyboard
1: Translate codes like XT keyboard

Bit 4 - Disable keyboard:

0: Device is enabled
1: Device is disabled

Bit 3 - Inhibit override:

0: Normal operation
1: Disables the keyboard inhibit

Bit 2 - System flag:

0: During cold boot
1: After cold boot

Bit 1 - Reserved (0)

Bit 0 - Keyboard interrupt:

0: Disabled
1: Enabled

21h-3Fh Read the 8042 RAM (bits 0-5 specify the address)

This command will return the value from the specified 8042 RAM location.

60h Write the 8042 Command Byte

Bit 7 - Reserved (0)

Bit 6 - Enable scan code translation:

0: Don't translate, pass through Set 2 scan codes
1: Translate codes to Set 1

Bit 5 - AT/XT mode:
0: Translate codes like AT keyboard
1: Translate codes like XT keyboard

Bit 4 - Disable keyboard:
0: Device is enabled
1: Device is disabled

Bit 3 - Inhibit override:
0: Normal operation
1: Disables the keyboard inhibit

Bit 2 - System flag:
0: During cold boot
1: After cold boot

Bit 1 - Reserved (0)

Bit 0 - Keyboard interrupt:
0: Disabled
1: Enabled

61h-7Fh Write the 8042 RAM (bits 0-5 specify the address)

This command will write the given value to the specified 8042 RAM location.

A1h CHIPS Extension Commands

The following functions should have the A1h command sent to Port 64h, then the function number sent to Port 60h, with all subsequent data also sent to Port 60h.

Function 00h - Return ID

This function is used to identify the keyboard controller. If a value of A6h is returned then the keyboard controller is a CHIPS Keyboard controller, part # N93N8042/A.

Function 02h - Write Input Port

The next data byte the 8042 receives it writes out to input port. Warning: If the system is not designed to support output devices connected to the input port, damage could be sustained to the system.

Function 04h - Turbo Switch Input Port

This function sets the Turbo switch input port bit mask and bit polarity. The turbo mask can specify any one of bits 0-6 on Port 1.

Data byte:

Bit 7 - Input Switch Polarity
0: Input 0 = Ctrl Alt Plus {High Speed}
1: Input 0 = Ctrl Alt Minus {Low Speed}

Bit 6-0 - Selected Input Pin:

Set bit to 1 if that bit in Port 1 should be used for the turbo switch input.

Function 05h - Turbo LED Output Port

This function sets the LED input port, port bit mask and bit polarity. The LED mask can either be Port 1 or Port 2, bits 0-5. It is the user's responsibility to make sure the pin/bit is available. On Port 2 some of these bits have industry standard definitions (eg. Gate A20, CPU Reset) and should not be used as Turbo LED outputs.

Data byte:

Bit 7 - Output Polarity:
0: Output of 0 turns on LED
1: Output of 0 turns off LED

Bit 6 - Select Port:
0: Port 1
1: Port 2

Bit 5-0 - Selected Output Pins:

Set bit(s) to 1 if that bit in the specified port (Bit 6) should be changed by the A2 and A3 commands.

A2h Turn on LED:

Must be preceded by A1 05 command

A3h Turn off LED:

Must be preceded by A1 05 command

AAh Keyboard Controller Self Test:

This command will execute a self test within the controller. 55h will be returned if the test is satisfactory, else FCh will be returned

ABh Keyboard Interface Test:

Drives the keyboard clock and data lines both high and low to verify the states. The test returns these results:

0h: No error
1h: Keyboard clock stuck low
2h: Keyboard clock stuck high
3h: Keyboard data stuck low
4h: Keyboard data stuck high

ACh Diagnostic Dump:

This command will dump 16 Bytes of RAM (20h-2Fh), 8042 Input Port, 8042 Output Port, 8042 Program Status Word, and the following message "CHIPS V xxx" (where xxx is the version number of the controller) followed by a <RETURN>. All data is sent in scan-code format.

ADh Disable Keyboard:

This sets bit 4 of the 8042 Command Byte, thereby causing the 8042 to ignore data coming in from the keyboard.

AEh Enable Keyboard:

This clears bit 4 of the 8042 Command Byte, allowing the 8042 to accept data coming in from the keyboard.

C0h Read Input Port:

This causes the 8042 to read the bits from the input port and send that byte to the system. This command is ignored if the OBF flag is true.

D0h Read Output Port:

The 8042 reads the output port and sends the byte to the system.

D1h Write Output Port:

The next data byte the 8042 receives it writes out to output port.

E0h Read Test Inputs:

The 8042 reads the state of the T0 and T1 inputs and are returned as bits 0 and 1 respectively.

F0h-FFh Pulse Output Port:

Output Port bits 0-3 are pulsed low then high. Bits 0-3 of the command represent which bits of the output port should be pulsed for approximately 6 microseconds.
(Note: 0 implies pulse bit, 1 implies don't modify bit).

HARDWARE SPECIFICATIONS

The CHIPS AT Keyboard controller is fabricated with an N-channel silicon-gate MOS process (NMOS). The controller has a 2Kx8 bit ROM for program memory, a 128x8 bit RAM for data memory, 18 I/O ports, an 8-bit timer/counter and clock generator on the chip. The equivalent of this chip is the Intel 8042 (p/n UPI-42/8042AH).

The following tables contain pin assignment, DC and AC characteristics of the CHIPS AT Keyboard Controller. For more information on this device please refer to the following publications:

MBL8042H/B: Universal Peripheral Interface 8-bit Microcomputer; Fujitsu Microelectronics, Inc.

UPI-41,42: 8041AH/8042AH/8741AH/8742AH Universal Peripheral Interface Controller; Intel Corporation, 10/89, 210393-3

Table 2. Pin Assignments

Symbol	DIP Pin #	Assignment Description
Test0	1	Kbd Clk Input
Test1	39	Kbd Data Input
XTAL1	2	+PCLK
XTAL2	3	-PCLK
RESET	4	
~SS	5	+5V
CS	6	8042 Chip Select
EA	7	Ground
~RD	8	~XIOR
A0	9	XA_2
~WR	10	~XIOW
SYNC	11	NC (No Connect)
D0-D7	12-19	XD0 - XD7
P10	27	NC (No Connect), Turbo Input, or Turbo LED Output
P11	28	NC (No Connect), Turbo Input, or Turbo LED Output
P12	29	NC (No Connect), Turbo Input, or Turbo LED Output
P13	30	NC (No Connect), Turbo Input, or Turbo LED Output
P14	31	RAM Select Input
P15	32	Manufacturing Jumper
P16	33	Primary Display Input
P17	34	Keyboard Inhibit
P20	21	Reset CPU Output
P21	22	A20 Gate Output
P22	23	NC (No Connect) or Turbo LED Output
P23	24	NC (No Connect) or Turbo LED Output
P24	35	~IRQ1: Keyboard Interrupt Output Buffer Full Output or Input Buffer Empty
P25	36	NC (No Connect) or Turbo LED Output
P26	37	~Keyboard Clk Output
P27	38	Keyboard Data Output

Table 3. Pin Description

Symbol	DIP Pin #	Type	Description
TEST 0 TEST 1	1 39	I I	KEYBOARD Clock Input KEYBOARD Data Input
XTAL 1 XTAL 2	2 3	I I	+PCLK -PCLK
RESET	4	I	RESET: Input used to reset status flip-flops
¯SS	5	I	SINGLE STEP: Single step input used in conjunction with the SYNC output to the step the program through each instruction (EPROM). This should be tied to +5V when not used. This pin is also used to put the device in Sync Mode by applying 12.5V to it
CS	6	I	CHIPS SELECT: Chip select input used to select one 8042 hip Select
EA	7	I	EXTERNAL ACCESS: External access input which allows emulation, testing and ROM/EPROM verification. This pin should be tied low if unused.
¯RD	8	I	READ: I/O read input enables CPU to read data and status words from the Output Data Bus Buffer or status register.
A_0	9	I	COMMAND/DATA SELECT: Address input used by the master processor to indicate whether byte transfer is data (A_0 = 0, F1 is reset) or command (A_0=1, F1 is set).
¯WR	10	I	WRITE: I/O write input which enables the CPU to write data and command words to the Input Data Bus Buffer.
SYNC	11	O	OUTPUT CLOCK: Output signal which occurs once per instruction cycle. SYNC can be used as a strobe for external circuitry. It is also used to synchronize single step operation.
D_0-D_7	12-19	I/O	DATA BUS: Three state, bidirectional DATA BUS BUFFER lines used to interface the controller to an 8-bit system data bus.
P_{10}-P_{17}	27-34	I/O	PORT 1: 8-bit, PORT 1 quasi-bidirectional I/O lines. P10-P17 access the signature row and security bit.
P_{20}-P_{27}	21-24 35-38	I/O	PORT 2: 8-bit, PORT2 quasi-bidirectional I/O lines. The lower 4 bits (P_{20}-P_{23}) interface directly to the 8243 I/O expander device and contain address and data information during PORT 4-7 access. The upper 4 bits (P_{24}-P_{27}) can be programmed to provide interrupt request and DMA handshake capability.
PROG	25	I/O	PROGRAM: Multifunction pin used as the program pulse input during PROM programming. This pin should be tied high if unused.
V_{CC}	40	-	POWER: +5V main power supply pin.
V_{DD}	26	-	POWER: +5V during normal operation. +12.5V during programming operation. Low power standby supply pin.
V_{SS}	20	-	GROUND: Circuit ground potential

Table 4 - D.C. Characteristics

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage (Except XTAL1, XTAL2, RESET)	-0.3	0.8	V	
V_{IL1}	Input Low Voltage (XTAL1, XTAL2, RESET)	-0.5	0.6	V	
V_{IH}	Input High Voltage (Except XTAL1, XTAL2, RESET)	2.0	V_{CC}	V	
V_{IH1}	Input High Voltage (XTAL1, RESET)	3.8	V_{CC}	V	
V_{IH2}	Input High Voltage (XTAL2)	2.2	V_{CC}	V	
V_{OL}	Output Low Voltage (D_0-D_7)		0.45	V	I_{OL} = 2.0 mA
V_{OL1}	Output Low Voltage (P_{10}-P_{17}, P_{20}-P_{27}, Sync)		0.45	V	I_{OL} = 1.6 mA
V_{OL2}	Output Low Voltage (PROG)		0.45	V	I_{OH} = 1.0 mA
V_{OH}	Output High Voltage (D_0-D_7)	2.4		V	I_{OH} = -400 μA
V_{OH1}	Output High Voltage (All Other Outputs)	2.4		V	I_{OH} = -50 μA
I_{IL}	Input Leakage Current (T0,T1, RD, WR, CS, A0, EA)		10	μA	$V_{SS} \mu V_{IN} \mu V_{CC}$
I_{OFL}	Output Leakage Current (D_0-D_7, High Z state)		10	μA	V_{SS}+ 0.45 μ $V_{OUT} \mu V_{CC}$
I_{LI}	Low Input Load Current (P_{10}-P_{17}, P_{20}-P_{27})		0.3	mA	V_{IL} = 0.8V
I_{LI1}	Low Input Load Current (RESET, SS)		0.2	mA	V_{IL} = 0.8V
I_{DD}	VDD Supply Current		20	mA	Typical = 8 mA
I_{CC}+I_{DD}	Total Supply Current		135	mA	Typical = 80 mA
I_{DD} Standby	Power Down Supply Current		20	mA	Typical = 8 mA
I_{IH}	Input Leakage Current (P_{10}-P_{17}, P_{20}-P_{27})		100	μA	V_{IN} = V_{CC}
C_{IN}	Input Capacitance		10	pF	T_A = 25 °C
C_{IO}	I/O Capacitance		20	pF	T_A = 25 °C

Table 5 - A.C. Characteristics

DBB READ

Symbol	Parameter	Min	Max	Units
t_{AR}	CS, A_0 Setup to RD	0		ns
t_{RA}	CS, A_0 Hold After RD	0		ns
t_{RR}	RD Pulse Width		160	ns
t_{AD}	CS, A_0 to Data Out Delay		130	ns
t_{RD}	RD to Data Out Delay	0	130	ns
t_{DF}	RD to Data Float Delay		85	ns

DBB WRITE

Symbol	Parameter	Min	Max	Units
t_{AW}	CS, A_0 Setup to WR	0		ns
t_{WA}	CS, A_0 Hold After WR	0		ns
t_{WW}	WR Pulse Width	160		ns
t_{DW}	Data Setup to WR	130		ns
t_{WD}	Data Hold After WR	0		ns

CLOCK

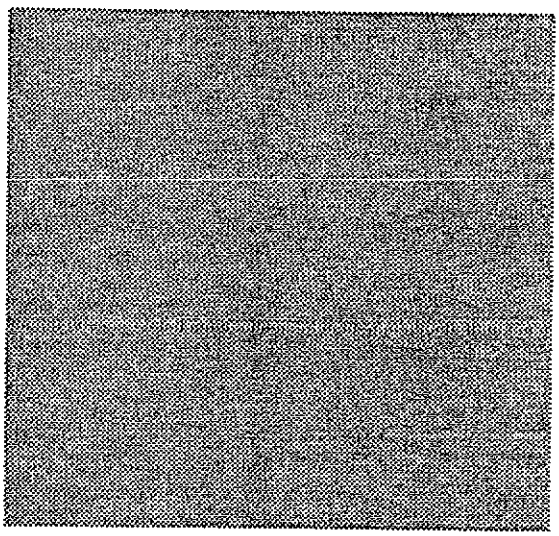
Symbol	Parameter	Min	Max	Units
t_{CY}	Cycle time	1.25	15.0	μs
t_{CYC}	Clock Period	80	613	ns
t_{PWH}	Clock High Time	30		ns
t_{PWL}	Clock Low Time	30		ns
t_R	Clock Rise Time		10	ns
t_F	Clock Fall Time		10	ns

DMA

Symbol	Parameter	Min	Max	Units
t_{ACC}	DACK to WR or RD	0		ns
t_{CAC}	RD or WR to DACK	0		ns
t_{ACD}	DACK to Data Valid	0	130	ns
t_{CRQ}	RD or WR to DRQ Cleared		110	ns

Table 6 - Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{CC},V_{DD}	Supply Voltage	-0.3	7.0	V	±10%
V_{IN}	Input Voltage	-0.3	7.0	V	±10%
T_A	Operating Temperature	0	70	°C	
T_{stg}	Storage Temperature	-55	150	°C	
P_D	Power Dissipation	1.5		W	



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