CISC 530 – Computing System Architecture

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ASSIGNMENT 1

Problem 1: Subtractor Design

a. Write Verilog code for a 1-bit full subtractor using logic equations (Difference = A-B-Bin). If you use delays, make sure to simulate for long enough to see the final result.

b. Write Verilog code for a 4-bit subtractor using the module defined in part (a) as a component. If you use delays, make sure to simulate for long enough to see the final result. Test it for the following input combinations: 1. A = 1001, B = 0011, Bin = 1 2. A = 0011, B = 0110, Bin = 1

1-bit full subtractor truth table:

A	B	Bin	Diff	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

1-Bit Subtractor:

Code:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    21:36:23 07/20/2019
// Design Name:
// Module Name:    OneBitSubtractor
// Project Name:
// Target Devices:
```

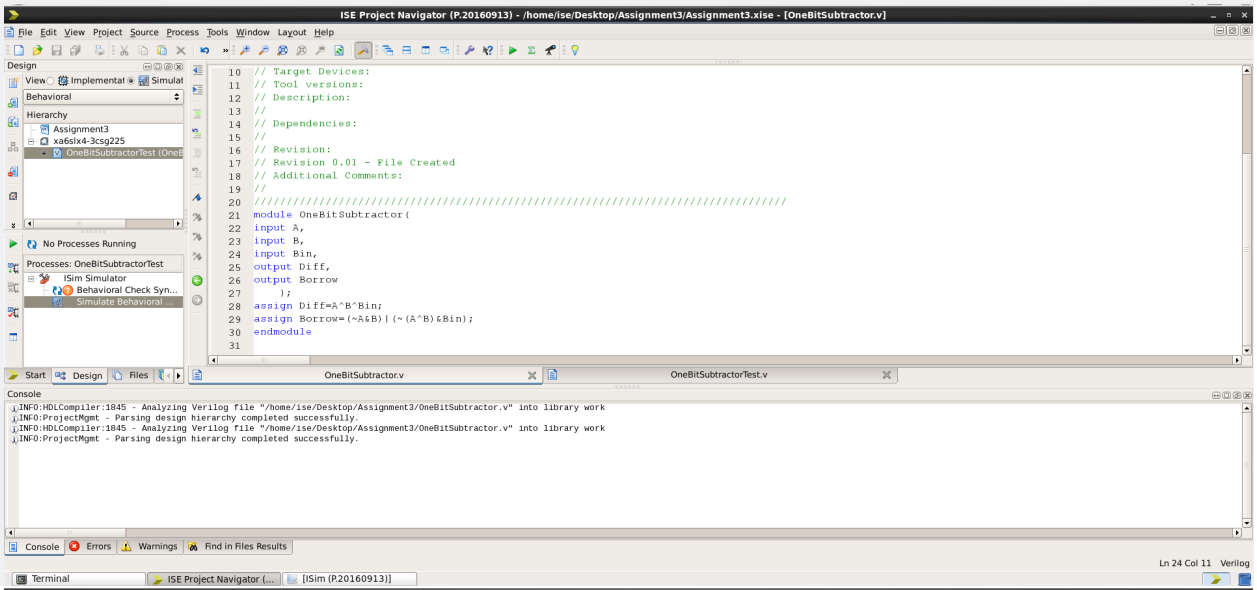
```
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module OneBitSubtractor(
input A,
input B,
input Bin,
output Diff,
output Borrow
    );
assign Diff=A^B^Bin;
assign Borrow=(~A&B)|(~(A^B)&Bin);
endmodule
```

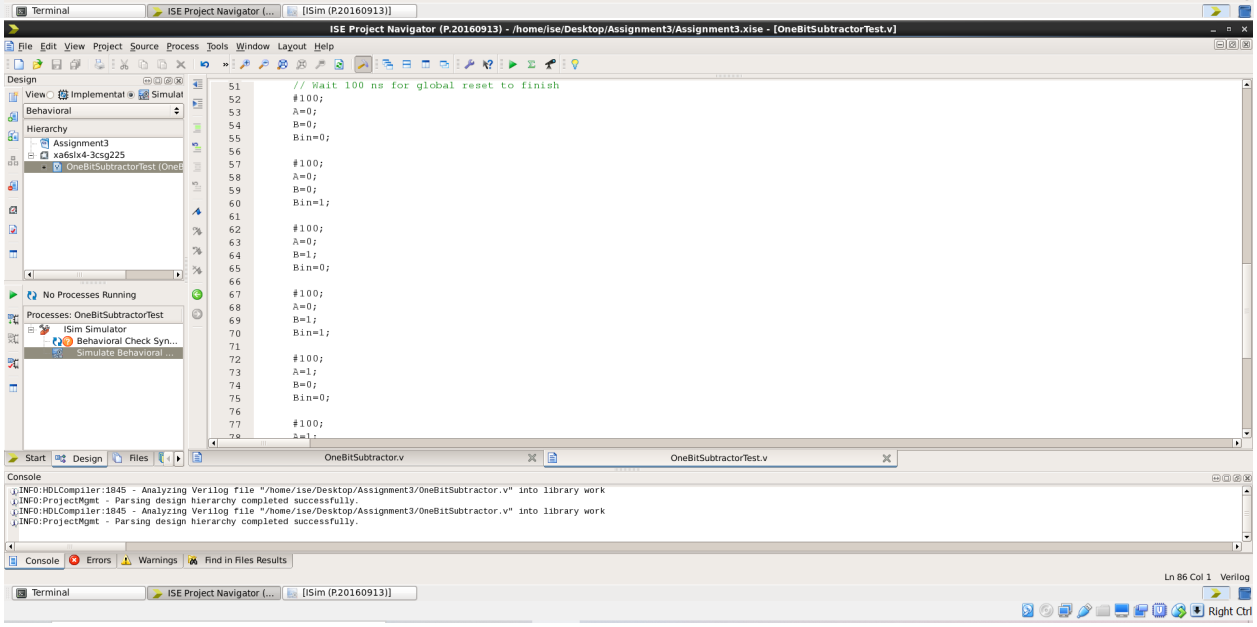
Test:

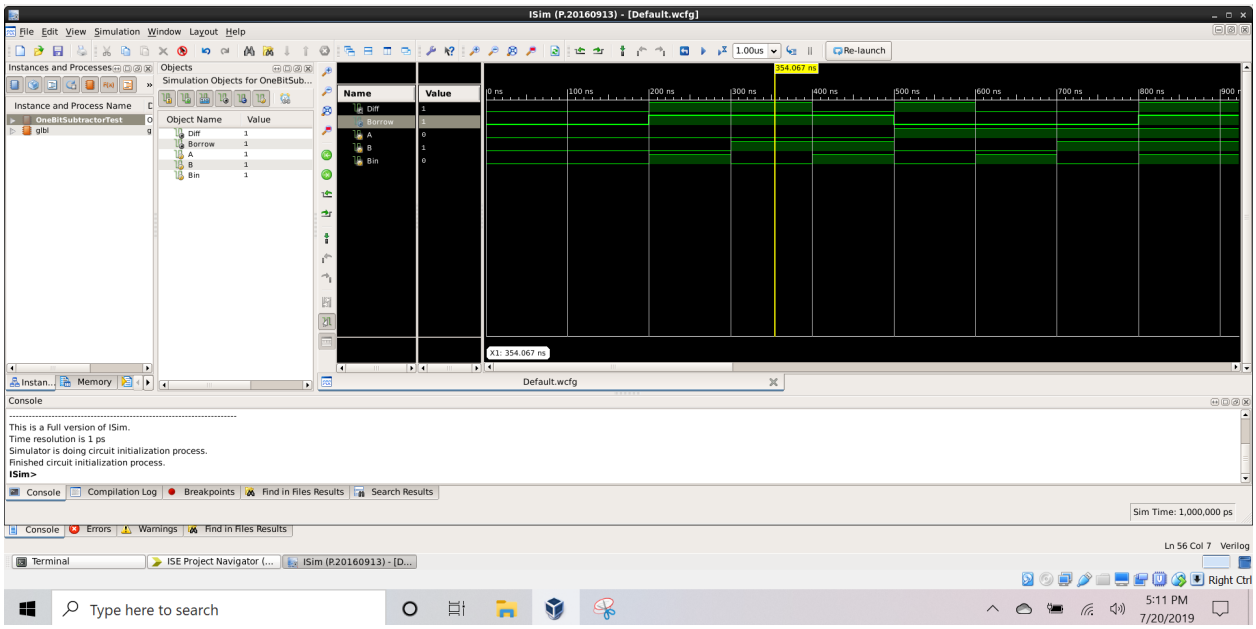
```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   21:53:31 07/20/2019
// Design Name:   OneBitSubtractor
// Module Name:   /home/ise/Desktop/Assignment3/OneBitSubtractorTest.v
// Project Name:  Assignment3
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: OneBitSubtractor
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module OneBitSubtractorTest;

        // Inputs
        reg A;
        reg B;
        reg Bin;
```

```
	// Outputs
	wire Diff;
	wire Borrow;

	// Instantiate the Unit Under Test (UUT)
	OneBitSubtractor uut (
		.A(A),
		.B(B),
		.Bin(Bin),
		.Diff(Diff),
		.Borrow(Borrow)
	);
	initial begin
		// Initialize Inputs
		A = 0;
		B = 0;
		Bin = 0;

		// Wait 100 ns for global reset to finish
		#100;
		A=0;
		B=0;
		Bin=0;

		#100;
		A=0;
		B=0;
		Bin=1;

		#100;
		A=0;
		B=1;
		Bin=0;

		#100;
		A=0;
		B=1;
		Bin=1;

		#100;
		A=1;
		B=0;
		Bin=0;

		#100;
		A=1;
		B=0;
		Bin=1;

    #100;
		A=1;
		B=1;
```

```
                Bin=0;

        #100;
                A=1;
                B=1;
                Bin=1;
                // Add stimulus here

            end
endmodule
```







4-Bit Subtractor:

Code:

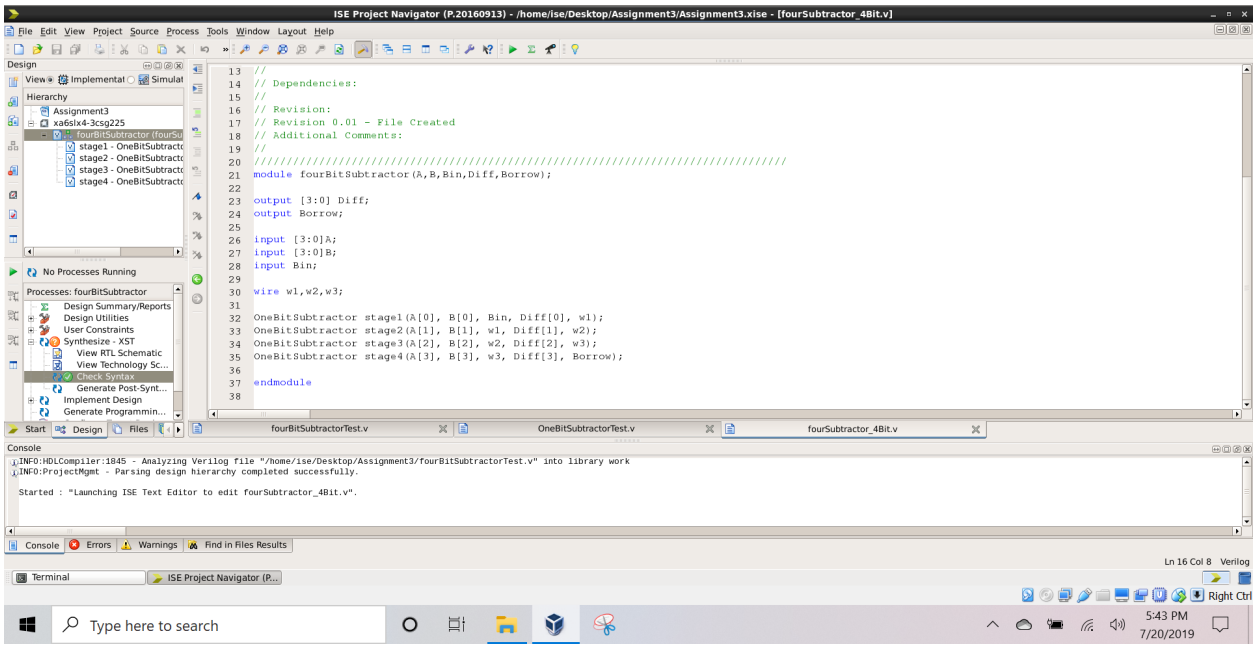
```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    22:13:45 07/20/2019
// Design Name:
// Module Name:    fourSubtractor_4Bit
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module fourSubtractor_4Bit(A,B,Bin,Diff,Borrow);

output [3:0] Diff;
output Borrow;

input [3:0]A;
input [3:0]B;
```

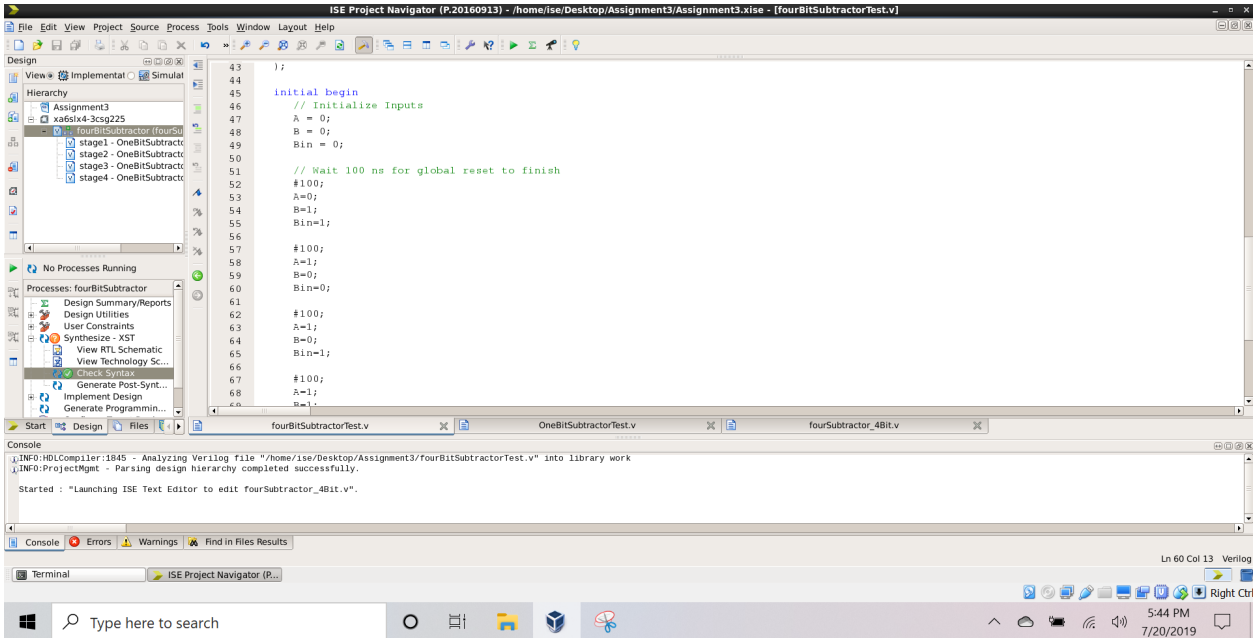
```
input Bin;

wire w1,w2,w3;

OneBitSubtractor stage1(A[0], B[0], Bin, Diff[0], w1);
OneBitSubtractor stage2(A[1], B[1], w1, Diff[1], w2);
OneBitSubtractor stage3(A[2], B[2], w2, Diff[2], w3);
OneBitSubtractor stage4(A[3], B[3], w3, Diff[3], Borrow);

endmodule
```

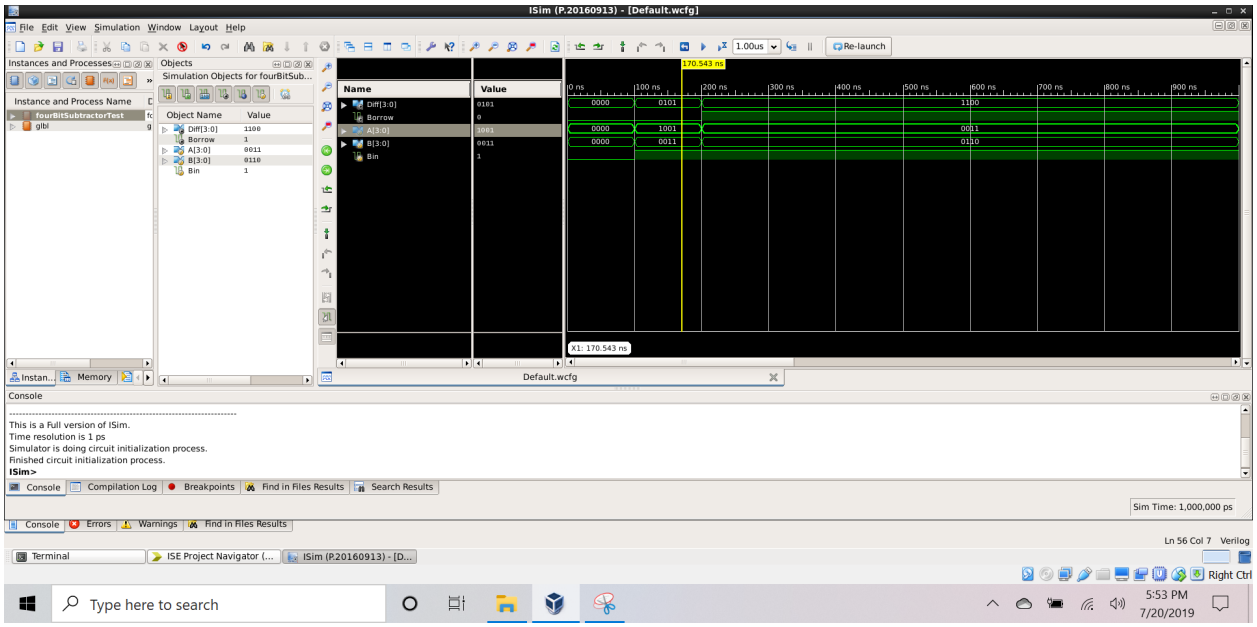
Test:

```
`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   22:39:23 07/20/2019
// Design Name:   fourBitSubtractor
// Module Name:   /home/ise/Desktop/Assignment3/fourBitSubtractorTest.v
// Project Name:  Assignment3
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: fourBitSubtractor
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module fourBitSubtractorTest;
        // Inputs
        reg [3:0] A;
        reg [3:0] B;
        reg Bin;

        // Outputs
        wire [3:0] Diff;
        wire Borrow;

        // Instantiate the Unit Under Test (UUT)
        fourBitSubtractor uut (
                .A(A),
                .B(B),
```

```
                .Bin(Bin),
                .Diff(Diff),
                .Borrow(Borrow)
        );
        initial begin
                // Initialize Inputs
                A = 0;
                B = 0;
                Bin = 0;

                // Wait 100 ns for global reset to finish
                #100;
                A=0;
                B=1;
                Bin=1;

                #100;
                A=1;
                B=0;
                Bin=0;

                #100;
                A=1;
                B=0;
                Bin=1;
      #100;
                A=1;
                B=1;
                Bin=0;
      #100;
                A=1;
                B=1;
                Bin=1;
                // Add stimulus here
          end

endmodule
```


ISE Project Navigator (P.20160913) - /home/ise/Desktop/Assignment3/Assignment3.xise - [fourSubtractor_4Bit.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
Assignment3
xa6slx4-3csg225
fourSubtractor (fourSu
stage1 - OneBitSubtracto
stage2 - OneBitSubtracto
stage3 - OneBitSubtracto
stage4 - OneBitSubtracto
No Processes Running
Processes: fourBitSubtractor
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sc...
Check Syntax
Generate Post-Synt...
Implement Design
Generate Programmin...
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //
21 module fourBitSubtractor(A,B,Bin,Diff,Borrow);
22
23 output [3:0] Diff;
24 output Borrow;
25
26 input [3:0]A;
27 input [3:0]B;
28 input Bin;
29
30 wire w1,w2,w3;
31
32 OneBitSubtractor stage1(A[0], B[0], Bin, Diff[0], w1);
33 OneBitSubtractor stage2(A[1], B[1], w1, Diff[1], w2);
34 OneBitSubtractor stage3(A[2], B[2], w2, Diff[2], w3);
35 OneBitSubtractor stage4(A[3], B[3], w3, Diff[3], Borrow);
36
37 endmodule
38
Start Design Files
fourBitSubtractorTest.v
OneBitSubtractorTest.v
fourSubtractor_4Bit.v
Console
INFO:HDLCompiler:1845 - Analyzing Verilog file "/home/ise/Desktop/Assignment3/fourBitSubtractorTest.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit fourSubtractor_4Bit.v".
Console Errors Warnings Find in Files Results
Ln 16 Col 8 Verilog
Terminal
ISE Project Navigator (P...
Right Ctrl
Type here to search
5:43 PM
7/20/2019


ISE Project Navigator (P.20160913) - /home/ise/Desktop/Assignment3/Assignment3.xise - [fourBitSubtractorTest.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Hierarchy
Assignment3
xa6slx4-3csg225
fourSubtractor (fourSu
stage1 - OneBitSubtracto
stage2 - OneBitSubtracto
stage3 - OneBitSubtracto
stage4 - OneBitSubtracto
No Processes Running
Processes: fourBitSubtractor
Design Summary/Reports
Design Utilities
User Constraints
Synthesize - XST
View RTL Schematic
View Technology Sc...
Check Syntax
Generate Post-Synt...
Implement Design
Generate Programmin...
43);
44
45 initial begin
46 // Initialize Inputs
47 A = 0;
48 B = 0;
49 Bin = 0;
50
51 // Wait 100 ns for global reset to finish
52 #100;
53 A=0;
54 B=1;
55 Bin=1;
56
57 #100;
58 A=1;
59 B=0;
60 Bin=0;
61
62 #100;
63 A=1;
64 B=0;
65 Bin=1;
66
67 #100;
68 A=1;
Start Design Files
fourBitSubtractorTest.v
OneBitSubtractorTest.v
fourSubtractor_4Bit.v
Console
INFO:HDLCompiler:1845 - Analyzing Verilog file "/home/ise/Desktop/Assignment3/fourBitSubtractorTest.v" into library work
INFO:ProjectMgmt - Parsing design hierarchy completed successfully.
Started : "Launching ISE Text Editor to edit fourSubtractor_4Bit.v".
Console Errors Warnings Find in Files Results
Ln 60 Col 13 Verilog
Terminal
ISE Project Navigator (P...
Right Ctrl
Type here to search
5:44 PM
7/20/2019



Problem 2: ALU Design

Design an Arithmetic and Logic Unit (ALU) that implements 8 functions as described in Table 1. Table 1 also illustrates the encoding of the control input. The 4-bit ALU has the following inputs:· · · A: 4-bit input

· B: 4-bit input

· Cin: 1-bit input

· Output: 4-bit output

· Cout: 1-bit output

· Control: 3-bit control input

Table 1: ALU Instructions Control

Control	Instruction	Operation
000	ADD	Output <= A + B + Cin; Cout contains the carry
001	Sub	Output <= A – B - Cin; Cout contains the borrow
010	Or	Or Output <= A or B
011	AND	And Output <= A and B
100	Shl	Output <= A[2:0] & ‘0’ 101
101	Shr	Output <= ‘0’ & A[3:1]
110	Rol	Output <= A[2:0] & A[3]
111	Ror	Output <= A[0] & A [3:1]

Code:

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:    22:57:08 07/20/2019
// Design Name:
// Module Name:    aluDesign
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
```

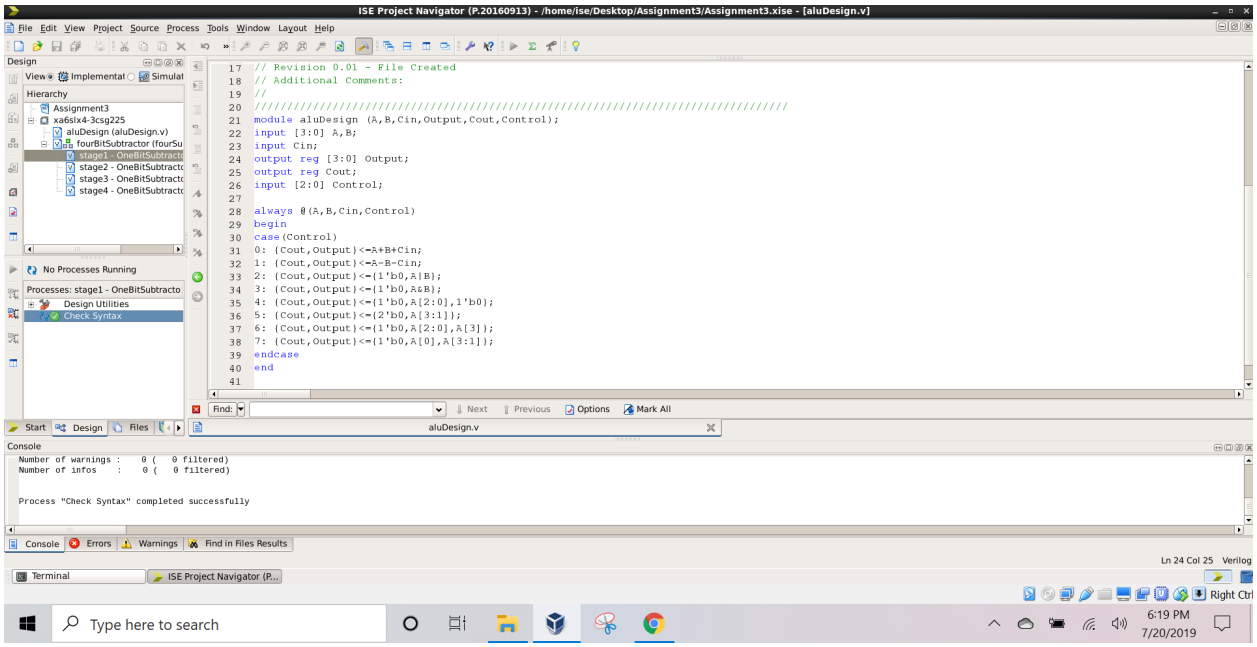
```
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////
module aluDesign (A,B,Cin,Output,Cout,Control);
input [3:0] A,B;
input Cin;
output reg [3:0] Output;
output reg Cout;
input [2:0] Control;

always @(A,B,Cin,Control)
begin
case(Control)
0: {Cout,Output}<=A+B+Cin;
1: {Cout,Output}<=A-B-Cin;
2: {Cout,Output}<={1'b0,A|B};
3: {Cout,Output}<={1'b0,A&B};
4: {Cout,Output}<={1'b0,A[2:0],1'b0};
5: {Cout,Output}<={2'b0,A[3:1]};
6: {Cout,Output}<={1'b0,A[2:0],A[3]};
7: {Cout,Output}<={1'b0,A[0],A[3:1]};
endcase
end

endmodule
```

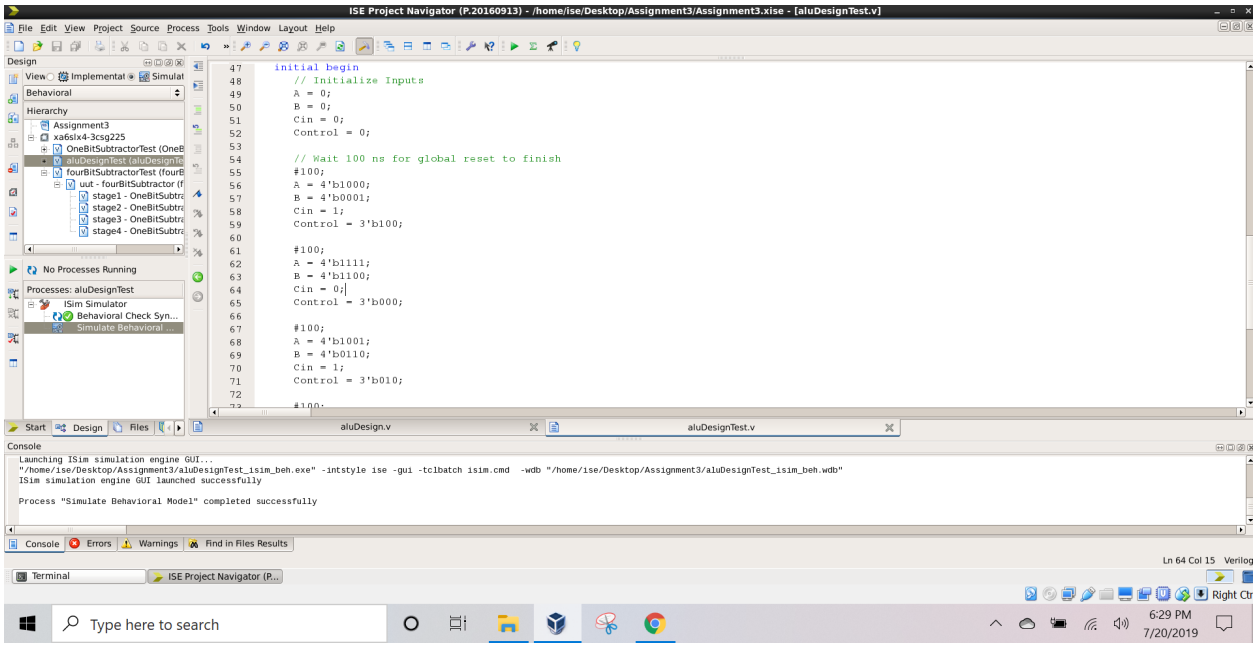
Test:

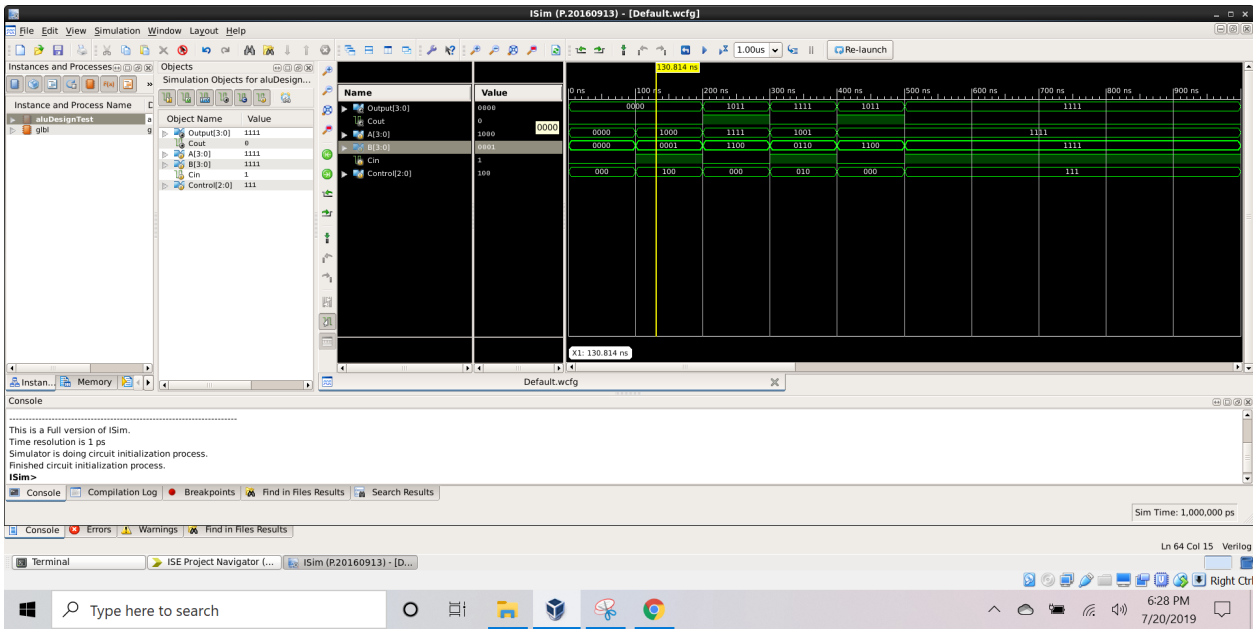
```
`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date:   23:21:14 07/20/2019
// Design Name:   aluDesign
// Module Name:   /home/ise/Desktop/Assignment3/aluDesignTest.v
// Project Name:  Assignment3
// Target Device:
// Tool versions:
// Description:
```

```
//
// Verilog Test Fixture created by ISE for module: aluDesign
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
////////////////////////////////////////////////////////////////////////////////

module aluDesignTest;

	// Inputs
	reg [3:0] A;
	reg [3:0] B;
	reg Cin;
	reg [2:0] Control;

	// Outputs
	wire [3:0] Output;
	wire Cout;

	// Instantiate the Unit Under Test (UUT)
	aluDesign uut (
		.A(A),
		.B(B),
		.Cin(Cin),
		.Output(Output),
		.Cout(Cout),
		.Control(Control)
	);

	initial begin
		// Initialize Inputs
		A = 0;
		B = 0;
		Cin = 0;
		Control = 0;

		// Wait 100 ns for global reset to finish
		#100;
		A = 4'b1000;
		B = 4'b0001;
		Cin = 1;
		Control = 3'b100;

		#100;
		A = 4'b1111;
		B = 4'b1100;
		Cin = 0;
		Control = 3'b000;
```

```
                #100;
                A = 4'b1001;
                B = 4'b0110;
                Cin = 1;
                Control = 3'b010;

                #100;
                A = 4'b1111;
                B = 4'b1100;
                Cin = 0;
                Control = 3'b000;

                #100;
                A = 4'b1111;
                B = 4'b1111;
                Cin = 1;
                Control = 3'b111;

                // Add stimulus here

        end

endmodule
```




ISE Project Navigator (P.20160913) - /home/ise/Desktop/Assignment3/Assignment3.xise - [aluDesignTest.v]
File Edit View Project Source Process Tools Window Layout Help
Design
Behavioral
Hierarchy
Assignment3
xa6slx4-3csg225
OneBitSubtractorTest (OneB
aluDesignTest (aluDesignTe
fourBitSubtractorTest (fourB
uut - fourBitSubtractor (f
stage1 - OneBitSubtra
stage2 - OneBitSubtra
stage3 - OneBitSubtra
stage4 - OneBitSubtra
No Processes Running
Processes: aluDesignTest
ISim Simulator
Behavioral Check Syn...
Simulate Behavioral ...
47 initial begin
48 // Initialize Inputs
49 A = 0;
50 B = 0;
51 Cin = 0;
52 Control = 0;
53
54 // Wait 100 ns for global reset to finish
55 #100;
56 A = 4'b1000;
57 B = 4'b0001;
58 Cin = 1;
59 Control = 3'b100;
60
61 #100;
62 A = 4'b1111;
63 B = 4'b1100;
64 Cin = 0;
65 Control = 3'b000;
66
67 #100;
68 A = 4'b1001;
69 B = 4'b0110;
70 Cin = 1;
71 Control = 3'b010;
72
Start Design Files
aluDesign.v
aluDesignTest.v
Console
Launching ISim simulation engine GUI...
"/home/ise/Desktop/Assignment3/aluDesignTest_isim_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "/home/ise/Desktop/Assignment3/aluDesignTest_isim_beh.wdb"
ISim simulation engine GUI launched successfully
Process "Simulate Behavioral Model" completed successfully
Console Errors Warnings Find in Files Results
Ln 64 Col 15 Verilog
Terminal
ISE Project Navigator (P...
Type here to search
6:29 PM
7/20/2019


ISim (P.20160913) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Instances and Processes
Instance and Process Name
aluDesignTest
glbl
Objects
Simulation Objects for aluDesign...
Object Name Value
Output[3:0] 1111
Cout 0
A[3:0] 1111
B[3:0] 1111
Cin 1
Control[2:0] 111
Name
Value
Output[3:0]
Cout
A[3:0]
B[3:0]
Cin
Control[2:0]
130.814 ns
X1: 130.814 ns
Default.wcfg
Console
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console Compilation Log Breakpoints Find in Files Results Search Results
Sim Time: 1,000,000 ps
Console Errors Warnings Find in Files Results
Ln 64 Col 15 Verilog
Terminal
ISE Project Navigator (...
ISim (P.20160913) - [D...
Type here to search
6:28 PM
7/20/2019