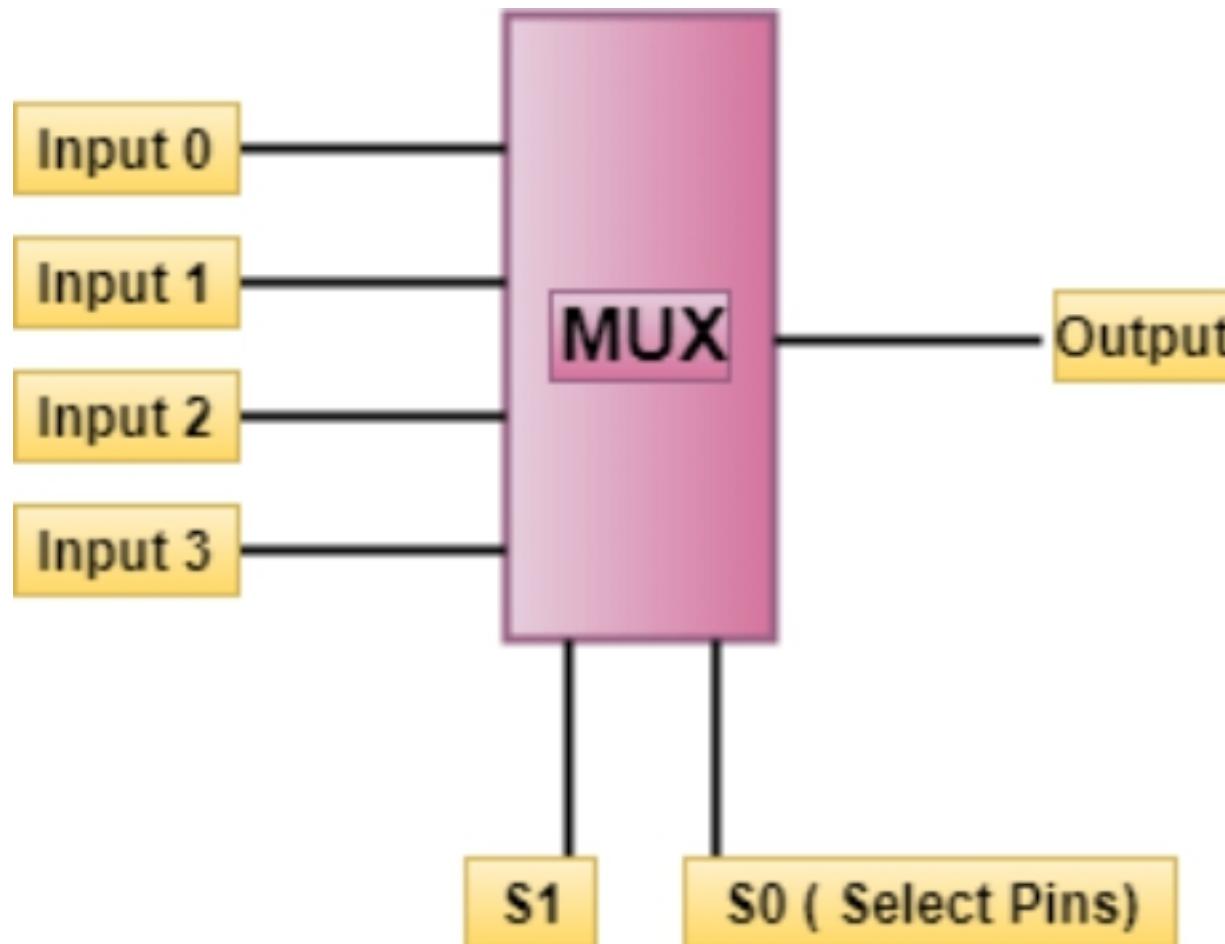


Multiplexing

- It quite often happens, in the design of large-scale digital systems, that a **single line is required to carry two or more different digital signals.**
- **Of course, only one signal at a time can be placed on the one line.** What is required that will **allow us to select, at different instants, the signal we wish to place** on this common line. Such a circuit is referred to as a Multiplexer.
- **A multiplexer performs the function of selecting the input on any one of ‘n’ input lines and feeding this input to one output line.**
- Multiplexing means **Sharing**.
- It is the process of switching information from several lines on to a single line in a specified sequence.
- A multiplexer or data selector is a logic circuit that accepts several data inputs and allows only one of them to get through to the output. Its an N-1 device.

Multiplexing

A multiplexer performs the function of selecting the input on any one of 'n' input lines and feeding this input to one output line.



Experiment Number 3 and 4 have two parts individually..

- (1) Testing/Validation of Multiplexing or Decoding Action
- (2) Implementation of a given Boolean function with Multiplexer or Decoder.

As an example,

Implement the Boolean Function $f(a, B, C) = A'B + BC + A'C$ using 4:1 Mux.

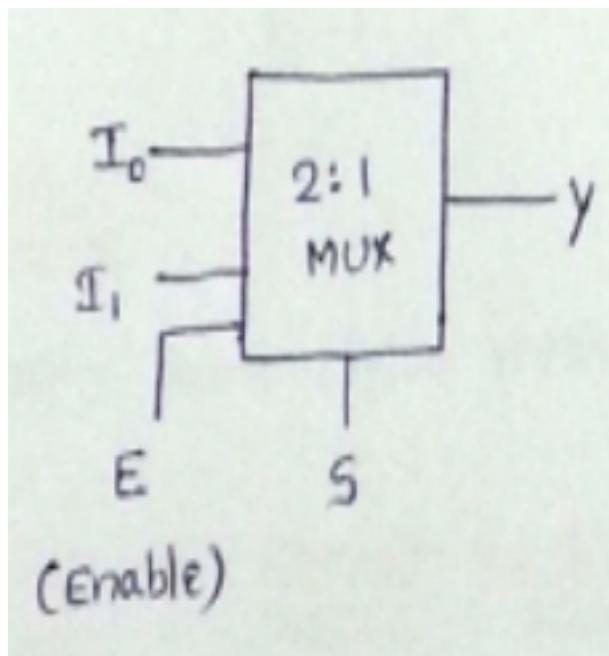
Or, using 2:1 Mux (Tree Concept)

Or, Implement the Full Adder using 4:1 Mux (So reduce the number of ICs XOR/OR/AND etc. to one IC (MUX) only.

Basic 2-Input Multiplexer (2:1 MUX)

The following figure shows the logic circuitary and function table for a 2-input multiplexer with data inputs I_0 and I_1 , chip enable (E) and data select input S.

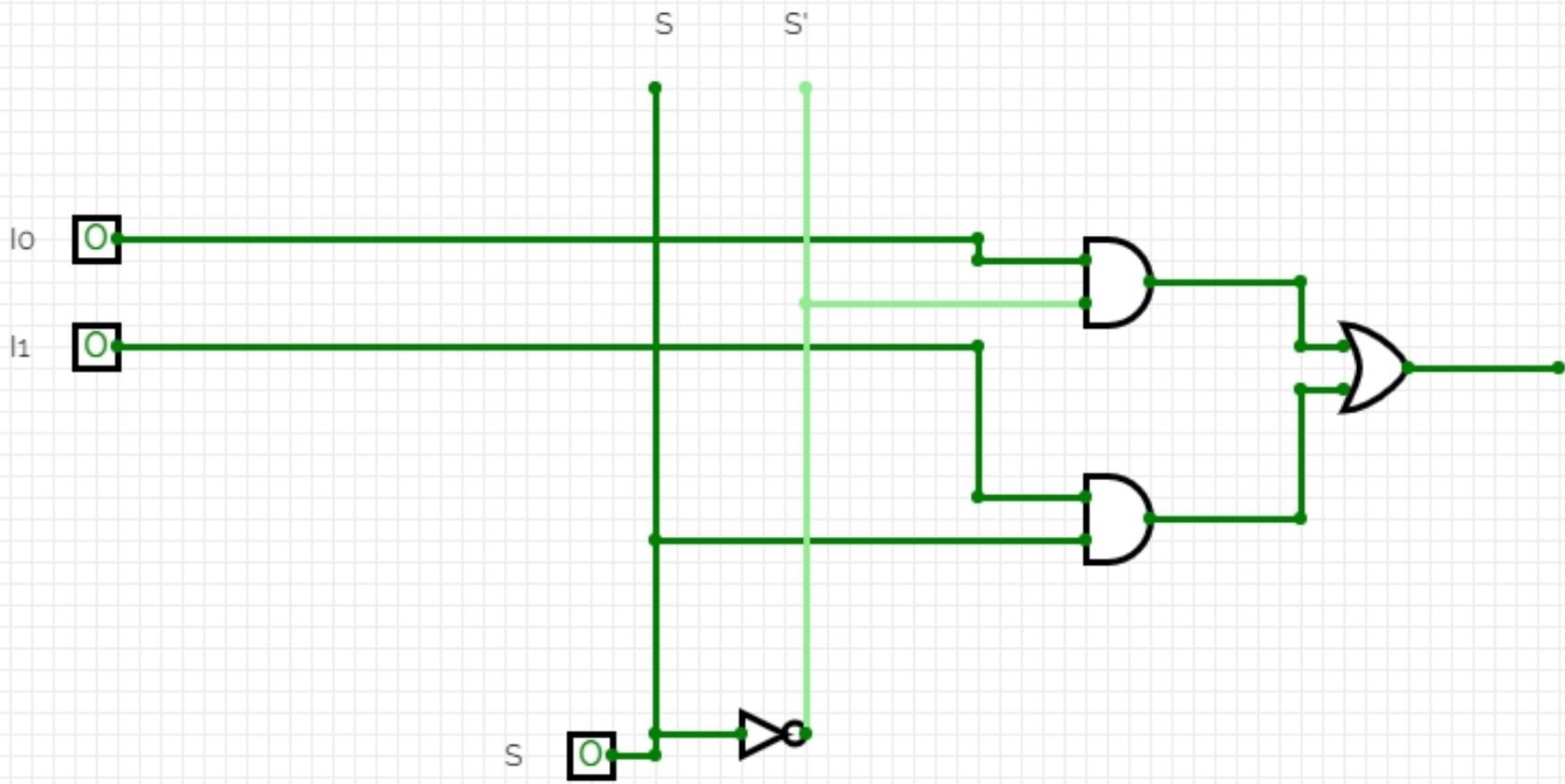
Logic symbol of 2:1 Multiplexer



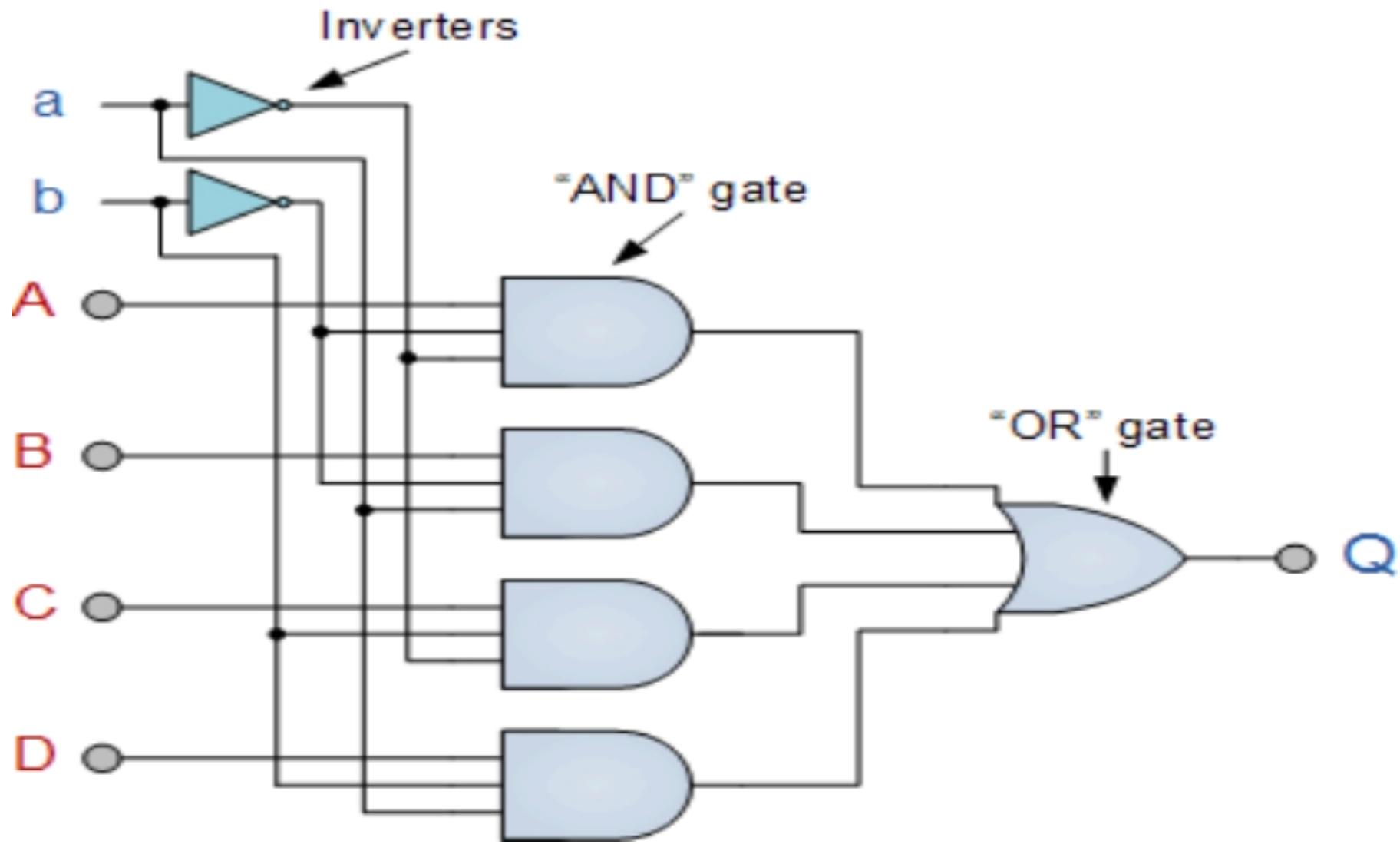
Function Table

E	S	Y
0	x	0
1	0	I_0
1	1	I_1

$$\text{Hence Logic function: } Y = E(S'I_0 + SI_1)$$

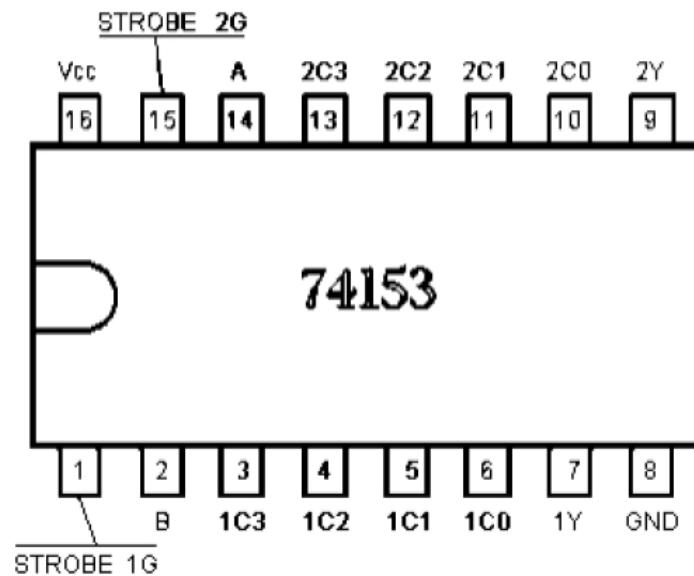


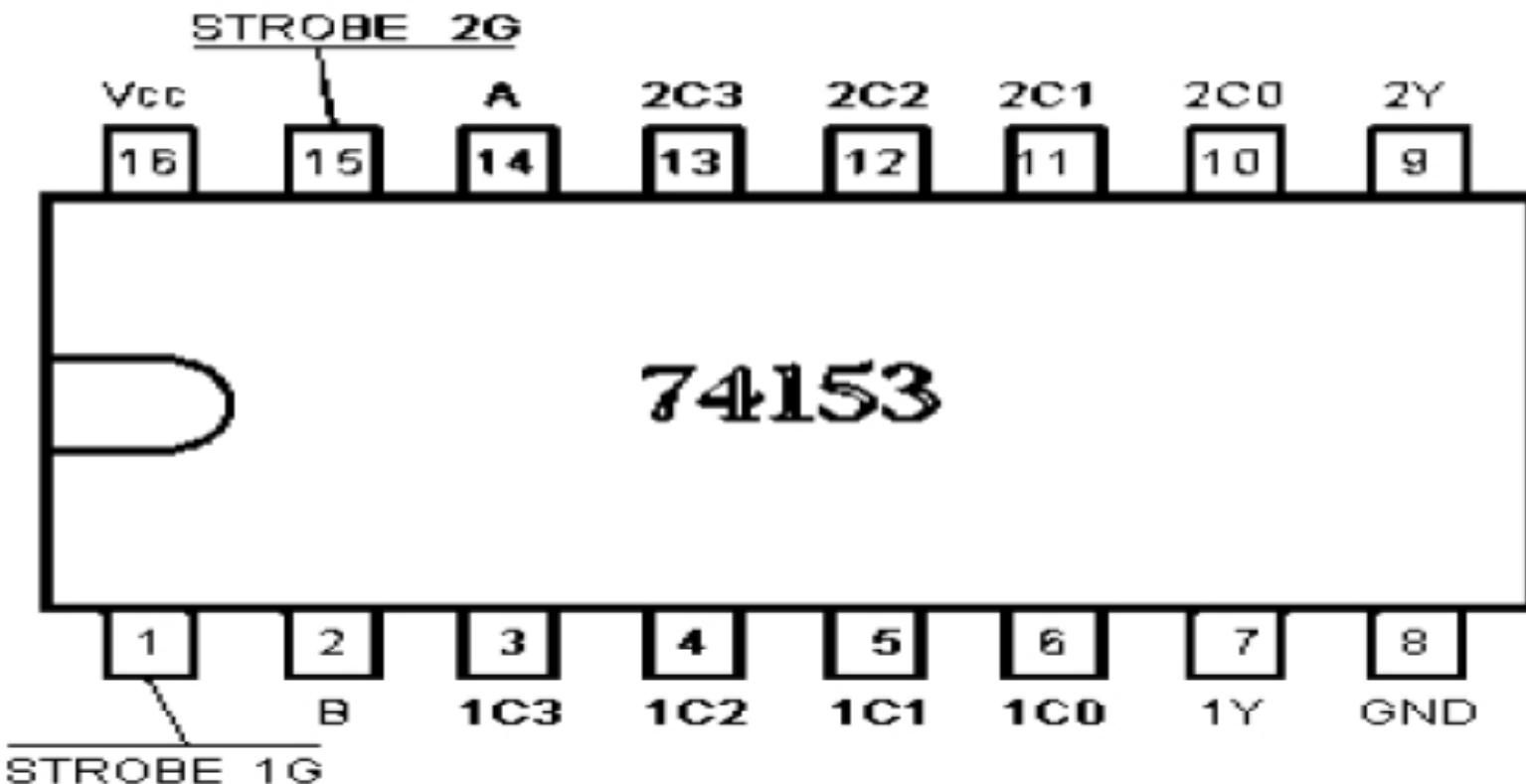
Logic Diagram (4:1 MUX)



Experiment 3: To design a circuit to implement Boolean Functions using Multiplexers.

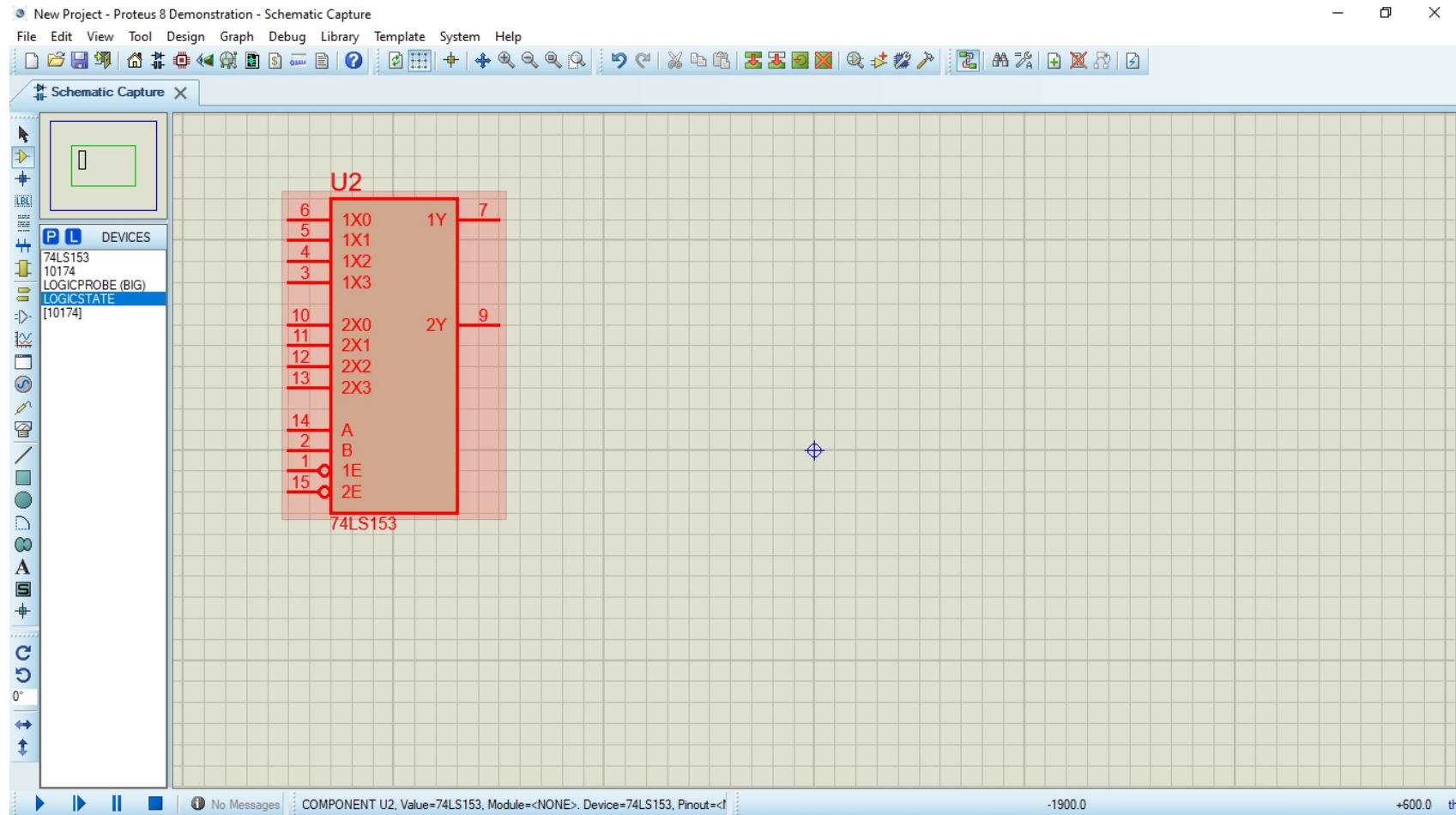
- IC1: Multiplexer IC (Dual 4:1 mux 74153),
- IC2: 7404
- **How to realize functionality of Dual 4 Line to 1 Line Multiplexer using 74153 IC.**





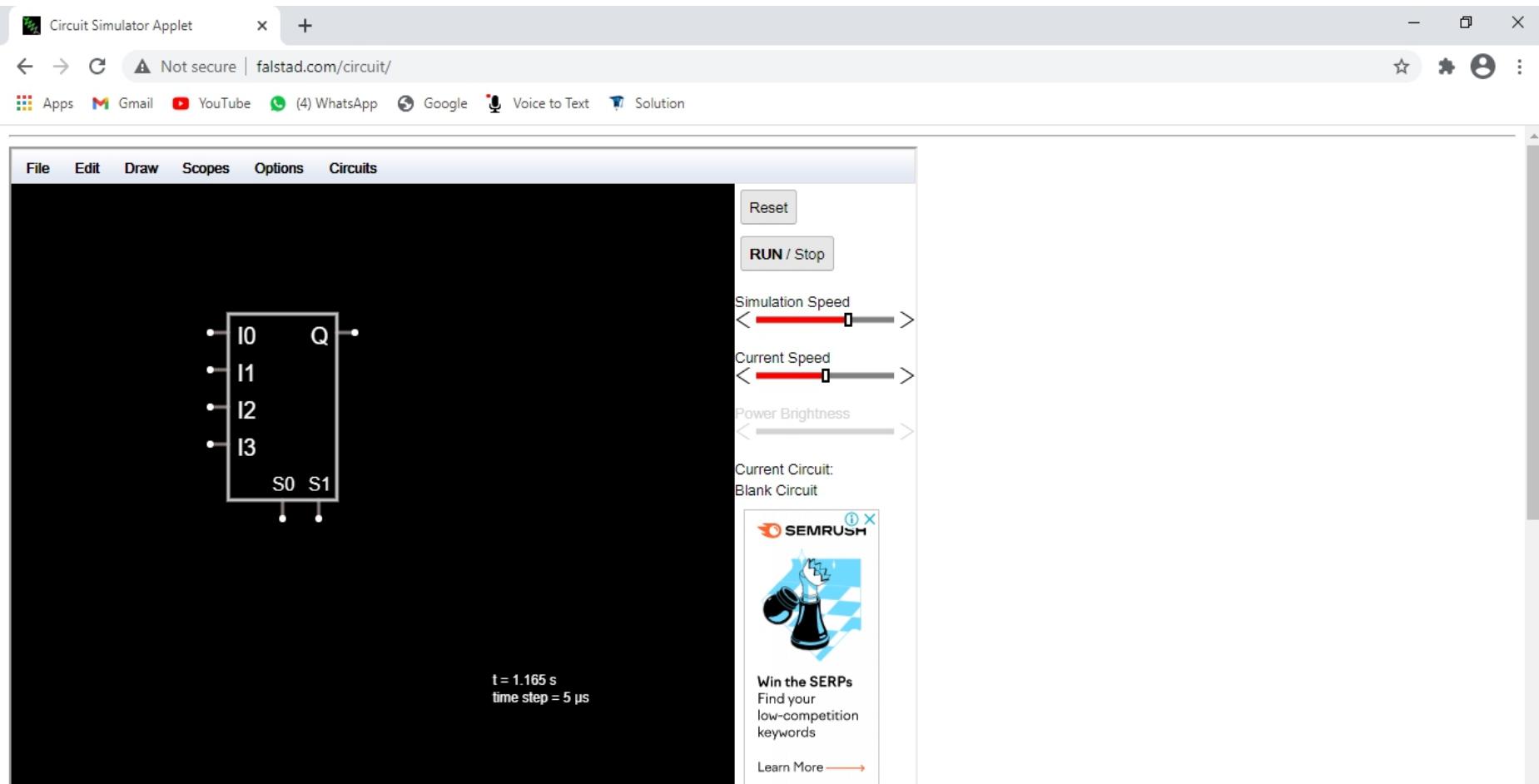
- Multiplexers are used as one method of reducing the number of IC packages required by a particular circuit design. This in turn reduces the cost of the system.
- Assume that we have four lines, C_0 , C_1 , C_2 and C_3 , which are to be multiplexed on a single line, Output (Y). The four input lines are also known as the Data Inputs.
- Since there are four inputs, we will need two additional inputs to the multiplexer, known as the Select Inputs, to select which of the inputs is to appear at the output. Call these select lines A and B. The gate implementation of a 4-line to 1-line multiplexer is shown above.

IC Package in Simulation



IC Package in Simulation

<http://falstad.com/circuit/>



This is an electronic circuit simulator. When the applet starts up you will see an animated schematic of a simple LRC circuit. The green color indicates positive voltage. The gray color indicates ground. A red color indicates negative voltage. The moving yellow dots indicate current.

To turn a switch on or off, just click on it. If you move the mouse over any component of the circuit, you will see a short description of that component and its current state in the lower right corner of the

- Add Wire w
- Add Resistor r
- Passive Components ►
- Inputs and Sources ►
- Outputs and Labels ►
- Active Components ►
- Active Building Blocks ►
- Logic Gates, Input and Output ►
- Digital Chips ►
- Analog and Hybrid Chips ►
- Drag ►
- Select/Drag Sel (space or Shift-drag)

S0 S1

- Add D Flip-Flop
- Add JK Flip-Flop
- Add T Flip-Flop
- Add 7 Segment LED
- Add 7 Segment Decoder
- ✓ Add Multiplexer
- Add Demultiplexer
- Add SIPO shift register
- Add PISO shift register
- Add Counter
- Add Ring Counter
- Add Latch
- Add Sequence generator
- Add Full Adder
- Add Half Adder
- Add Custom Logic
- Add Static RAM

4. Procedure

- a) At first go through the structure of 74153. Then apply high level voltage to Vcc and low level voltage to GND. If Vcc and ground are not connected properly then error message will be shown and no output will be generated.
- b) Next, apply high level voltage to Strobe1G or strobe 2G. If STROBE 1G is low, 1st Multiplexer is activated. If STROBE 2G is low, then 2nd Multiplexer is activated.
- c) Next, apply low level voltage to the select inputs A and B (A Most Significant Bit, B Less significant bit). Then apply a high level voltage to 2C0. Now check that how Dual 4 Line to 1 Line Multiplexer select the particular input to be multiplexed and to be applied to the output IY {1 = 1, 2}.
- d) For all the combinations of the select inputs A, B verify that both the LEDs are glowing or not glowing. If the LED glows, it indicates that the corresponding output has reached logic 1 level. Similarly, a dark LED indicates low level output voltage.
- e) If both the Strobe inputs are low then both Multiplexers are activated.

5. Cautions:

1. Do not press the IC on breadboard until pins are aligned with pours.
2. Make connection properly.
3. There should not any short circuit in the circuit.
4. Avoid the heating of IC.

Implementation of Full Adder using 4:1 mux

Inputs			Sum	Carry
A	B	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

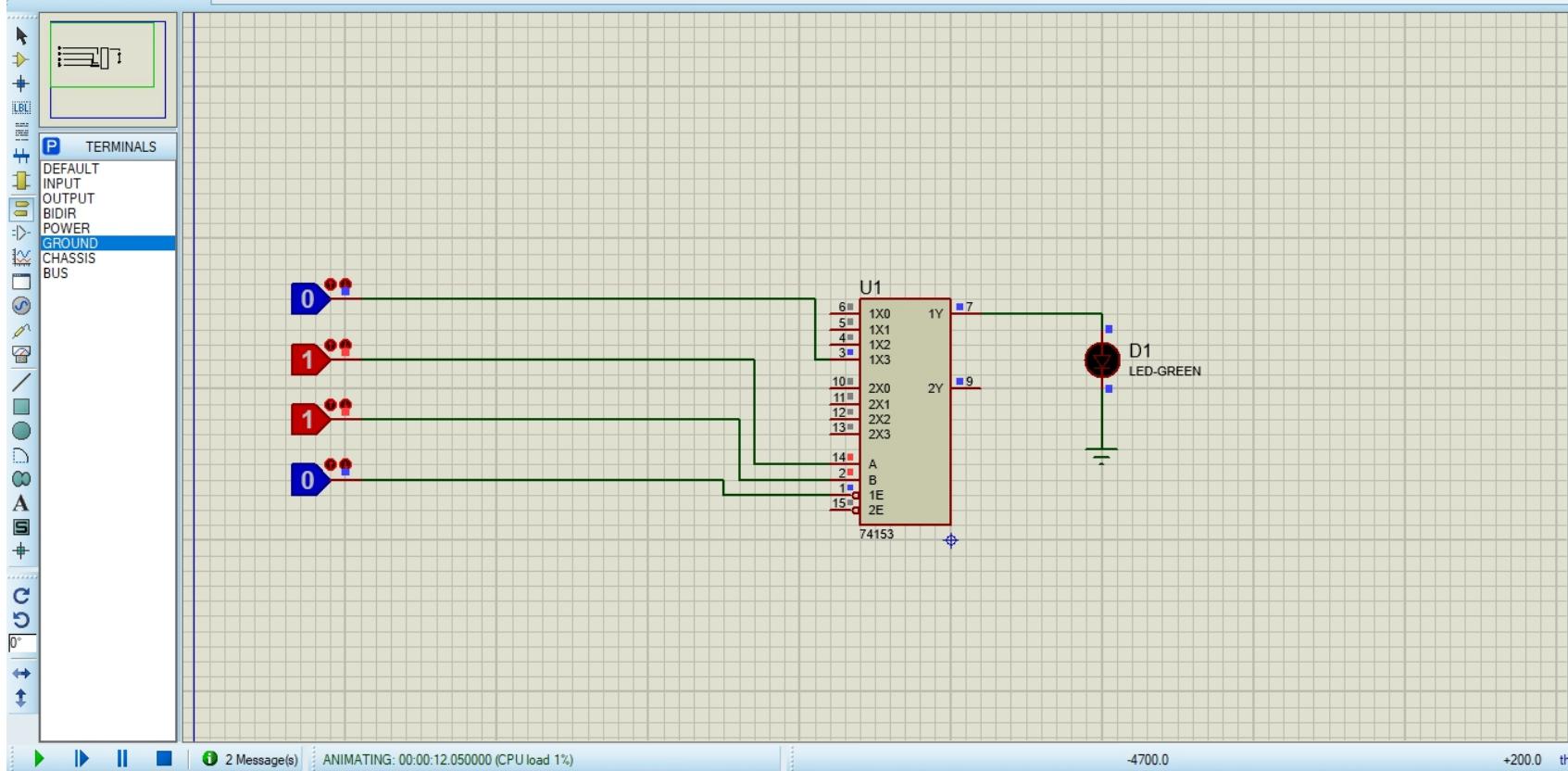
Development of Function Table

New Project - Proteus 8 Demonstration - Schematic Capture

File Edit View Tool Design Graph Debug Library Template System Help

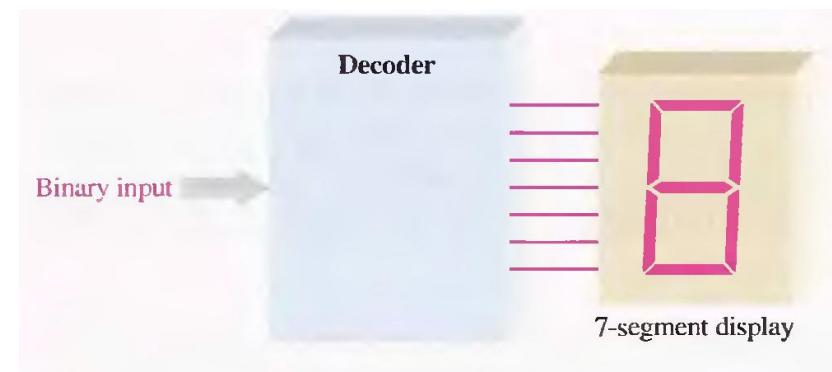
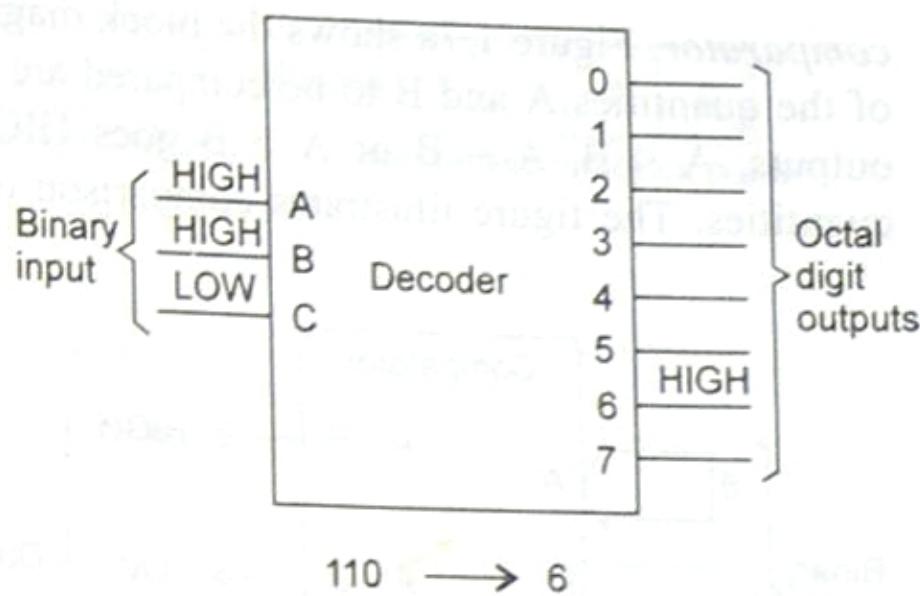


Schematic Capture X



Decoding

- Decoding is the inverse operation of encoding. A **decoder converts binary-coded information (ABC) to unique outputs such as decimal, octal digits, etc.**
- In the binary-to-octal decoder as shown in figure, a combination of specific levels on the input lines produces a HIGH on the corresponding output line. The figure shows decoding of the binary **110** to octal digit **6**.

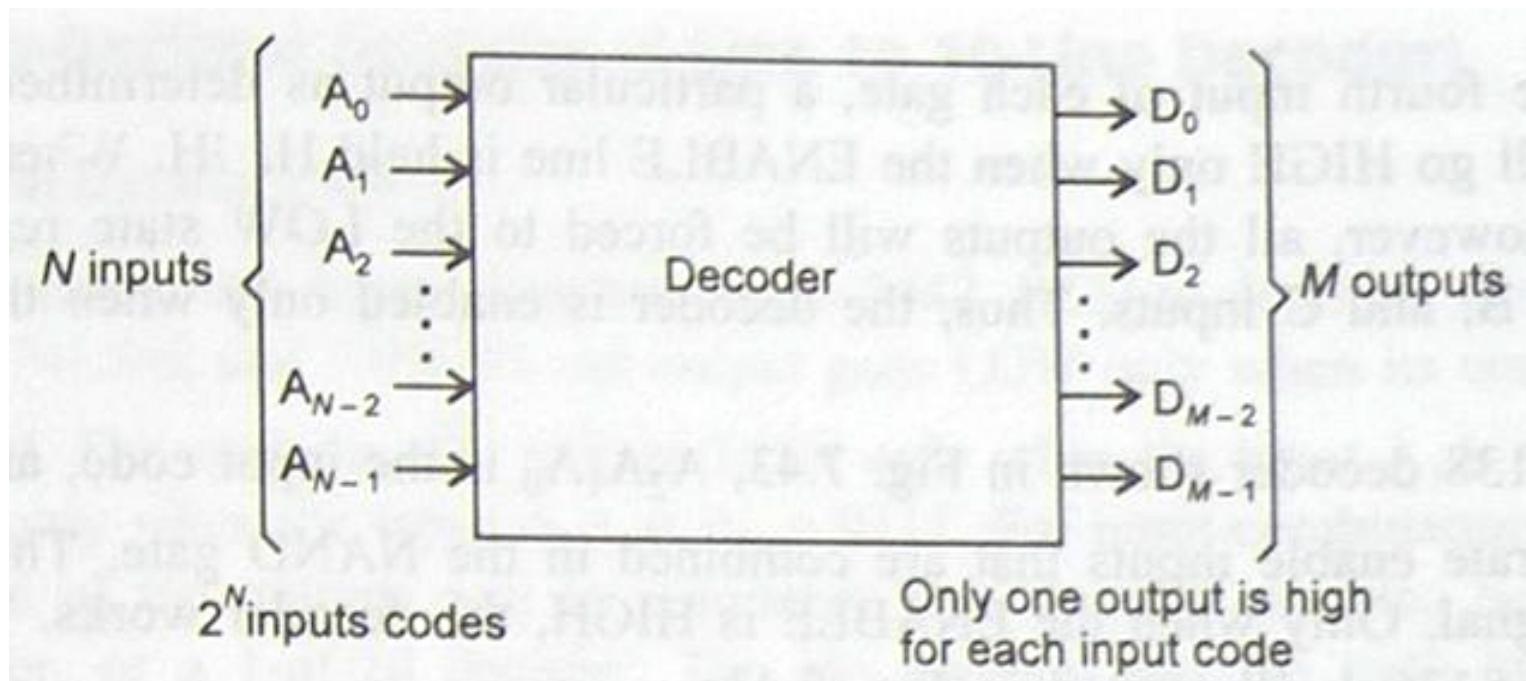


Decoders

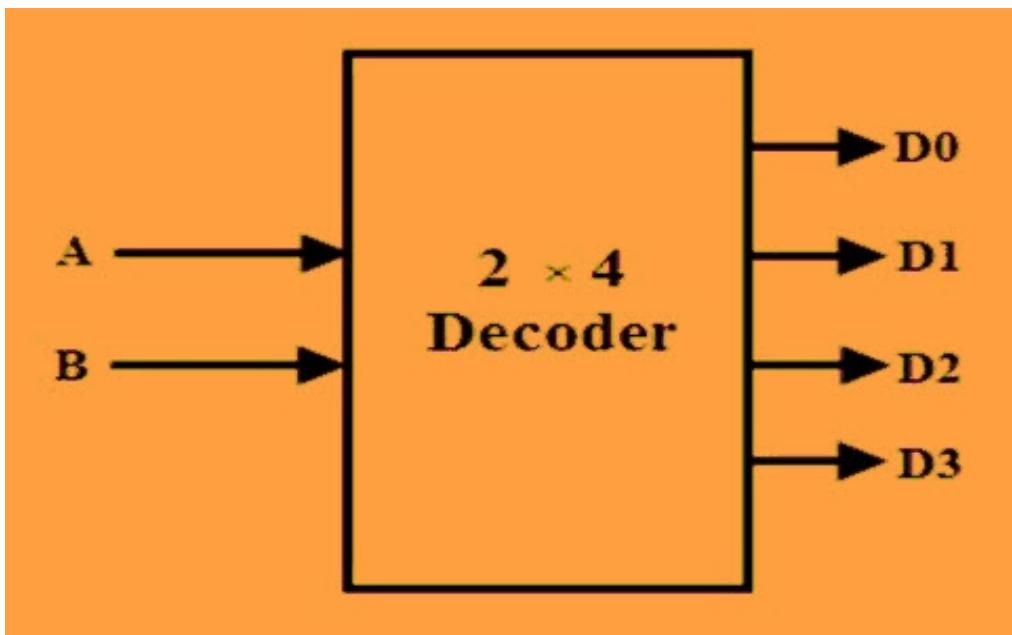
A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs.

The following figure shows the general decoder diagram with N inputs and M Outputs. Since each of the N inputs can be a 0 or a 1, there are 2^N possible input combinations or codes. For each of these input combinations, only one of the M outputs will be active (HIGH), all the other outputs will remain inactive (LOW).

Some decoders are designed to produce active low output, while all the other outputs remain HIGH.



2:4 Line Decoder



Truth Table

A ₁	A ₀	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

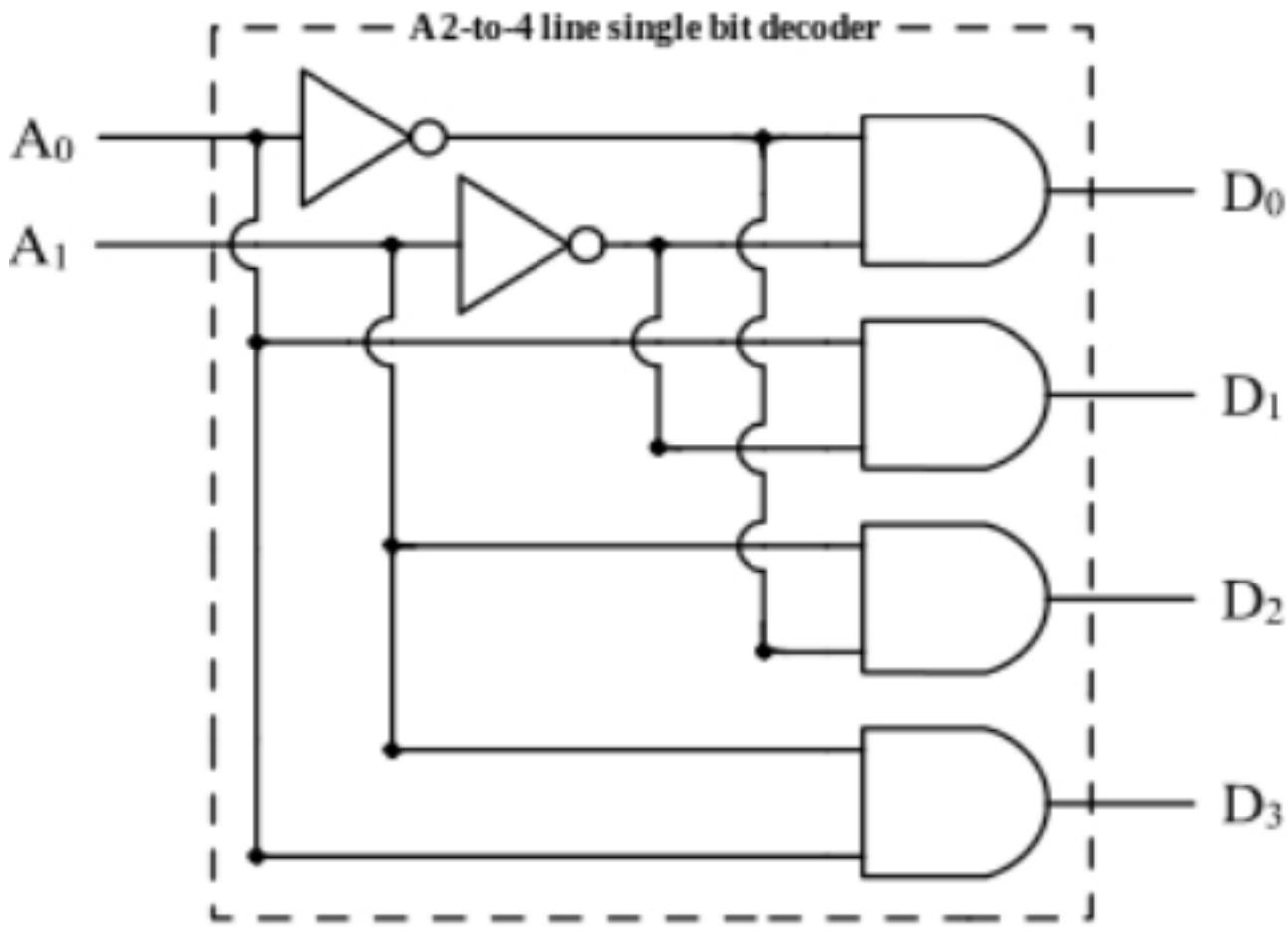
Minterm Equations

$$D_0 = \overline{A}_1 \cdot \overline{A}_0$$

$$D_1 = \overline{A}_1 \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A}_0$$

$$D_3 = A_1 \cdot A_0$$



Truth Table

A ₁	A ₀	D ₃	D ₂	D ₁	D ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

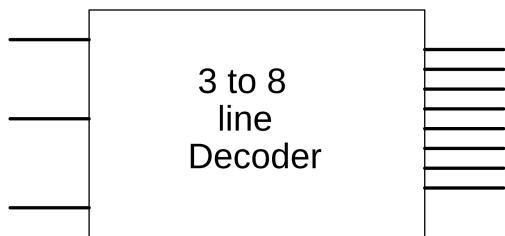
$$D_0 = \overline{A}_1 \cdot \overline{A}_0$$

$$D_1 = \overline{A}_1 \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A}_0$$

$$D_3 = A_1 \cdot A_0$$

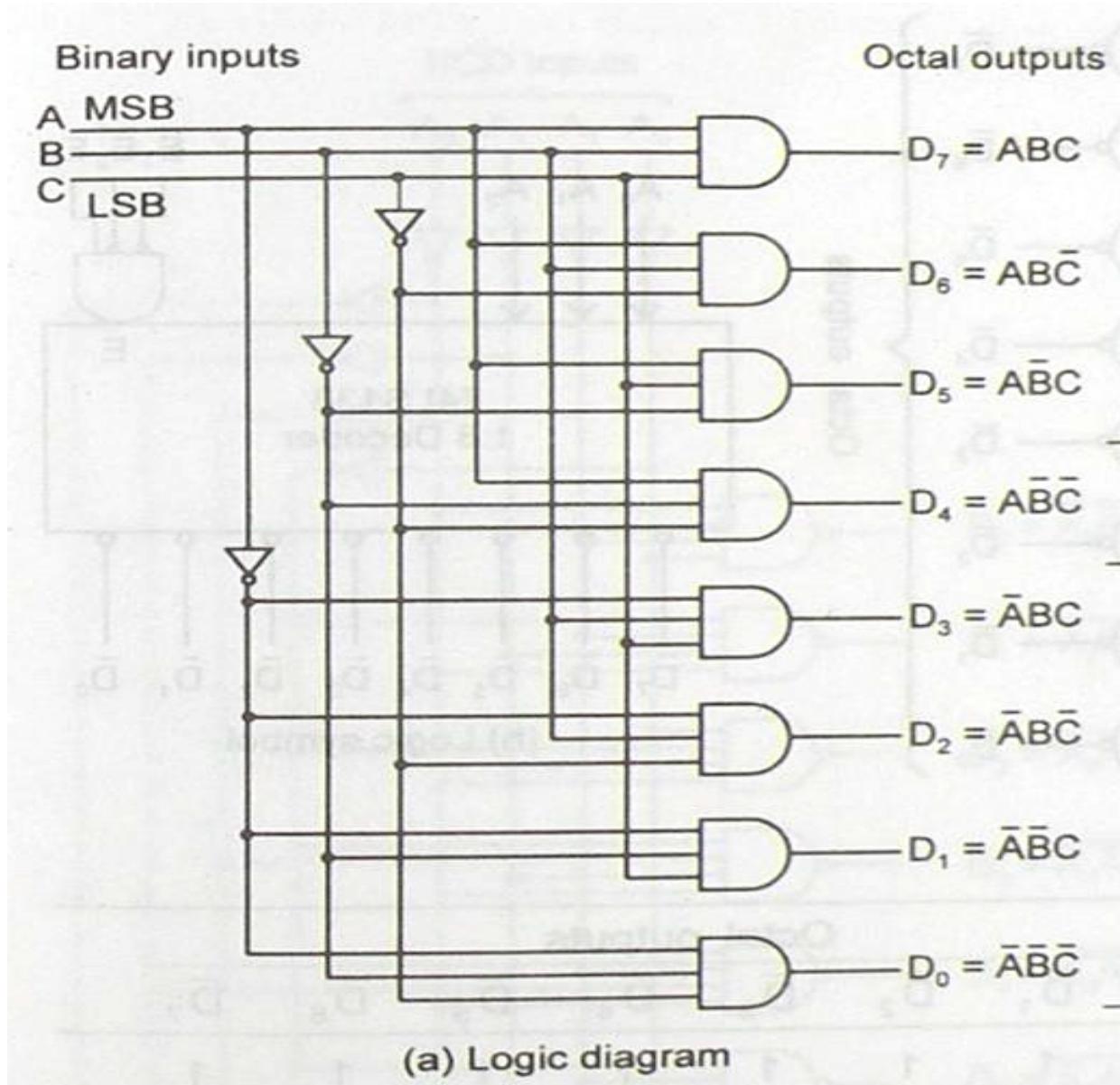
3-Line to 8-Line Decoder



The following figure shows the circuitry for a decoder with 3 inputs and 8 outputs.

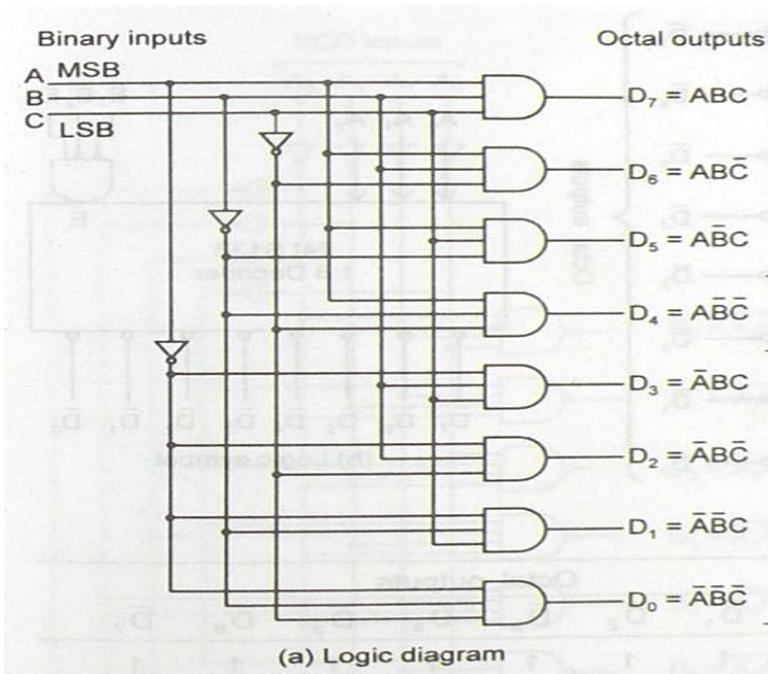
It uses all AND gates, and therefore, the outputs are active-High.

For active-Low outputs, NAND gates are used.



3-Line to 8-Line Decoder

The following figure shows the circuitry for a decoder with 3 inputs and 8 outputs. It uses all AND gates, and therefore, the outputs are active-High. For active-Low outputs, NAND gates are used.



(a) Logic diagram

Inputs	Outputs										
	A	B	C	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	0	1

(b) Truth table

This decoder can be referred in several ways. It can be called a 3-line to 8-line decoder because it has 3 input lines and 8 output lines.

It can also called a binary-to-octal decoder because it takes a 3-bit binary input code and activates one of the 8 (octal) outputs corresponding to the code.

It is also referred to as a 1-of-8 decoder because only one of the 8 outputs is activated at one time.

Experiment 4: To design a circuit to implement Boolean Functions using Decoders.

- IC 74138 and others (7404/7432/7400/7408/7410)
- **IC 74138** works as a **3-to-8 active low decoder**, based on the values assigned to 3 select inputs of the 3 enable inputs, G_1 must be made High value while G_{2A} and G_{2B} must be low. The 8 active low inputs (Y_0 to Y_7) correspond to 8 max terms (M_0 to M_7) or in other words, component of the corresponding min terms m_0-m_7 . For example, $Y_0 = \text{component of } CBA = C + B + A$.

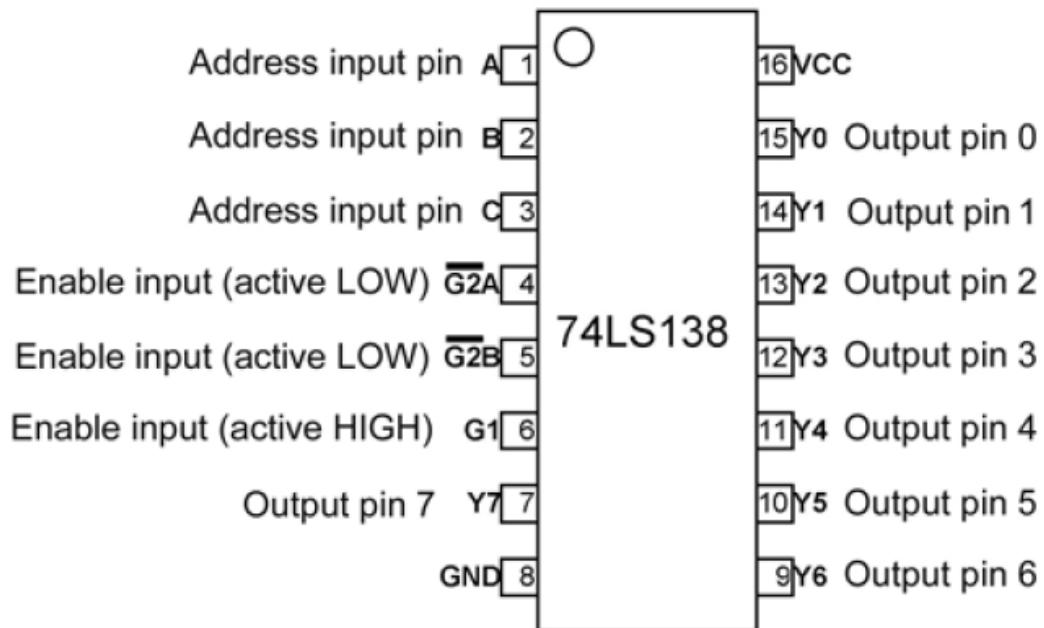


Figure 1: Pin configuration of IC 74138

Truth table of 74138

Inputs						Outputs								
G2A	G2B	G1	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	
H	X	X	X	X	X	H	H	H	H	H	H	H	H	
X	H	X	X	X	X	H	H	H	H	H	H	H	H	
X	X	L	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	
L	L	H	H	L	L	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	H	H	L	H	H	H	L	H	H	H	H	
L	L	H	L	L	H	H	H	H	H	L	H	H	H	
L	L	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	H	L	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	H	H	H	H	H	H	H	H	L	H	
L	L	H	H	H	H	H	H	H	H	H	H	H	L	

H = HIGH, L = LOW and X = Don't Care

Testing of Decoder..

4. Procedure

1. At first go through the structure of 74138. Then apply high level voltage to VCC and apply low level voltage to GND and also apply high level voltage to G1.
2. Next, apply low level voltage to all the three select inputs (C B A). Now check that Y0 is at low state. Other outputs are at high state.
3. Apply low level voltage to C and B and apply high level voltage to A. Now check that Y1 is at low state. Other outputs are at high state.
4. Apply low level voltage to C and A and apply high level voltage to B. Now check that Y2 is at low state. Other outputs are at high state.
5. Apply low level voltage to C and apply high level voltage to B and A. Now check that Y3 is at low state. Other outputs are at high state.
6. Next, apply high level voltage to C and apply low level voltage to B and A. Now check that Y4 is at low state. Other outputs are at high state.
7. Apply high level voltage to C and A and apply low level voltage to B. Now check that Y5 is at low state. Other outputs are at high state.
8. Next, apply high level voltage to C and B high and apply low level voltage to A. Now check that Y6 is at low state. Other outputs are at high state.
9. Next, apply high level voltage to all the select inputs (C,B,A). Now check that Y7 is at low state. Other outputs are at high state.

Full Adder (Truth-Table)

Inputs		
A	B	C_{in}
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Sum		Carry
S		C_{out}
0		0
1		0
1		0
0		1
1		0
0		1
0		1
1		1

