1. Description

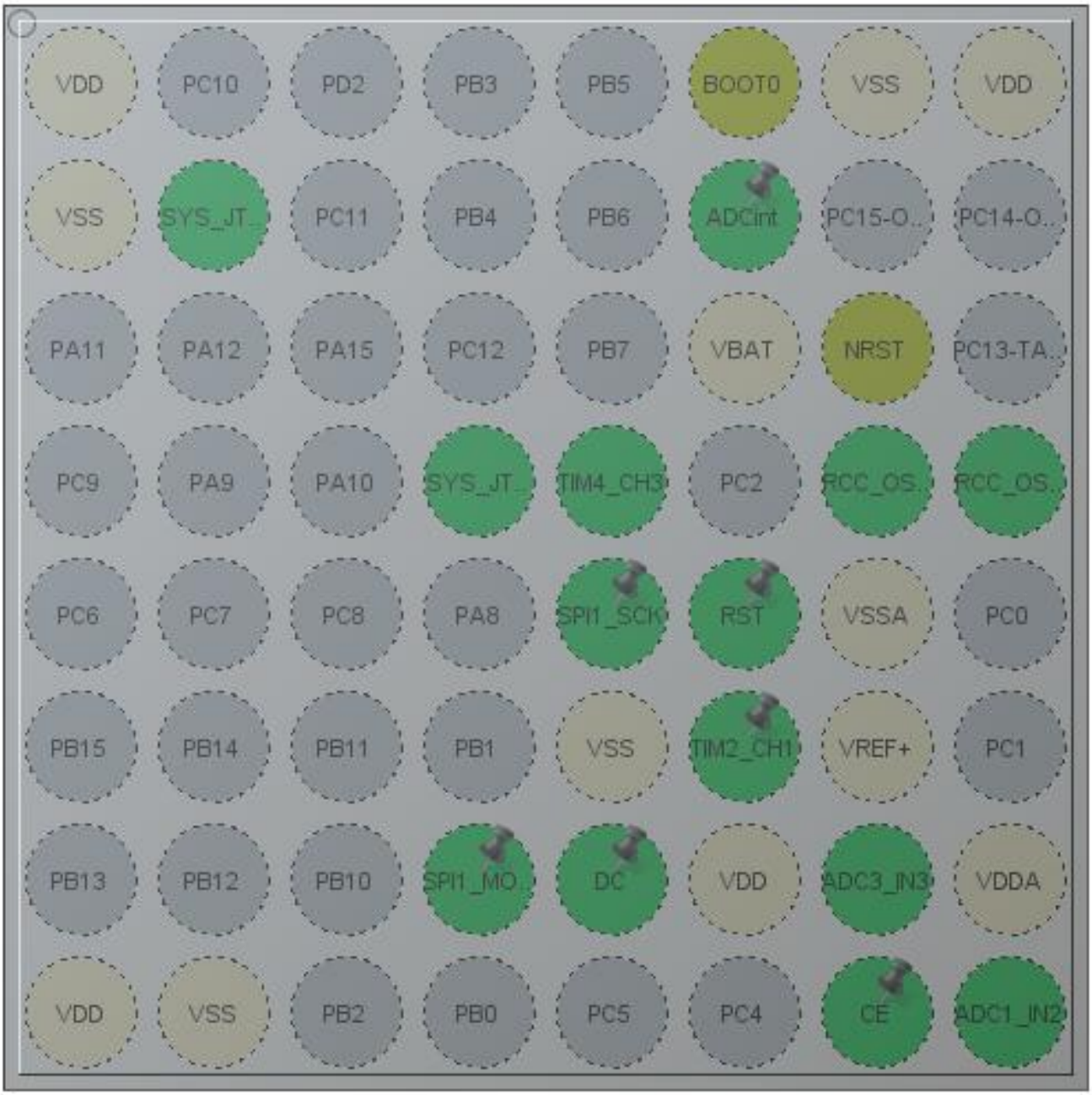
1.1. Project

Project Name	F1_Nokia5110DMA
Board Name	custom
Generated with:	STM32CubeMX 5.6.1
Date	04/12/2020

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103REYx
MCU Package	WLCSP64
MCU Pin number	64

2. Pinout Configuration



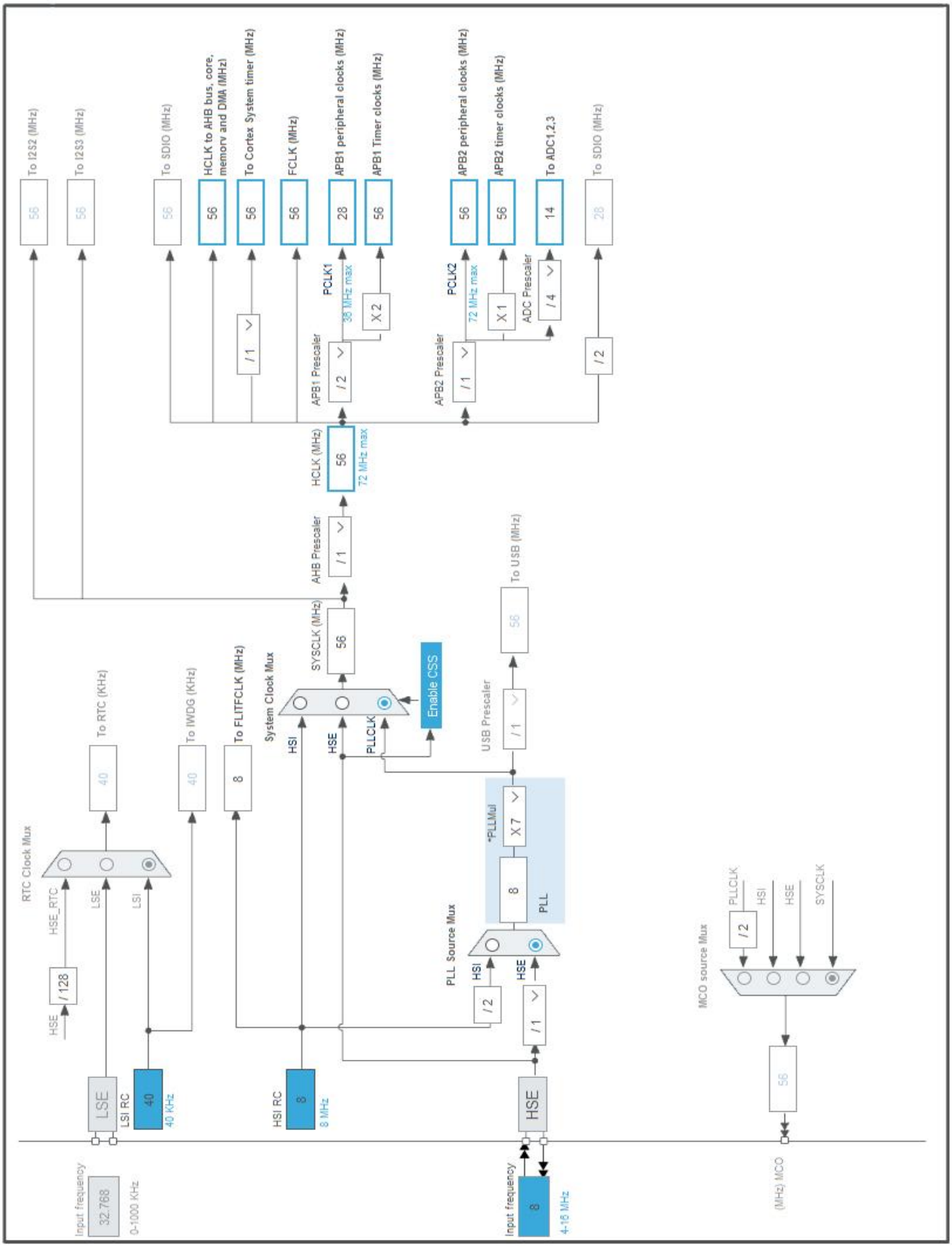
WLCSP64 (Top view)

3. Pins Configuration

Pin Number WLCSP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A1	VDD	Power		
A6	BOOT0	Boot		
A7	VSS	Power		
A8	VDD	Power		
B1	VSS	Power		
B2	PA14	I/O	SYS_JTCK-SWCLK	
B6	PB9 *	I/O	GPIO_Output	ADCint
C6	VBAT	Power		
C7	NRST	Reset		
D4	PA13	I/O	SYS_JTMS-SWDIO	
D5	PB8	I/O	TIM4_CH3	
D7	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
D8	PD0-OSC_IN	I/O	RCC_OSC_IN	
E5	PA5	I/O	SPI1_SCK	
E6	PA1 *	I/O	GPIO_Output	RST
E7	VSSA	Power		
F5	VSS	Power		
F6	PA0-WKUP	I/O	TIM2_CH1	
F7	VREF+	Power		
G4	PA7	I/O	SPI1_MOSI	
G5	PA6 *	I/O	GPIO_Output	DC
G6	VDD	Power		
G7	PA3	I/O	ADC3_IN3	
G8	VDDA	Power		
H1	VDD	Power		
H2	VSS	Power		
H7	PA4 *	I/O	GPIO_Output	CE
H8	PA2	I/O	ADC1_IN2	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	F1_Nokia5110DMA
Project Folder	V:\St Code\F1_Nokia5110DMA
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103REYx
Datasheet	14611 Rev12

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

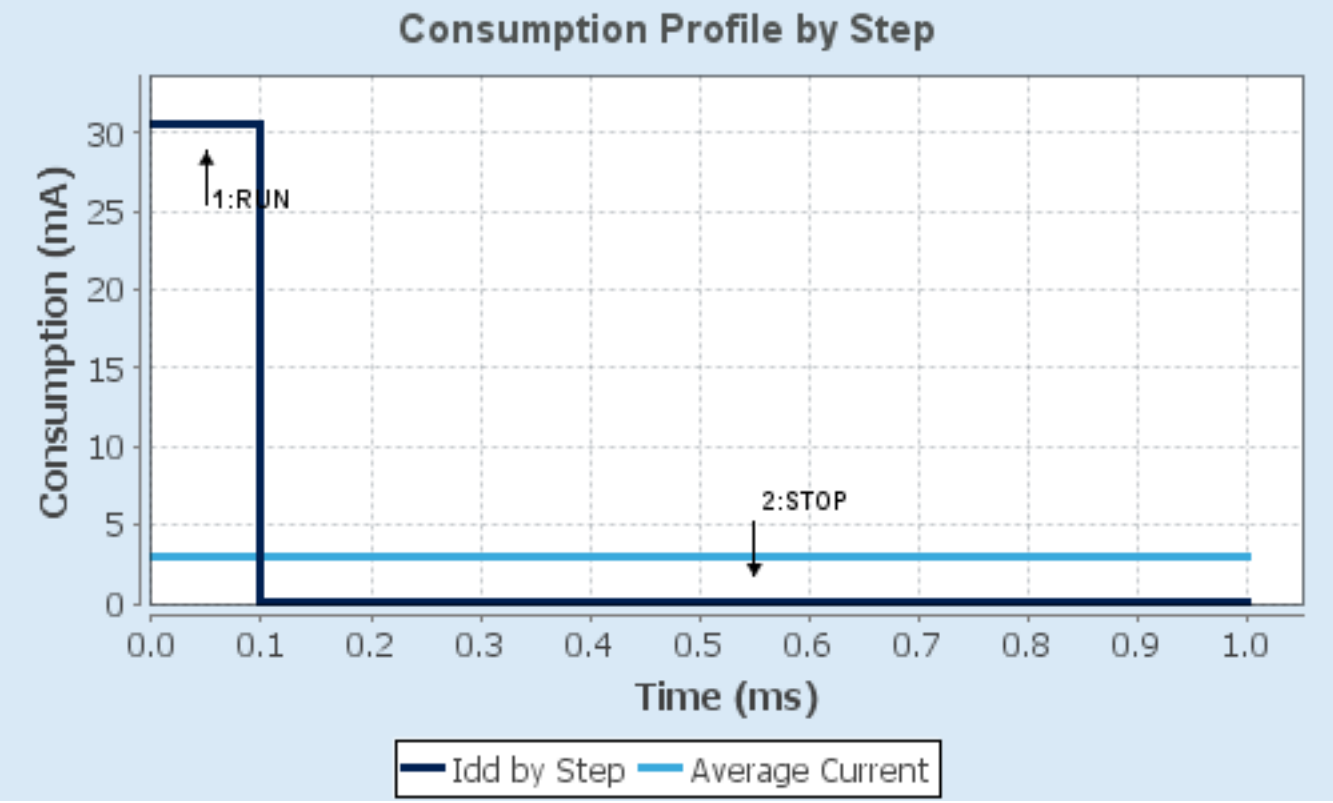
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	30.5 mA	25 µA
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	99.97	105
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN2

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 8 Trigger Out event ***
Rank	1
Channel	Channel 2
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC3

mode: IN3

7.2.1. Parameter Settings:

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	**Timer 8 Trigger Out event ***

Rank	1
Channel	Channel 3
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

WatchDog:

Enable Analog WatchDog Mode	false

7.3. GPIO

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.5. SPI1

Mode: Transmit Only Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**3.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.7. TIM1

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**5599 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.8. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**5 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1000 ***
Output compare preload	Enable
Fast Mode	**Enable ***
CH Polarity	High

7.9. TIM4

mode: Clock Source

Channel3: PWM Generation CH3

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2250 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**1 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.10. TIM8

Clock Source : Internal Clock

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**420 ***

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA2	ADC1_IN2	Analog mode	n/a	n/a	
ADC3	PA3	ADC3_IN3	Analog mode	n/a	n/a	
RCC	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	n/a	**High ***	
	PA7	SPI1_MOSI	Alternate Function Push Pull	n/a	**High ***	
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	**High ***	
TIM4	PB8	TIM4_CH3	Alternate Function Push Pull	n/a	Low	
GPIO	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ADCint
	PA1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RST
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DC
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CE

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_TX	DMA1_Channel3	Memory To Peripheral	Low
ADC1	DMA1_Channel1	Peripheral To Memory	**Very High ***
ADC3	DMA2_Channel5	Peripheral To Memory	**Very High ***

SPI1_TX: DMA1_Channel3 DMA request Settings:

Mode:	Normal
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC3: DMA2_Channel5 DMA request Settings:

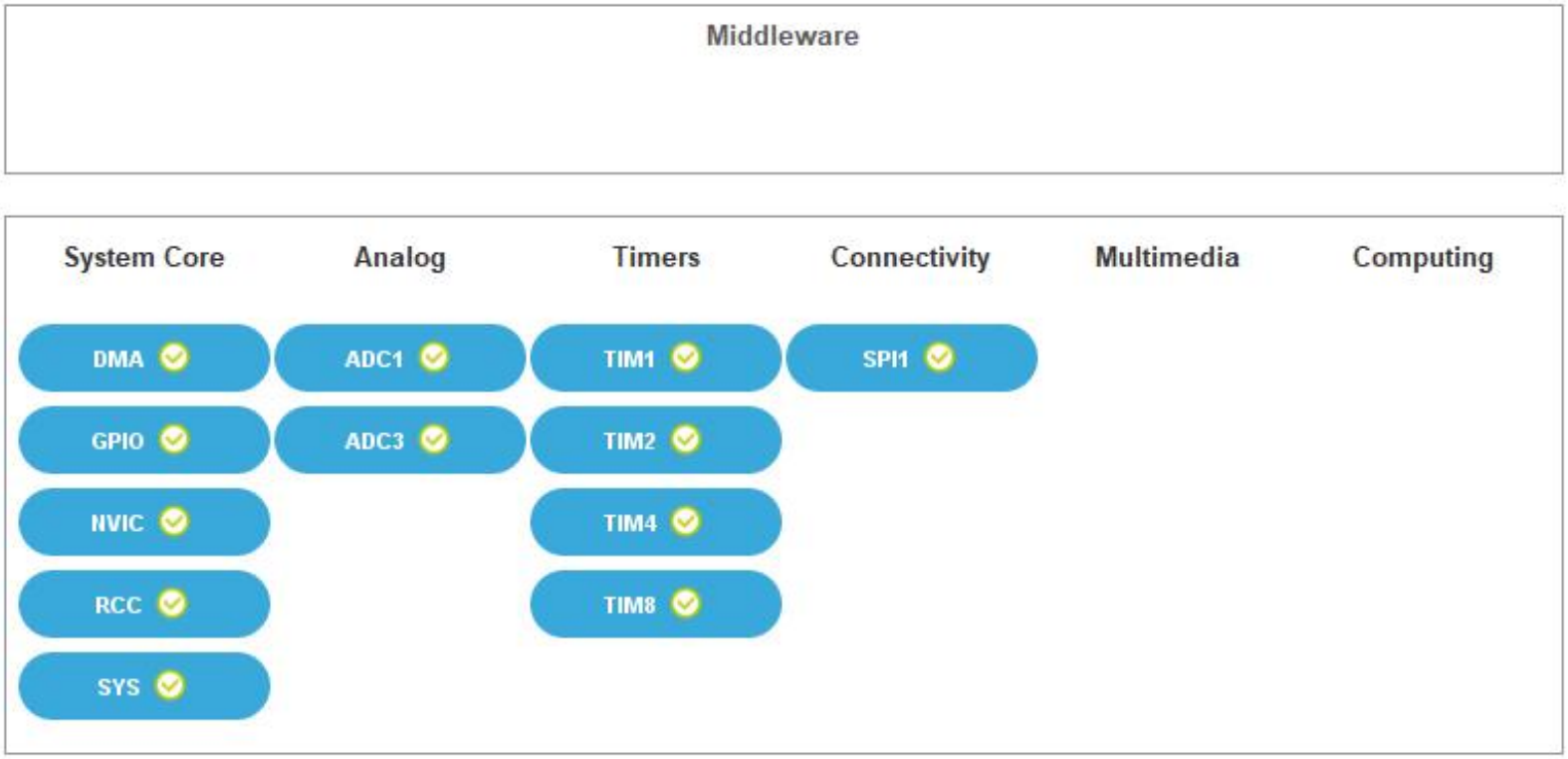
Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel3 global interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	15	0
TIM1 break interrupt	true	0	0
TIM1 update interrupt	true	0	0
TIM1 trigger and commutation interrupts	true	0	0
TIM1 capture compare interrupt	true	0	0
TIM2 global interrupt	true	0	0
ADC3 global interrupt	true	0	0
DMA2 channel4 and channel5 global interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
TIM8 break interrupt	unused		
TIM8 update interrupt	unused		
TIM8 trigger and commutation interrupts	unused		
TIM8 capture compare interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report