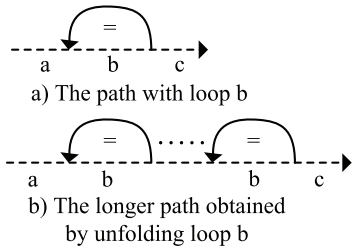
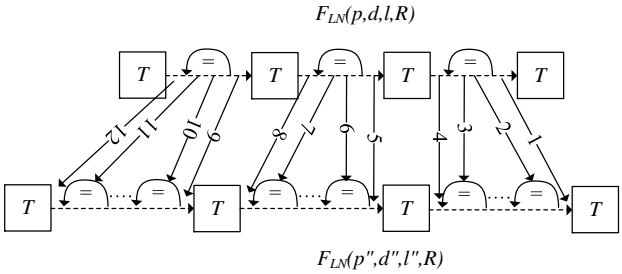
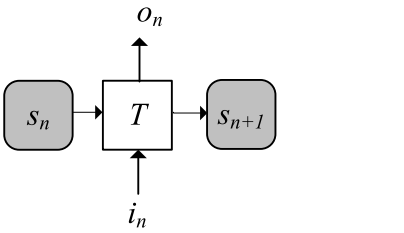
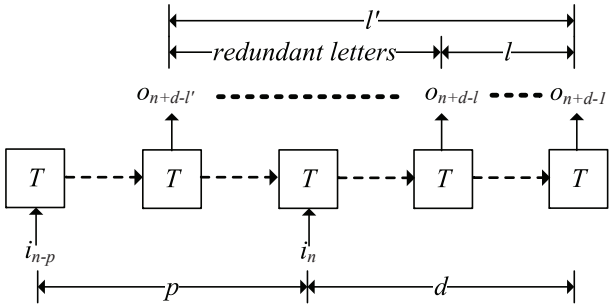
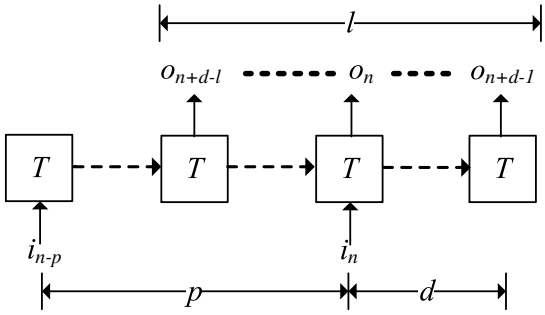


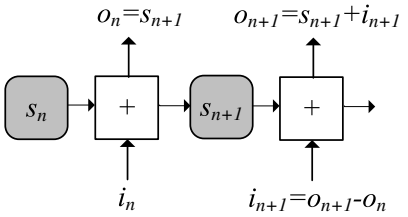




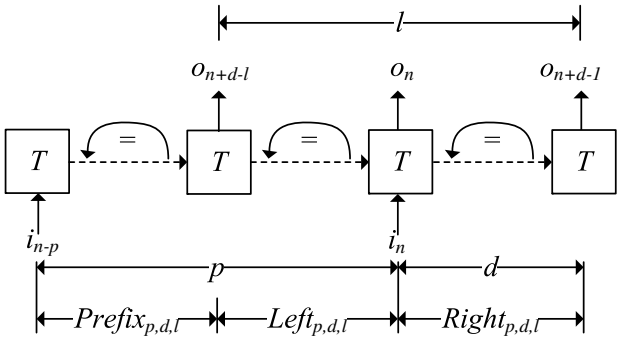




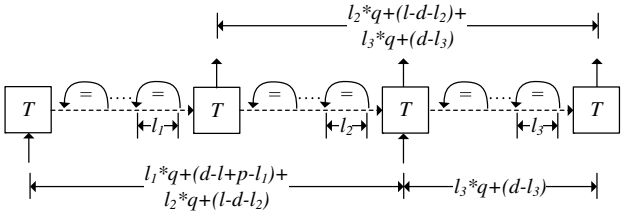
	XGXS	XFI	scrambler	PCI-E	T2 Ethernet
Lines number of Verilog source code	214	466	24	1139	1073
#regs	15	135	58	22	48
Data path width	8	64	66	10	10



		XGXS	XFI	scrambler	PCI-E	T2 Ethernet
[3]	Time to check PC(sec)	1.06	70.52	5.74	2.40	66.37
	d, p, l	1,1,1	0,3,2	0,2,2	2,1,1	4,1,1
This paper	Time to check PC(sec)	0.29	17.86	2.67	0.47	29.64
	improve %	72.64	74.67	53.48	80.42	55.34
	d, p, l	1,2,1	0,3,2	0,2,2	2,2,1	4,4,1



	XGXS	XFI	scrambler	PCI-E	T2 Ethernet
The decoders built manually	921	6002	1629	852	1446
The decoders built by this paper's algorithm	700	12754	1455	455	552



	XGXS	XFI	scrambler	PCI-E	T2 Ethernet
The decoders built manually	12.33	46.65	6.54	19.03	23.36
The decoders built by this paper's algorithm	11.96	28.13	6.54	9.09	12.69

	XGXS	XFI	scrambler	PCI-E	T2 Ethernet
The algorithm of [3](sec)	0.98	35.08	2.54	1.36	17.39
This paper's algorithm(sec)	0.16	7.59	1.17	0.33	2.19
improve %	83.67	78.36	53.94	75.74	87.41