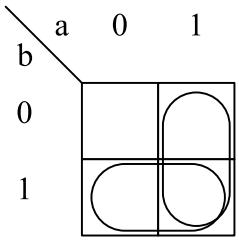
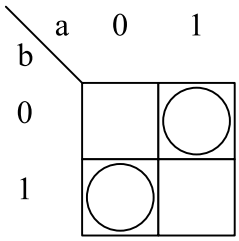
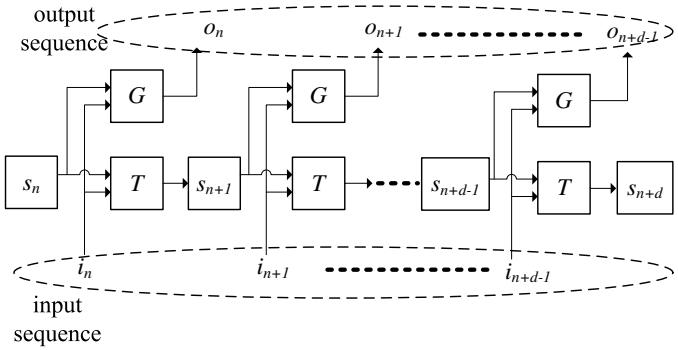
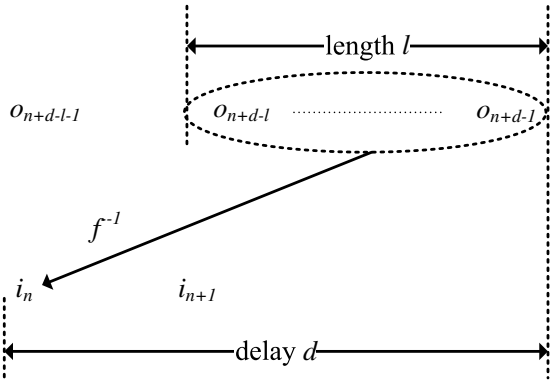


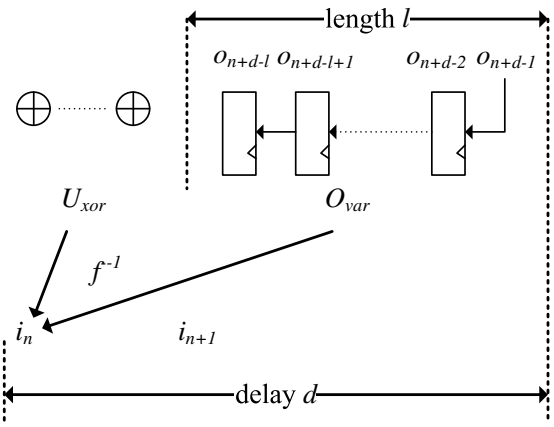
a) OR



b) XOR


output
sequence
o_n
o_{n+1}
o_{n+d-1}
G
G
G
s_n
T
s_{n+1}
T
s_{n+d-1}
T
s_{n+d}
i_n
i_{n+1}
i_{n+d-1}
input
sequence


length l
$o_{n+d-l-1}$
o_{n+d-l}
o_{n+d-1}
f^{-l}
i_n
i_{n+1}
delay d


length l
o_{n+d-l} $o_{n+d-l+1}$
o_{n+d-2} o_{n+d-1}
U_{xor}
O_{var}
f^{-1}
i_n
i_{n+1}
delay d

	XGXS	XFI	scrambler	PCIE	T2 ethernet
Line number of verilog source code	214	466	24	1139	1073
#regs	15	135	58	22	48
Data path width	8	64	66	10	10

	XGXS	XFI	scra-mbler	PCIE	T2 et-hernet
run time (seconds)	0.51	71.60	2.51	32.74	44.48
d	1	0	0	2	4
p	0	3	1	1	0
l	1	2	2	1	1

		XGXS	XFI	scrambler	PCIE	T2 ethernet
BFL only	time(s)	32.67	time out	8.56	time out	time out
BFL + XORMIN	time(s)	1.52	2939.47	11.97	47.55	36.64
	$\|F_E\|$	25470	5084496	499200	52209	459204
	#SAT	984	137216	8320	528	1032
BFL+ XORMIN +UNSAT	time(s)	1.08	752.83	1.84	0.82	27.08
	$\|F_E^v\|$	6694	188717	4807	6635	51204
	#SAT	480	16828	256	243	538

	XGXS	XFI	scrambler	PCIE	T2 ethernet
hand-written decoders	913	4886	1514	952	2225
decoders built by Shen[6]	667	15269	1302	344	661
decoders built by our algorithm	652	16659	1302	345	569

	XGXS	XFI	scrambler	PCIE	T2 ethernet
hand-written decoders	12.33	46.65	6.54	19.03	23.36
decoders built by our algorithm	13.23	58.73	6.54	8.07	17.07