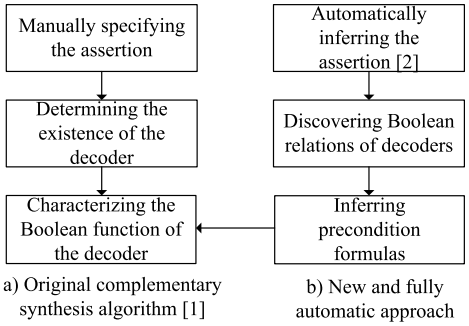

Fig. 1. The original and new flows of complementary synthesis

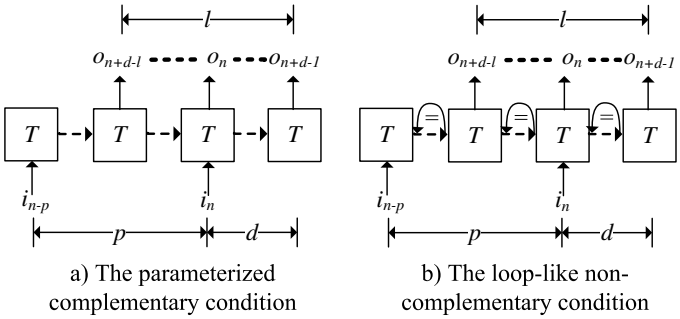

Fig. 2. The parameterized complementary condition and the loop-like non-complementary condition

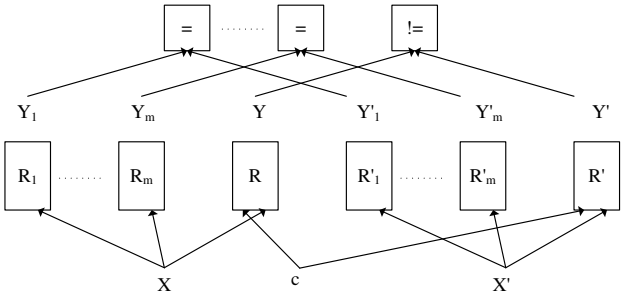

Fig. 3. The SAT instance that discovers decoders

TABLE I
INFORMATION ON BENCHMARKS

	XGXS	XFI	scrambler	PCIE	T2 Ethernet
#line of verilog	214	466	24	1139	1073
#regs	15	135	58	22	48
Data path width	8	64	66	10	10
#Config pin	3	120	1	16	26

TABLE II
EXPERIMENTAL RESULTS

		XG-XS	XFI	scra-mbler	PCI-E	T2 E-ther
[10]	Runtime(sec)	0.07	17.84	2.70	0.47	30.59
	d, p, l	1,2,1	0,3,2	0,2,2	2,2,1	4,2,1
this paper	Runtime 1	4.53	264.19	13.03	10.39	426.12
	Runtime 2	0.11	12.11	1.26	0.27	3.07
	Runtime 3	0.13	13.69	1.49	0.23	2.86
	d, p, l	1,5,1	0,5,2	0,5,2	2,5,1	4,5,1