25-Dec-2011

Dear Dr. Shen:Manuscript ID TCAD-2011-0407.R1 entitled "Inferring Assertion for Complementary Synthesis" which you submitted to the Transactions on Computer-Aided Design of Integrated Circuits and Systems, has been reviewed. The comments of the reviewer(s) are included at the bottom of this letter.

The reviewer(s) suggest some minor revisions to your manuscript. I invite you to respond to their comments and revise your manuscript.

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You will be unable to make your revisions on the originally submitted version of the manuscript. Instead, revise your manuscript using a word processing program and save it on your computer. Please also highlight the changes to your manuscript within the document by using bold, underlined, or colored text.

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When submitting your revised manuscript, you will be able to respond to the comments made by the reviewer(s) in the space provided. You can use this space to document any changes you make to the original manuscript. In order to expedite the processing of the revised manuscript, please be as specific as possible in your response to the reviewer(s).

IMPORTANT: Your original files are available to you when you upload your revised manuscript. Please delete any redundant files before completing the submission.

Because we are trying to facilitate timely publication of manuscripts submitted to the Transactions on Computer-Aided Design of Integrated Circuits and Systems, your revised manuscript should be submitted by 29-Jan-2012. If it is not possible for you to submit your revision by this date, we may have to consider your paper as a new submission.

Once again, thank you for submitting your manuscript to the Transactions on Computer-Aided Design of Integrated Circuits and Systems and I look forward to receiving your revision.

Sincerely,
Prof. Sachin Sapatnekar
Editor-in-Chief, Transactions on Computer-Aided Design of Integrated Circuits and Systems
tcad@umn.edu

Reviewer(s)' Comments to Author:

Reviewer: 1
Comments to the Author
The authors addressed my comments.
REPLY TO REVIEWER:
Thank you very much for your effort in polishing this paper.

Reviewer: 2
Comments to the Author
You have not answered my objection about enumeration of reversible encoders. (The most complex assertion you get consists of 6 variables. Finding the right assignment should be trivial.) There are three ways to address this objection.

1) You just admit that for the examples you tried enumeration of reversible encoders does not have much practical value but you believe that it may come useful in the future. You also give a plausible scenario where such enumeration becomes practical.

2) You give an example (that you have not described in the current manuscript) where enumeration of reversible encoders satisfying your assertion is really helpful

3) You remove the part about enumeration of encoders from the paper.

REPLY TO REVIEWER:
According to the last row of table I, these benchmarks have 16, 26 or even 120 configuration pins. It is definitely non-trivial to find the right assignments for so many pins. Therefore, the ability to infer an assertion with small number of variables from large number of configuration pins indicates exactly the power of our algorithm.
At the same time, for the most complex XFI encoder with 120 configuration pins, the user can easily select the correct decoder by inspecting only 2 pins, instead of all 120 pins.
Please also refer to page 1, right column paragraph 4, which starts with "For example", and also the subsection V.C.

Reviewer: 3
Comments to the Author
Thanks for the clarification. However the following comments remain to be further clarified.

1. (Prior Comment 4: In Section IV.C, computing f using Craig interpolation may seem unnecessary as cofactoring f' already yields a desired solution. Having Craig interpolation in the computation may seem just the matter of speedup as stated in the last sentence of Section IV. If this is the case, please provide experimental evaluation comparing the computation with and without Craig interpolation.)

Please make room based on the suggestions below for a brief comparison on computations with and without Craig interpolation. Selecting one representative circuit to discuss is sufficient to let the reader gain some insights.

REPLY TO REVIEWER:
Actually, the Craig interpolation is used not only to speed up the computation, it is also used to get the formula *na* in step 9 of Algorithm 1. These *na* are used to compute the final assertion in step 5.
So Craig interpolation cannot be avoided in our algorithm.

2. (Prior Comment 6: For Section VI, there are no additional experiments compared to [2]. Essentially only Phase 1 is experimented. Please experiments on Phase 2 and Phase 3 computations as well. Showing statistics of the computed Boolean relations and their assertions (in terms of formula size, CPU time, etc.) provides the reader a better idea how the proposed algorithms work in practice.)

Please report the runtimes of Phases 1-3 separately.

REPLY TO REVIEWER:
I have changed it according to your suggestions. Please refer to table II and the third paragraph of Subsection V.A.

3. (Prior Comment 8: XFI and scrambler have 2 decoders each. Please list their respective two assertions, rather than just one each. (Prior Comment 9) How can scrambler have 2 decoders with its assertion equals "True"? It seems that the assertions of different decoders must be disjoint.)

What is the difference between "precondition formulas" and "inferred assertions"? While they seem to be the same, the shown formulas of XFI and scrambler in Section V.B and Section V.C in this revision are not well related. Please discuss their connections.

REPLY TO REVIEWER:
It is my fault that I had not presented it clearly.
Please refer to the paragraph under the Equation (7), which starts with "Two different". Actually, a decoder R_i 's precondition formula IA_i is the set of configuration letters that leads to the existence of R_i. So the union of all such IA_i should be equal to the assertion IA inferred by Algorithm 1. This is also indicated by the experimental result in Subsection V.C.
In the last submission (the 2nd submission) of this paper, the union of IA_1 and IA_2 of XFI is not equal to IA, this was caused by a bug in the implementation of my AIG package.
This bug causes two problems in the last submission:

1 **The Inferred assertion of XFI includes an additional sub-formula TEST_MODE. This problem does not exist in current submission(the 3rd submission). Please refer to Subsection V.B.**
2 **The first precondition formula IA_1 of XFI was RESET &!TEST_MODE & !DATA_VALID in the last submission. It is not correct, and now it is corrected and is RESET &!TEST_MODE in this submission. Please refer to the third paragraph of Subsection V.C.**

The correction of this bug also leads to the change of the inferred assertion of T2_ether benchmark in Subsection V.B . But the new assertion is logically equivalent to that of the last submission.

4. Please explain the runtime differences (especially the substantial slow-downs of XFI and T2 Ether) between this new version and prior submitted version. Is it due to bug fixing or other reasons?

REPLY TO REVIEWER:
Yes, there is a deeply hidden bug in the program of the first submission. The encoding space of two totally unrelated SAT instances are overlapped with each other, so the result of merging these two SAT instances was not equal to their conjunction.
I correct this bug in the program of the second submission, which had led to significantly larger runtime overhead.
In the last two month, I had further improved the runtime overhead of my program, so it is much faster now in current submission. Please refer to Table II.

Other suggestions:

P1. "i) Manually specifying …" -> "i) manually specifying …"

P1. "me" -> "the first author"

P1. "… pins, in which only two have …" -> "… pins, only two of which have …"

P1. "these TWO pin" -> "these two pins"

REPLY TO REVIEWER: All are changed. Thank you for your suggestions.

P4. Table I can be removed by referring to [2] (with "#Config pin" info moved back to Table II) to make room for further clarification.

REPLY TO REVIEWER: According to our explanation about Craig interpolation, we don't need to make room any more.

P5. The last paragraph of Section V.C (as it repeats what was said in Section I) can be removed to make room for further clarification.

REPLY TO REVIEWER: I remove this paragraph to make room for explaining the issue 3.

Associate Editor: Kunz, Wolfgang
Comments to the Author:
Your paper has improved but requires another revision. The reviewers give specific suggestions. In case you should decide not to follow any of these suggestions in your revision please explain this carefully in your rebuttal.