

Curriculum vitae

Name : ShengYu Shen

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Summary :

I am a lead ASIC design engineer of NUDT with 17 years experience and 11 successfully taped out chips, including nnARM processor compatible with ARM 926, a DSP compatible with TI TMS320C30, and many router and PCIE interface chips used in TianHe supercomputers that were ranked as the 1st place in Top500 list for 6 times.

I am also an associated professor of National University of Defense Technology (NUDT) leading a formal method research team that focuses on high level synthesis, model checking, theorem proving and static analysis. And I have published lots of papers on top ranked journals and conferences, such as TCAD, TODAES, ICCAD, DATE, ASPDAC, FMCAD, VMCAI and CHARM.

Education:

2005 Ph.D., Computer Science, National University of Defense Technology(NUDT)

2000 M.S., Computer Science, National University of Defense Technology(NUDT)

1997 B.S., Computer Science, National University of Defense Technology(NUDT)

Skills:

- Computer architecture, including pipeline, cache, MMU, bus and software/hardware interface;
- Formal methods including high level synthesis, model checking, theorem proving, static analysis, SAT/SMT, BDD and Craig interpolant;
- Error correction code, including Reed-Solomon and convolution code;
- Chip design and verification, including emulation, synthesis, timing, ECO, assertion based formal verification, simulation and UVM;
- Low latency and high bandwidth physical coding sub-layer(PCS) binding multiple lanes for Intel QPI, Ethernet and TianHe supercomputer's proprietary communication protocol;
- Programming languages including C++, OCaml, TCL, Perl, Verilog, SystemVerilog and PSL;
- Good English communication skills, both written and verbal;
- Technology writing with Latex.

Engineering Experience :

2010-2014: Lead engineer of NUDT in 6 chip projects, including 4 router and PCIE interface chips for TianHe supercomputers with 14~25G Serdes, and a cache coherence node controller chip for Intel QPI protocol, and a 40Gbps serdes test chip. I also designed physical coding sub-layer and forward error correction modules for these chips with up to 20 lanes and 40Gbps each lane. And I also performed synthesis, STA, equivalent checking and ECO for these chips. And I also coordinates out-sourced backend teams across China, India, Singapore and US.

2005-2009: Senior ASIC design engineer of NUDT in 4 router and PCIE interface chip projects for TianHe supercomputers with 3.125~10G Serdes. And I also performed synthesis, STA, equivalent checking and ECO. And I also coordinates out-sourced backend teams.

2001-2003: Ph.D. candidate of NUDT designing nnARM processor compatible with ARM 926 and porting Linux to it. This chip was taped out with TSMC 0.18 process and ran at 300Mhz. Please refer to http://www.eetimes.com/document.asp?doc_id=1144157 for details.

1997-2000: Postgraduate of NUDT designing a floating point multiplier for a TI TMS320C30 compatible DSP project. And I further boost frequency of this multiplier with wave pipelining technology by developing Verilog parser and latency balancing algorithm.

Academic Research Experience:

2007-2014: Developing complementary synthesis algorithm [1-7] that automatically generates decoder from encoders of communication protocols, such as Ethernet and PCI Express. It parses the encoder's source code, iteratively unrolls its transition relation, decides the decoder's existence by iteratively building the monotonically converging over-approximation and under-approximations of the state space, and generates the decoder's Boolean function with Craig interpolant. Please refer to <https://github.com/shengyushen/compsyn> for these algorithms.

2003-2006: Developing counterexample minimizing algorithms[8-12] used in counterexample-guided abstraction and refinement framework. It backtracks the implication graph of the SAT solver to find out the relevant clauses, which leads to a smaller counterexample.

1997-2000: Developing wave pipelining algorithm that boosting circuit frequency by balancing latency along different paths.

Academic Publications:

Journals:

1. ShengYu Shen: **Inferring Assertion for Complementary Synthesis**. IEEE Transactions on CAD of Integrated Circuits and Systems 31(8): 1288-1292 (2012)
2. ShengYu Shen: **A Halting Algorithm to Determine the Existence of the Decoder**. IEEE Transactions on CAD of Integrated Circuits and Systems 30(10): 1556-1563 (2011)
3. ShengYu Shen: **Synthesizing Complementary Circuits Automatically**. IEEE Transactions on CAD of Integrated Circuits and Systems 29(8): 1191-1202 (2010)
4. Ying Qin, ShengYu Shen: **Complementary Synthesis for Encoder with Flow Control Mechanism**. ACM Transactions on Design Automation of Electronic Systems (TODAES) Volume 21 Issue 1, November 2015. Article No. 12

Conferences:

5. ShengYu Shen: **Inferring assertion for complementary synthesis**. ICCAD 2011: 404-411
6. ShengYu Shen: **A halting algorithm to determine the existence of decoder**. FMCAD 2010: 91-99
7. ShengYu Shen: **Synthesizing complementary circuits automatically**. ICCAD 2009: 381-388
8. ShengYu Shen: **A fast counterexample minimization approach with refutation analysis and incremental SAT**. ASP-DAC 2005: 451-454
9. ShengYu Shen: **Minimizing Counterexample of ACTL Property**. CHARME 2005: 393-397
10. ShengYu Shen: **A Faster Counterexample Minimization Algorithm Based on Refutation Analysis**. DATE 2005: 672-677

11. ShengYu Shen: **Minimizing Counterexample with Unit Core Extraction and Incremental SAT**. VMCAI 2005: 298-312
12. ShengYu Shen: **Localizing Errors in Counterexample with Iteratively Witness Searching**. ATVA 2004: 456-469

Honors and Awards:

1. Distinguished Award of National Science and Technology Progress, for developing TianHe supercomputer, 2014.
2. Distinguished Doctoral Thesis at NUDT, 2007.

Research Grants:

1. Automatically Complementary Synthesis for Communication Application (Sponsored by Chinese NSF, 2011-2013)
2. Fixing Program with Counterexample Minimization(Sponsored by Chinese NSF, 2007-2009)

Seeking Jobs:

1. CPU/DSP design and verification engineer.
2. Research staff or lead engineer developing formal method tools.