Complementary Synthesis for Encoder with Flow Control Mechanism

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Complementary synthesis automatically generates an encoder's decoder with the assumption that the encoder's all input variables can always be uniquely determined by its output symbol sequence. However, many modern encoders employ flow control mechanism that fail this assumption. Such encoders, when its output symbol sequence is too fast to be processed by the decoder, will stop outputting data symbols, but instead output an idle symbol that can only uniquely determine a subset of the encoder's input variables. And the decoder should recognize and discard this idle symbol. Although this mechanism can prevent losing data symbols, it fail the assumption of all complementary synthesis algorithm, because some input variables can not be uniquely determined by the idle symbol.

This paper proposes the first algorithm to handle such encoders with flow control mechanism. **First**, it identifies all input variables that can be uniquely determined, and take them as flow control variables. **Second**, it infers a predicate over these flow control variables, that enables all other input variables to be uniquely determined. **Third**, the decoder's Boolean function for flow control variablescan be characterized with Craig interpolant. For other input variables, the inferred predicate must be enforced before characterzing their Boolean function with Craig interpolant.

Experimental results on several complex encoders indicate that our algorithm can always correctly identify the flow control variables, infer the predicates and generate the decoder's Boolean functions.

Categories and Subject Descriptors: B.5.2 [**Design Aids**]: Automatic synthesis; B.6.3 [**Design Aids**]: Automatic synthesis

General Terms: Algorithms, Logic synthesis, Verification

Additional Key Words and Phrases: Craig interpolation, decoder, encoder, finite-state transition system, satisfiability solving

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1. INTRODUCTION

One of the most difficult jobs in designing communication and multimedia chips is to design and verify complex encoder and decoder pairs. The encoder maps its input variables $\vec{i}$ to its output variables $\vec{o}$, while the decoder recovers $\vec{i}$ from $\vec{o}$. **Complementary synthesis [Shen et al. 2009;2010; 2011; 2012;Liu et al. 2011;2012;Tu and Jiang 2013] try to ease this job by automatically generating a decoder from**

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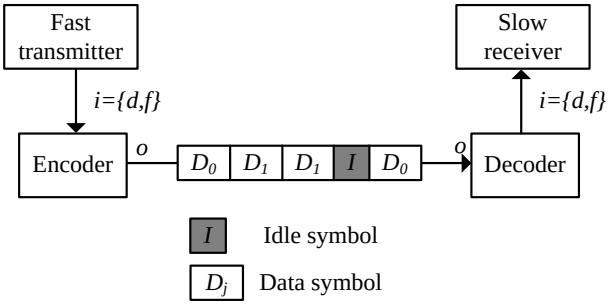
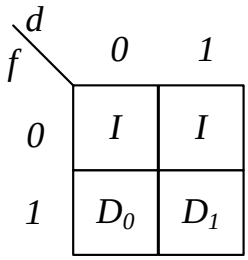


a) The faster transmitter and slower receiver connected by the encoder and decoder



b) The encoding table of the encoder with flow control mechanism

Fig. 1. An encoder with flow control mechanism

an encoder's specification, with the assumption that $\vec{i}$ can always be uniquely determined by a bounded sequence of $\vec{o}$.

However, the encoders of many high speed communication systems employ flow control mechanism [Abts and Kim 2011] that fails this assumption. Figure 1a) shows the structure of a communication system with flow control mechanism, which include a faster transmitter and a slower receiver connected by a pair of encoder and decoder. There are two input variables from the transmitter to the encoder: the data bit d to be encoded, and the flow control bit f indicating the validness of d. Figure 1b) shows the encoding table of the encoder with flow control mechanism, which maps f and d to the output symbol $\vec{o}$.

The flow control mechanism prevent the faster transmitter from overwhelming the slower receiver in the following way. When the receiver can keep up with the transmitter, f will be 1, and the decoder can always recover both f and d according to Figure 1b). But when the receiver can not keep up with the transmitter, the transmitter will drop f to 0 to stop transmitting new D_i, but instead transmitting the idle symbol I without considering the value of d. And the decoder should discard this idle symbol I, and send $f \equiv 0$ to the receiver with whatever value on d.

This mechanism can prevent the faster transmitter from transmitting to many data that can not be handled by the slower receiver. But it fail the assumption of all current complementary synthesis algorithms [Shen et al. 2009;2010; 2011; 2012;Liu et al. 2011;2012;Tu and Jiang 2013], because d can not be uniquely by the idle symbol I. It is obvious that, to resolve this problem and generate the decoder, we only need to consider the case $f \equiv 1$, the predicate that enable d to be uniquely determined. For other case $f \equiv 0$, d is not need by the receiver and can be any value.

Thus, according to this insight, we propose in this paper the first complementary synthesis algorithm to handle encoders with flow control mechanism in three steps: **First**, it applies the classical halting complementary synthesis algorithm [Shen et al. 2011] to identify all the input variables of the encoder that can be uniquely determined, and call them the flow control variables $\vec{f}$. Other input variables that can not be uniquely determined is called the data variables $\vec{d}$. **Second**, it infers a sufficient and necessary predicate $valid(\vec{f})$ that enables $\vec{d}$ to be uniquely determined by a bounded sequence of the encoder's output variables $\vec{o}$. **Finally**, it characterizes the decoder's Boolean function that computes each flow control variable $f \in \vec{f}$ by building a Craig

interpolant[McMillan 2003]. On the other hand, for other data variables $\vec{d}$, their values are meaningful only when $valid(\vec{f}) \equiv 1$. Thus, the decoder's Boolean functions that compute each $d \in \vec{d}$ can be built similarly, but only after enforcing $valid(\vec{f}) \equiv 1$.

The second step of this algorithm seems somewhat similar to that of [Shen et al. 2012] in the sense that both algorithms infer predicates that enable $\vec{d}$ or $\vec{i}$ to be uniquely determined. But the essential difference between them is that the algorithm of [Shen et al. 2012] infers a global assertion that must be enforced on all the steps along the unrolled transition relation, while our algorithm infers a local predicate that is only enforced at the current step when we need to recover the value of $\vec{d}$. Thus, our algorithm can be seen as a generalization of [Shen et al. 2012].

Experimental results indicate that, for several complex encoders from real projects (e.g., Ethernet [IEEE 2012] and PCI Express [PCI-SIG 2009]), our algorithms can always correctly identify the flow control variables, infer the predicates and generate the decoders.

The remainder of this paper is organized as follows. Section 2 introduces the background material; Section 3 presents the algorithm that identifies the flow control variables, while Section 4 infers the predicate that enables $\vec{d}$ to be uniquely determined by a bounded sequence of $\vec{o}$; Section 5 presents the algorithm to characterize the decoder's Boolean function; Sections 6 and 7 present the experimental results and related works; Finally, Section 8 sums up the conclusion.

2. PRELIMINARIES

2.1. Propositional satisfiability

The Boolean value set is denoted as $B = \{0, 1\}$. A vector of variables is represented as $\vec{v} = (v, \ldots)$. The number of variables in $\vec{v}$ is denoted as $|\vec{v}|$. If a variable v is a member of $\vec{v}$, that is $\vec{v} = (\ldots, v, \ldots)$, then we say $v \in \vec{v}$; otherwise we say $v \notin \vec{v}$. For a variable v and a vector $\vec{v}$, if $v \notin \vec{v}$, then the new vector that contains both v and all members of $\vec{v}$ is denoted as $v \cup \vec{v}$. If $v \in \vec{v}$, then the new vector that contains all members of $\vec{v}$ except v, is denoted as $\vec{v} - v$. For the two vectors $\vec{a}$ and $\vec{b}$, the new vector with all members of $\vec{a}$ and $\vec{b}$ is denoted as $\vec{a} \cup \vec{b}$. The set of truth valuations of $\vec{v}$ is denoted as $[\![\vec{v}]\!]$, for instance, $[\![(v_1, v_2)]\!] = \{(0, 0), (0, 1), (1, 0), (1, 1)\}$.

A Boolean formula F over a variable set V is constructed by connecting variables from V with symbols $\neg$, $\wedge$, $\vee$ and $\Rightarrow$, which stand for logical connectives negation, conjunction, disjunction, and implication, respectively.

The propositional satisfiability problem(abbreviated as SAT) for a Boolean formula F over a variable set V is to find a satisfying assignment $A : V \to B$, so that F can be evaluated to 1. If such a satisfying assignment exists, then F is satisfiable; otherwise, it is unsatisfiable.

According to [Ganai et al. 2004a], the positive and negative cofactors of $f(v_1 \ldots v \ldots v_n)$ with respect to variable v are $f_v = f(v_1 \ldots 1 \ldots v_n)$ and $f_{\overline{v}} = f(v_1 \ldots 0 \ldots v_n)$, respectively. **Cofactoring** is the action that applies 1 or 0 to v to get f_v or $f_{\overline{v}}$.

Given two Boolean formulas ϕ_A and ϕ_B, with $\phi_A \wedge \phi_B$ unsatisfiable, there exists a formula ϕ_I referring only to the common variables of ϕ_A and ϕ_B such that $\phi_A \Rightarrow \phi_I$ and $\phi_I \wedge \phi_B$ is unsatisfiable. We call ϕ_I the **interpolant**[Craig 1957] of ϕ_A with respect to ϕ_B and use McMillan's algorithm [McMillan 2003] to generate it.

2.2. Finite state machine

The encoder is modeled by a finite state machine(FSM) $M = (\vec{s}, \vec{i}, \vec{o}, T)$, consisting of a state variable vector $\vec{s}$, an input variable vector $\vec{i}$, an output variable vector $\vec{o}$, and a

transition function $T : [\![\vec{s}]\!] \times [\![\vec{i}]\!] \rightarrow [\![\vec{s}]\!] \times [\![\vec{o}]\!]$ that computes the next state and output variable vector from the current state and input variable vector.

The behavior of FSM M can be reasoned by unrolling transition function for multiple steps. The state variable $s \in \vec{s}$, input variable $i \in \vec{i}$ and output variable $o \in \vec{o}$ at the n-th step are respectively denoted as s_n, i_n and o_n. Furthermore, the state, the input and the output variable vectors at the n-th step are respectively denoted as $\vec{s}_n$, $\vec{i}_n$ and $\vec{o}_n$. A **path** is a state sequence $< \vec{s}_n, \ldots, \vec{s}_m >$ with $\exists \vec{i}_j \vec{o}_j (\vec{s}_{j+1}, \vec{o}_j) \equiv T(\vec{s}_j, \vec{i}_j)$ for all $n \leq j < m$. A **loop** is a path $< \vec{s}_n, \ldots, \vec{s}_m >$ with $\vec{s}_n \equiv \vec{s}_m$.

2.3. The halting algorithm to determine if an input variable can be uniquely determined by a bounded sequence of output variable vector

All the state-of-the-art complementary synthesis algorithms [Shen et al. 2009;2010; 2011; 2012;Liu et al. 2011;2012;Tu and Jiang 2013] assume that $\vec{i}$ can be uniquely determined, so they always take $\vec{i}$ as a whole, and never consider individual variables $i \in \vec{i}$. But in this paper, we need to check each $i \in \vec{i}$ one by one, so there may be minor differences between our presentation and that of [Shen et al. 2009;2010; 2011; 2012;Liu et al. 2011;2012;Tu and Jiang 2013].

The first such halting algorithm is proposed in [Shen et al. 2011]. Its basic idea is to unroll the transition relation into longer and longer length. And for each length, we use two approximated approaches to determine the answer, the first is a sound one that presented in 2.3.1, while the second is a complete one presented in 2.3.2. That is, when the first says **YES** then the answer is **YES**, and when the second approach says **NO** then the answer is **NO**. And we will show in 2.3.3 that these two approach will eventually converge and give conclusive answer at some particular unrolling length.

*2.3.1. **The sound approach**. .*

As shown in Figure 2, on the unrolled transition relations, an input variable $i \in \vec{i}$ can be uniquely determined, if there exist three integers p, l and r, such that for any particular valuation of the output sequence $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$, i_{p+l} cannot take on two different values. This can be checked by solving $F_{PC}(p, l, r)$ in Equation (1).

$$F_{PC}(p,l,r) := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r} \{(\vec{s}_{m+1}, \vec{o}_m) \equiv T(\vec{s}_m, \vec{i}_m)\} \\ \wedge & \bigwedge_{m=0}^{p+l+r} \{(\vec{s'}_{m+1}, \vec{o'}_m) \equiv T(\vec{s'}_m, \vec{i'}_m)\} \\ \wedge & \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \\ \wedge & i_{p+l} \neq i'_{p+l} \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i}_m) \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i'}_m) \end{array} \right\} \quad (1)$$

Here, p is the length of the prefix state transition sequence. l and r are the lengths of the two output sequences $< \vec{o}_{p+1}, \ldots, \vec{o}_{p+l} >$ and $< \vec{o}_{p+l+1}, \ldots, \vec{o}_{p+l+r} >$ that are on the left-hand and right-hand sides of i_{p+l}, which is used to determine i_{p+l}. Line 1 of Equation (1) corresponds to the left path in Figure 2, while Line 2 corresponds to the right path in Figure 2. These two paths are of the same length. Line 3 forces these two paths' output sequences to be the same, while Line 4 forces their i_{p+l} to be different. **Line 5 and 6 are the assertion predicates given by the user that constrain the valid valuation on $\vec{i}$. PC in Equation 1 is the abbreviation of "Parameterized complementary", which means $F_{PC}(p, l, r)$ is used to check whether the encoder's input can be uniquely determined.**

According to Figure 2, it is obvious that the first three lines of Equation (1) are always satisfiable, because they are just two unrolled transition re-

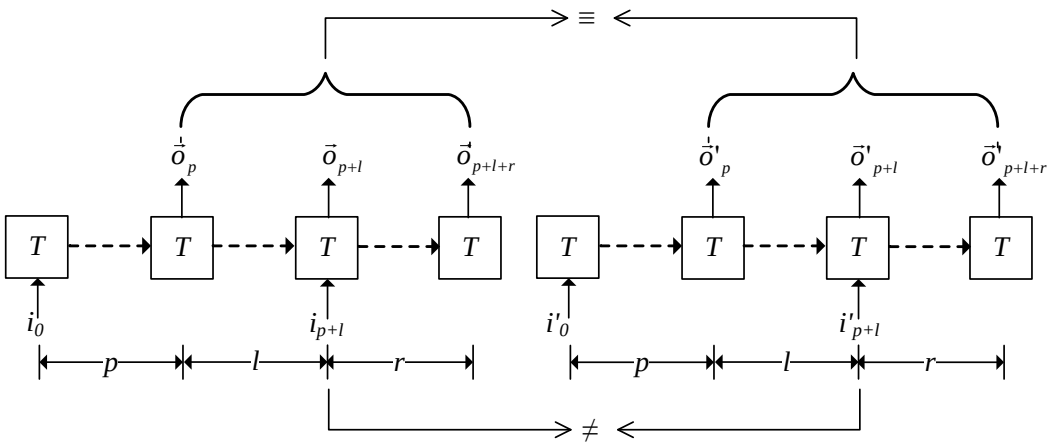


Fig. 2. The sound approach checking if i_{p+l} can be uniquely determined

lation sequence with the same output sequence. And the last two lines are constraints on input variables. We always check their satisfiability before running our algorithm. So the unsatisfiability of $F_{PC}(p,l,r)$ always means $i_{p+l} \equiv i'_{p+l}$.

According to Figure 2, it is obvious that, if $F_{PC}(p,l,r)$ is unsatisfiable, then $F_{PC}(p',l',r')$ is also unsatisfiable with $p' \geq p$, $l' \geq l$ and $r' \geq r$. By studying Equation (1), we can find that the clause set of $F_{PC}(p',l',r')$ is a super set of $F_{PC}(p,l,r)$. This also lead to the same conclusion.

This means, the bounded proof of $F_{PC}(p,l,r)$'s unsatisfiability can be generalized to all cases for larger p, l and r.

PROPOSITION 2.1. *If $F_{PC}(p,l,r)$ is unsatisfiable, then i_{p+l} can be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$ for all larger p, l and r.*

Equation (1) does not include an initial state, instead it use the p steps prefix state transition sequence $< \vec{s_0}, \ldots, \vec{s_p} >$ to propagate the constraints $assertion(\vec{i})$ into the state sequence $s_{\vec{p+1}}, \ldots, s_{\vec{p+l+r}}$, such that some states that can not be reached with $assertion(\vec{i})$ can be eliminated. This leads to two major advantages over considering initial states: First, it simplify and speedup our algorithm by avoiding the need to compute the reachable state set or inductive invariants. Second and more important, it improve the decoder's reliability by preventing any corrupted data from affecting the decoder's state, that is, any corrupted $\vec{o}$ fed to the decoder can only affect the decoder for finite number of steps.

Of course this approach have one drawback that it is a little bit too stronger than necessary. That is, it requires that $\vec{i}$ must be uniquely determined on a larger state set R^p that is reachable in p steps from any states, instead of on the smaller reachable states R. It is obvious that $R \subset R^p$. Tu and Jiang [2013] propose a breakthrough algorithm that overcomes this shortcoming by inferring inductive invariants. Their work is orthogonal to ours. So to simplify our discussion, we will not integrate their work here. At the

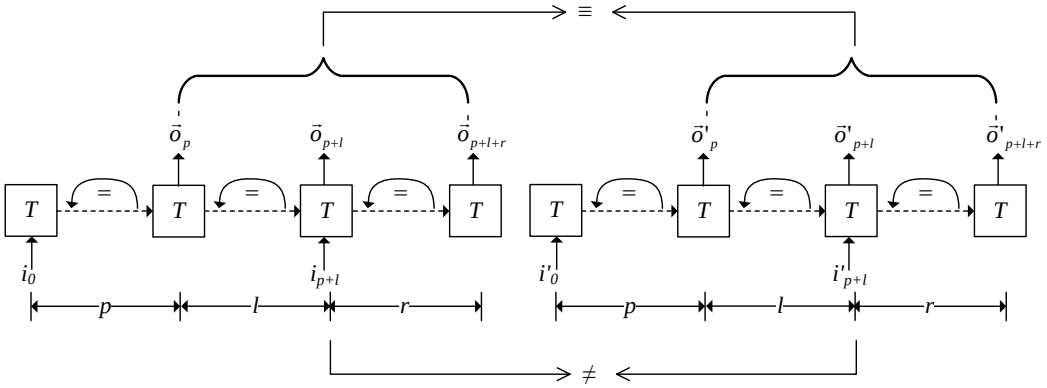


Fig. 3. The complete approach checking if i_{p+l} can NOT be uniquely determined

same time, for all the benchmarks we have tried, our current approach is sufficient.

2.3.2. ***The complete approach****. .*

We have just learned that, if $F_{PC}(p,l,r)$ is unsatisfiable, then i_{p+l} can be uniquely determined for larger p, l and r. **On the other hand**, if $F_{PC}(p,l,r)$ is satisfiable, then i_{p+l} cannot be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$ for this particular valuation of p, l and r. There are two possible cases:

(1) i_{p+l} can be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$ for larger p, l and r;
(2) i_{p+l} can not be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$ for any p, l and r at all.

If it is the first case, then by iteratively increasing the value of p, l and r, $F_{PC}(p,l,r)$ will eventually become unsatisfiable. But if it is the second case, then this iterative algorithm will never terminate.

So, to obtain a halting algorithm, we need to distinguish these two cases. One such solution is shown in Figure 3, which is similar to Figure 2 but with three additional constraints to detect loops on the three state sequences $< \vec{s}_0, \ldots, \vec{s}_p >$,$< \vec{s}_{p+1}, \ldots, \vec{s}_{p+l} >$ and $< \vec{s}_{p+l+1}, \ldots, \vec{s}_{p+l+r} >$. It is formally defined in Equation (2) with the last three lines corresponding to the three constraints used to detect loops.

$$F_{LN}(p,l,r) := \left\{ \begin{array}{ll} & F_{PC}(p,l,r) \\ \wedge & \bigvee_{x=0}^{p-1} \bigvee_{y=x+1}^{p} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \\ \wedge & \bigvee_{x=p+1}^{p+l-1} \bigvee_{y=x+1}^{p+l} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \\ \wedge & \bigvee_{x=p+l+1}^{p+l+r-1} \bigvee_{y=x+1}^{p+l+r} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \end{array} \right\} \quad (2)$$

LN stands for "loop non-complementary", which means $F_{LN}(p,l,r)$ with three loops is used to check whether the input variables can NOT be uniquely determined.

When $F_{LN}(p,l,r)$ is satisfiable, then i_{p+l} cannot be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$. **More importantly, by unrolling these three loops, we can generalize this conclusion to all larger p, l and r:**

PROPOSITION 2.2. *If $F_{LN}(p,l,r)$ is satisfiable, then $i_{p'+l'}$ cannot be uniquely determined by $< \vec{o}_{p'}, \ldots, \vec{o}_{p'+l'+r'} >$ for any larger $p' \geq p$, $l' \geq l$ and $r' \geq r$.*

ALGORITHM 1: $CheckUniqueness(i)$:The halting algorithm to determine whether i can be uniquely determined by a bounded sequence of output variable vector $\vec{o}$

Input: The input variable i.
Output: whether i can be uniquely determined by $\vec{o}$, and the value of p, l and r.

```
1 p:= 1; l:= 1; r:= 1;
2 while 1 do
3 |   p++; l++; r++;
4 |   if F_PC(p,l,r) is unsatisfiable then
5 |   |   return (1,p,l,r);
6 |   else if F_LN(p,l,r) is satisfiable then
7 |   |   return (0,p,l,r);
8 |
```

2.3.3. ***The full algorithm.*** .

With Propositions 2.1 and 2.2, we can generalize the bounded proof to unbounded proof. Thus, we can build the halting Algorithm 1 that determines if there exists p, l and r that enable an input variable i_{p+l} to be uniquely determined by the encoder's output sequence $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$.

On the one hand, if there actually exists such p, l and r, then eventually $F_{PC}(p,l,r)$ will become unsatisfiable in Line 4; on the other hand, if there does not exist such p, l and r, then eventually p, l and r will be larger than the encoder's longest path without loop, which means that there will be three loops in $< \vec{s}_0, \ldots, \vec{s}_p >$,$< \vec{s}_{p+1}, \ldots, \vec{s}_{p+l} >$ and $< \vec{s}_{p+l+1}, \ldots, \vec{s}_{p+l+r} >$. This will make $F_{LN}(p,l,r)$ satisfiable in Line 6. Both cases will lead to this Algorithm's termination.

Although Algorithm 1 is sufficient to determine whether i can be uniquely determined, the values of $< p,d,l >$ found by Algorithm 1 contain some redundancy, which may cause unnecessarily large overheads on the circuit area.

There are two approaches to resolve this problem. The first one is not to increase the valuation of p, l and r simultaneously, but instead increase them one by one with three nested loops. This approach need to call SAT solver for $O(n^3)$ times, with $n = max(p,l,r)$. We have tried this approach in our previous work [Shen et al. 2009; Shen et al. 2010].

The second one is to follow Algorithm 1, and then use Algorithm 2 to minimize p,d and l one by one. This approach need to call SAT solver for $O(n)$ times,

ALGORITHM 2: $RemoveRedundancy(p,d,l)$

```
1  for l' = l → 0 do
2  |   if F_PC(p,l'−1,r) is satisfiable then
3  |   |   break
4  |
5  for r' = r → 0 do
6  |   if F_PC(p,l',r'−1) is satisfiable then
7  |   |   break
8  |
9  for p' = p → 0 do
10 |   if F_PC(p',l',r'−1) is satisfiable then
11 |   |   break
12 |
13 return < p',d',l' >
```

much less than the first approach. But each formula is larger than that of the first approach.

In [Shen et al. 2011], we have found that the second approach is much faster than the first one. This means, the number of calling SAT solver matter more than the formula size. I think this can be explained by the SAT solver's ability in ignoring irrelevant facts.

3. IDENTIFYING FLOW CONTROL VARIABLES

To facilitate the presentation of our algorithm, we partition the input variable vector $\vec{i}$ into two vectors: the flow control vector $\vec{f}$ and the data vector $\vec{d}$.

The flow control variables $\vec{f}$ are used to represent the validness of $\vec{d}$. So, for a properly designed encoder, $\vec{f}$ should always be uniquely determined by a bounded sequence of the encoder's output $\vec{o}$, or else the decoder cannot recognize the validness of $\vec{d}$.

Thus, Algorithm 3 is proposed to identify $\vec{f}$.

At Line 3, it simply applies Algorithm 1 to each input variable $i \in \vec{i}$ of the encoder, to check whether i_{p+l} can be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$. If yes, the values of p,l and r are also computed.

At Line 5, the input variable i that can be uniquely determined will be added to the vector $\vec{f}$. And, at the following three lines, the maximal values of p, l and r are computed.

On the other hand, when $\vec{i}$ is very long, the run time overhead of testing each $i \in \vec{i}$ one by one would also be very large. To speed up this testing procedure, when the result of $CheckUniqueness$ is (0,?,?,?) at Line 3, every $j \in \vec{i}$ that has different values for j_{p+l} and j'_{p+l} in the satisfying assignment of $F_{LN}(p,l,r)$ can also be ruled out at Line 12, because their own $F_{LN}(p,l,r)$ is also satisfiable.

In some particular case, some data variable $d \in \vec{d}$ can be uniquely determined, just like a flow control variable $f \in \vec{f}$. In this case, d may be identified as a flow control variable by Algorithm 3. But this do not harm our over-

ALGORITHM 3: $FindFlowControl(\vec{i})$:Identifying the flow control variables

Input: The input variable vector $\vec{i}$.
Output: $\vec{f} \subset \vec{i}$ is the vector of the encoder's input variables that can be uniquely determined by a bounded sequence of output variable vector $\vec{o}$, and the maximal value of p, l and r .

```
1  f⃗: = <>; p_max:= 0 ; l_max:= 0 ; r_max:= 0 ;
2  foreach i ∈ i⃗ do
3      (uniq,p,l,r):= CheckUniqueness(i);
4      if uniq ≡ 1 then
5          f⃗ := i ∪ f⃗;
6          p_max := max(p_max, p);
7          l_max := max(l_max, l);
8          r_max := max(r_max, r);
9      else
10         Assume A is the satisfying assignment of F_LN(p,l,r) in Line 6 of Algorithm 1;
11         foreach j ∈ i⃗ do
12             if A(j_{p+l}) ≠ A(j'_{p+l}) then i⃗ := i⃗ − j
13 return (f⃗,p_max,l_max,r_max)
```

all framework, because the decoder's Boolean function can still be correctly characterized in Section 5.

After we have got $\vec{f}$ from Algorithm 3, we take $\vec{d} := \vec{i} - \vec{f}$, that is, all input variables that are not flow control variables.

4. INFERRING PREDICATE THAT ENABLES THE ENCODER'S DATA VECTOR TO BE UNIQUELY DETERMINED

In subsection 4.1, we propose an algorithm to characterize a Boolean function that makes a Boolean formula satisfiable. In subsection 4.2, we apply this algorithm to infer $valid(\vec{f})$, the predicate that enable $\vec{d}$ to be uniquely determined by a bounded sequence of $\vec{o}$.

4.1. Characterizing a function that makes a Boolean formula satisfiable

Assume that $R(\vec{a}, \vec{b}, t)$ is a Boolean formula with $R(\vec{a}, \vec{b}, 0) \wedge R(\vec{a}, \vec{b}, 1)$ unsatisfiable. $\vec{a}$ and $\vec{b}$ are respectively called the important and the non-important variable vectors, while t is the target variable.

We need to characterize a Boolean function $FSAT(\vec{a})$, which covers and only covers all the valuations of $\vec{a}$ that can make $R(\vec{a}, \vec{b}, 1)$ satisfiable. It is formally defined below:

$$FSAT(\vec{a}) := \begin{cases} 1 & \exists \vec{b}.R(\vec{a}, \vec{b}, 1) \\ 0 & otherwise \end{cases} \tag{3}$$

Thus, a naive algorithm of computing $FSAT(\vec{a})$ is to enumerate all valuations of $\vec{a}$, and collect all those valuations that make $R(\vec{a}, \vec{b}, 1)$ satisfiable. But the number of valuations to be enumerated is $2^{|\vec{a}|}$, which will prevent this algorithm from terminating within reasonable time for a long $\vec{a}$.

We can speed up this naive algorithm by expanding each valuation of $\vec{a}$ to a larger set with Craig interpolant[McMillan 2003]. Intuitively, assume that $R(\vec{a}, \vec{b}, 1)$ is satisfiable with a satisfying assignment $A : \vec{a} \cup \vec{b} \cup \{t\} \rightarrow \{0, 1\}$, the following new formula can be constructed by cofactoring:

$$R(\vec{a}, A(\vec{b}), 1) \tag{4}$$

ALGORITHM 4: $CharacterizingFormulaSAT(R, \vec{a}, \vec{b}, t)$:Characterizing a Boolean function over $\vec{a}$ that can make $R(\vec{a}, \vec{b}, 1)$ satisfiable

---

Input: The Boolean formula $R(\vec{a}, \vec{b}, t)$, its important variable vector $\vec{a}$, its non-important variable vector $\vec{b}$, and its target variable t.

Output: $FSAT(\vec{a})$ that makes $R(\vec{a}, \vec{b}, 1)$ satisfiable.

```
1 FSAT(a) := 0 ;
2 while R(a, b, 1) ∧ ¬FSAT(a) is satisfiable do
3     assume A : a ∪ b ∪ {t} → {0, 1} is the satisfying assignment ;
4     φ_A(a) := R(a, A(b), 1) ;
5     φ_B(a) := R(a, A(b), 0) ;
6     assume ITP(a) is the Craig interpolant of φ_A with respect to φ_B ;
7     FSAT(a) := ITP(a) ∨ FSAT(a) ;
8 return FSAT(a)
```

Because $R(\vec{a}, A(\vec{b}), 0) \wedge R(\vec{a}, A(\vec{b}), 1)$ is unsatisfiable, the Craig interpolant $ITP(\vec{a})$ of $R(\vec{a}, A(\vec{b}), 1)$ with respect to $R(\vec{a}, A(\vec{b}), 0)$ can be computed and used as an over-approximation of the set of $\vec{a}$ that makes $R(\vec{a}, A(\vec{b}), 1)$ satisfiable. At the same time, $ITP(\vec{a}) \wedge R(\vec{a}, A(\vec{b}), 0)$ is unsatisfiable, so $ITP(\vec{a})$ covers nothing that can make $R(\vec{a}, A(\vec{b}), 0)$ satisfiable. Thus,$ITP(\vec{a})$ covers exactly the set of valuations of $\vec{a}$ that can make $R(\vec{a}, A(\vec{b}), 1)$ satisfiable.

Based on the foregoing discussion, Algorithm 4 is proposed to characterize $FSAT(\vec{a})$. Line 2 checks whether there is still some new valuation of $\vec{a}$ that can make $R(\vec{a}, \vec{b}, 1)$ satisfiable, but has not been covered by $FSAT(\vec{a})$. Lines 4 and 5 assign the value of $\vec{b}$ from the satisfying assignment to $R(\vec{a}, \vec{b}, 1)$ and $R(\vec{a}, \vec{b}, 0)$ respectively, to remove $\vec{b}$ from them.

Thus, $\phi_A \wedge \phi_B$ in Line 6 is unsatisfiable, and the common variables vector of ϕ_A and ϕ_B is $\vec{a}$. So a Craig interpolant $ITP(\vec{a})$ can be generated with the McMillian's algorithm[McMillan 2003].

$ITP(\vec{a})$ is added to $FSAT(\vec{a})$ in Line 7 and ruled out in Line 2.

Each iteration of the while loop in Algorithm 4 adds at least a valuation of $\vec{a}$ to $FSAT(\vec{a})$, which means that $FSAT(\vec{a})$ is a Boolean function that covers a bounded and strictly increasing set of valuations of $\vec{a}$. So Algorithm 4 is a halting one.

4.2. Inferring $valid(\vec{f})$ that enables $\vec{d}$ to be uniquely determined

This subsection introduces the non-trivial details of how to infer the predicate $valid(\vec{f})$. So we first present an intuitive and informal introduction in 4.2.1. And then present its details in 4.2.2 and 4.2.3. Finally, we present the overall algorithm framework in 4.2.4.

*4.2.1. **Intuitive introduction**. .*

In this Section, what we want is the predicate $valid(\vec{f})$ that enables $\vec{d}$ to be uniquely determined, that is, the set of all valuations of $valid(\vec{f}_{p+l})$ that can make $F_{PC}(p, l, r)$ unsatisfiable for some p,l and r.

But what we have is only Algorithm 4 that can find out the set of valuation of $\vec{f}_{p+l}$ that can make $F_{PC}(p, l, r)$ satisfiable. We call the predicate that cover and only cover this set $FSAT_{PC}(p, l, r)$. And we will present how to infer it in 4.2.2.

But as shown in Subsection 2.3, $\vec{d}_{p+l}$ not uniquely determined for some particular p,l and r, may become uniquely determined for larger p,l and r. For example, an encoder with 3 step latency can not uniquely determine its input $\vec{i}$ with p,l and r smaller than 3. But it can with p,l and r larger than 3. That means, a particular valuation of $\vec{f}_{p+l}$ that makes $F_{PC}(p, l, r)$ satisfiable for some p,l and r, may make it unsatisfiable for some larger p,l and r.

So as shown in Figure 4, $\neg FSAT_{PC}(p, l, r)$ is only an under-approximation of $valid(\vec{f})$ which grow monotonically with respect to the valuation of p,l and r. We still need an over-approximation that shrink monotonically to construct a halting algorithm.

Inspired by the Figure 3 and $F_{LN}(p, l, r)$, we can compute this over-approximation by using Algorithm 4 to find out the set of valuation of $\vec{f}_{p+l}$ that can make $F_{LN}(p, l, r)$ satisfiable. We call the predicate that covers and only covers this set $FSAT_{LN}(p, l, r)$. With a satisfiable $F_{LN}(p, l, r)$, by unrolling the three loops in Figure 3, we can prove that $F_{LN}(p, l, r)$ is still satisfiable for larger p,l and r. That means $FSAT_{LN}(p, l, r)$ is a set of valuation of $\vec{f}_{p+l}$ that makes $F_{LN}(p, l, r)$ satisfiable and grows monotonically with

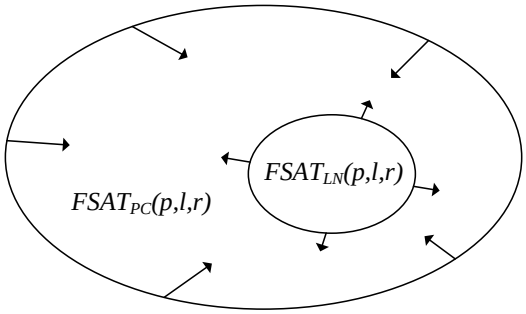


Fig. 4. The monotonicity of $FSAT_{PC}(p,l,r)$ and $FSAT_{LN}(p,l,r)$

respect to p,l and r. So as shown in Figure 4, $\neg FSAT_{LN}(p,l,r)$ is an over-approximation of $valid(\vec{f})$ that shrinks monotonically. We will present how to infer it in 4.2.3.

Together with these two inferred predicates, an iterative algorithm is presented in 4.2.4 to infer $valid(\vec{f})$.

4.2.2. ***Computing*** $FSAT_{PC}(p,l,r)$. .

By replacing i in Equation (1) with $\vec{d}$, we have:

$$F^d_{PC}(p,l,r) := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r}\{(\vec{s}_{m+1},\vec{o}_m) \equiv T(\vec{s}_m,\vec{i}_m)\} \\ \wedge & \bigwedge_{m=0}^{p+l+r}\{(\vec{s'}_{m+1},\vec{o'}_m) \equiv T(\vec{s'}_m,\vec{i'}_m)\} \\ \wedge & \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \\ \wedge & \vec{d}_{p+l} \neq \vec{d'}_{p+l} \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i}_m) \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i'}_m) \end{array} \right\} \tag{5}$$

If $F^d_{PC}(p,l,r)$ is satisfiable, then $\vec{d}_{p+l}$ cannot be uniquely determined by $< \vec{o}_p,\ldots,\vec{o}_{p+l+r} >$. We define a new formula $T_{PC}(p,l,r)$ by collecting the 3rd line of Equation (5):

$$T_{PC}(p,l,r) := \left\{ \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \right\} \tag{6}$$

By substituting $T_{PC}(p,l,r)$ back into $F^d_{PC}(p,l,r)$, we have a new formula:

$$F'_{PC}(p,l,r,t) := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r}\{(\vec{s}_{m+1},\vec{o}_m) \equiv T(\vec{s}_m,\vec{i}_m)\} \\ \wedge & \bigwedge_{m=0}^{p+l+r}\{(\vec{s'}_{m+1},\vec{o'}_m) \equiv T(\vec{s'}_m,\vec{i'}_m)\} \\ \wedge & \vec{d}_{p+l} \neq \vec{d'}_{p+l} \\ \wedge & t \equiv T_{PC}(p,l,r) \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i}_m) \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i'}_m) \end{array} \right\} \tag{7}$$

It is obvious that $\vec{d}$ cannot be uniquely determined for a particular valuation of p, l and r if $F'_{PC}(p,l,r,1)$ is satisfiable. We further define:

$$\vec{a} := \vec{f}_{p+l} \tag{8}$$

$$\vec{b} := \vec{d}_{p+l} \cup \vec{d'}_{p+l} \cup \vec{s}_0 \cup \vec{s'}_0 \cup \bigcup_{0 \le x \le p+l+r, x \ne (p+l)} (\vec{i}_x \cup \vec{i'}_x) \tag{9}$$

$\vec{f}_{p+l}$ can be uniquely determined, so we do not need to consider $\vec{f'}_{p+l}$. Thus, $\vec{a} \cup \vec{b}$ is the vector that contains all the input variable vectors $< \vec{i}_0, \ldots, \vec{i}_{p+l+r} >$ and $< \vec{i'}_0, \ldots, \vec{i'}_{p+l+r} >$ at all steps for the two sequences of unrolled transition function. It also contains the two initial states $\vec{s}_0$ and $\vec{s'}_0$. In addition, T is a function that computes the next state and the output variable vector from the current state and input variable vector. So $\vec{a}$ and $\vec{b}$ can uniquely determine the value of t in $F'_{PC}(p, l, r, t)$. Thus, for a particular combination of p,l and r, the Boolean function over $\vec{f}_{p+l}$ that makes $F'_{PC}(p, l, r, 1)$ satisfiable can be computed by calling Algorithm 4 with $F'_{PC}(p, l, r, t)$, $\vec{a}$ and $\vec{b}$ defined above:

$$FSAT_{PC}(p, l, r) := CharacterizingFormulaSAT(F'_{PC}(p, l, r, t), \vec{a}, \vec{b}, t) \tag{10}$$

Thus, we have the following proposition:

PROPOSITION 4.1. *$FSAT_{PC}(p, l, r)$ is the Boolean function over $\vec{f}_{p+l}$ that makes $\vec{d}_{p+l}$ to be not uniquely determined for a particular p, l and r.*

4.2.3. ***Computing*** $FSAT_{LN}(p, l, r)$. .

Similarly, by replacing i in Equation (2) with $\vec{d}$, we have:

$$F^d_{LN}(p, l, r) := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r} \{(\vec{s}_{m+1}, \vec{o}_m) \equiv T(\vec{s}_m, \vec{i}_m)\} \\ \wedge & \bigwedge_{m=0}^{p+l+r} \{(\vec{s'}_{m+1}, \vec{o'}_m) \equiv T(\vec{s'}_m, \vec{i'}_m)\} \\ \wedge & \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \\ \wedge & \vec{d}_{p+l} \ne \vec{d'}_{p+l} \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i}_m) \\ \wedge & \bigwedge_{m=0}^{p+l+r} assertion(\vec{i'}_m) \\ \wedge & \bigvee_{x=0}^{p-1} \bigvee_{y=x+1}^{p} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \\ \wedge & \bigvee_{x=p+1}^{p+l-1} \bigvee_{y=x+1}^{p+l} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \\ \wedge & \bigvee_{x=p+l+1}^{p+l+r-1} \bigvee_{y=x+1}^{p+l+r} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \end{array} \right\} \tag{11}$$

If $F^d_{LN}(p, l, r)$ is satisfiable, then $\vec{d}_{p+l}$ cannot be uniquely determined by $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$. Furthermore, by unrolling those three loops in the last three lines of Equation (11), we can prove that $\vec{d}$ cannot be uniquely determined for any larger $p' \ge p$,$l' \ge l$ and $r' \ge r$. We further define a new formula $T_{PC}(p, l, r)$ by collecting the 3rd line and the last three lines of Equation (11):

$$T_{LN}(p, l, r) := \left\{ \begin{array}{cc} & \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \\ \wedge & \bigvee_{x=0}^{p-1} \bigvee_{y=x+1}^{p} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \\ \wedge & \bigvee_{x=p+1}^{p+l-1} \bigvee_{y=x+1}^{p+l} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \\ \wedge & \bigvee_{x=p+l+1}^{p+l+r-1} \bigvee_{y=x+1}^{p+l+r} \{\vec{s}_x \equiv \vec{s}_y \wedge \vec{s'}_x \equiv \vec{s'}_y\} \end{array} \right\} \tag{12}$$

By replacing the 3rd line and the last three lines of Equation (11) with $T_{LN}(p, l, r)$, we got:

ALGORITHM 5: $InferringUniqueFormula$:inferring the predicate $valid(\vec{f}_{p+l})$ that enables $\vec{d}_{p+l}$ to be uniquely determined

```
1 p:= p_max; l:= l_max; r:= r_max ;
2 while ¬FSAT_LN(p,l,r) ∧ FSAT_PC(p,l,r) is satisfiable do
3     p ++ ; l ++ ; r ++ ;
4 end
5 return ¬FSAT_LN(p,l,r)
```

$$F'_{LN}(p,l,r,t) := \left\{ \begin{array}{c} \bigwedge_{m=0}^{p+l+r}\{(\vec{s}_{m+1},\vec{o}_m) \equiv T(\vec{s}_m,\vec{i}_m)\} \\ \wedge \ \bigwedge_{m=0}^{p+l+r}\{(\vec{s'}_{m+1},\vec{o'}_m) \equiv T(\vec{s'}_m,\vec{i'}_m)\} \\ \wedge \quad \vec{d}_{p+l} \neq \vec{d'}_{p+l} \\ \wedge \quad t \equiv T_{LN}(p,l,r) \\ \wedge \quad \bigwedge_{m=0}^{p+l+r} assertion(\vec{i}_m) \\ \wedge \quad \bigwedge_{m=0}^{p+l+r} assertion(\vec{i'}_m) \end{array} \right\} \tag{13}$$

Then $\vec{d}$ cannot be uniquely determined for any larger $p' \geq p$,$l' \geq l$ and $r' \geq r$ if $F'_{LN}(p,l,r,1)$ is satisfiable. Thus, for a particular combination of p,l and r, the formula over $\vec{f}_{p+l}$ that makes $F'_{LN}(p,l,r,1)$ satisfiable can be computed by

$$FSAT_{LN}(p,l,r) := CharacterizingFormulaSAT(F'_{LN}(p,l,r,t),\vec{a},\vec{b},t) \tag{14}$$

Thus we have the following proposition:

PROPOSITION 4.2. *$FSAT_{LN}(p,l,r)$ is the formula over $\vec{f}_{p+l}$ that makes $\vec{d}_{p+l}$ to be not uniquely determined for every $p' \geq p$, $l' \geq l$ and $r' \geq r$.*

4.2.4. *The algorithm to compute* $valid(\vec{f})$. .

With Propositions 4.1 and 4.2, the algorithm that infers the predicate $valid(\vec{f}_{p+l})$ is shown in Algorithm 5. It just iteratively increases the value of p, l and r, until $\neg FSAT_{LN}(p,l,r) \wedge FSAT_{PC}(p,l,r)$ is unsatisfiable. The proofs of its termination and correctness are given in the next subsection.

4.3. Proofs of termination and correctness

First we need to prove the following three lemmas:

LEMMA 4.3. $\mathbf{FSAT_{PC}(p,l,r)}$ *in Algorithm 5 monotonically decreases.*

PROOF. For any $p' > p$,$l' > l$ and $r' > l$, assume $A : \vec{f}_{p'+l'} \rightarrow B$ is a Boolean valuation of the flow control vector at $(p'+l')$-step. Further assume that A is covered by $FSAT_{PC}(p',l',r')$.

According to Equation (10) and Algorithm 4, we know that A can make $F'_{PC}(p',l',r',1)$ satisfiable, that is, there exists another satisfying assignment A' of $F'_{PC}(p',l',r',1)$ that has the same value for $\vec{f}_{p+l}$.

Intuitively, as shown in Figure 5, we can map the valuations of the state, input and output vectors in $F'_{PC}(p',l',r',1)$ to that of $F'_{PC}(p,l,r,1)$ by aligning the $(p'+l')$-step to $(p+l)$-step, and discard the two prefix and postfix state transition sequences. Formally, for each $p'+l'-l-p \leq n \leq p'+l'+r$, we map s_n in $F'_{PC}(p',l',r',1)$ to $s_{n-p'-l'+l+p}$ in $F'_{PC}(p,l,r,1)$. i_n and o_n are also mapped similarly.

With this mapping, we can transform the satisfying assignment A' of $F'_{PC}(p',l',r',1)$ to yet another satisfying assignment A'' of $F'_{PC}(p,l,r,1)$.

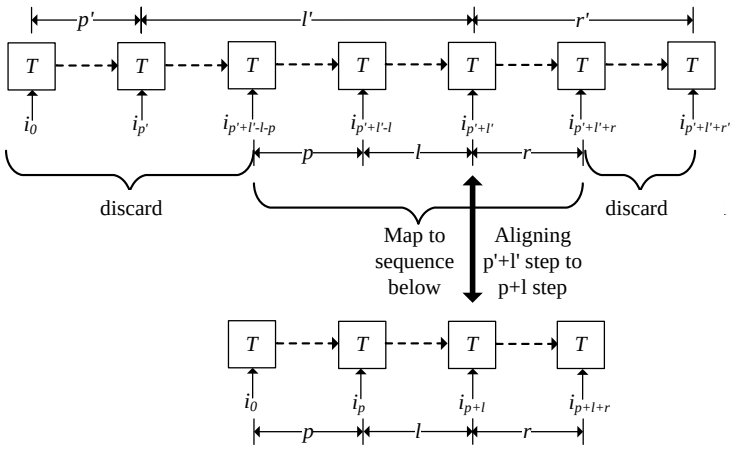


Fig. 5. Mapping $F'_{PC}(p', l', r', 1)$ to $F'_{PC}(p, l, r, 1)$ by aligning

By restricting the domain of A'' to $\vec{f}_{p+l}$, we got the fourth satisfying assignment A'''. According to the mapping presented above, we know that $A''' \equiv A$.

Thus, every A covered by $FSAT_{PC}(p', l', r')$ is also covered by $FSAT_{PC}(p, l, r)$.

Thus, $FSAT_{PC}(p, l, r)$ monotonically decreases. □

LEMMA 4.4. $\mathbf{FSAT_{LN}(p, l, r)}$ *in Algorithm 5 monotonically increases.*

PROOF. According to the definition of $F'_{LN}(p, l, r, t)$ in Equation (13), with any satisfying assignment of $F'_{LN}(p, l, r, 1)$, those three loops in $T_{LN}(p, l, r)$ can be unrolled to got a longer state transition sequence. With an mapping similar to Figure 5, we can prove that $F'_{LN}(p', l', r', 1)$ is satisfiable for all larger p', l' and r'. So, according to Equation (14), we have $FSAT_{LN}(p, l, r) \Rightarrow FSAT_{LN}(p', l', r')$, that is, $FSAT_{LN}(p, l, r)$ monotonically increases. □

LEMMA 4.5. $FSAT_{LN}(p, l, r) \Rightarrow FSAT_{PC}(p, l, r)$

PROOF. It is obvious that $F'_{LN}(p, l, r, 1) \Rightarrow F'_{PC}(p, l, r, 1)$, so $FSAT_{LN}(p, l, r) \Rightarrow FSAT_{PC}(p, l, r)$ holds. □

These three lemmas are depicted intuitively in Figure 4, which makes it obvious that $\neg FSAT_{LN}(p, l, r) \wedge FSAT_{PC}(p, l, r)$ monotonically decreases in Algorithm 5. With these lemmas, let's first prove that Algorithm 5 is a halting one.

THEOREM 4.6. *Algorithm 5 is a halting algorithm.*

PROOF. As the encoder is represented by a finite state machine, the length of the longest path without loop is finite. If Algorithm 5 does not halt, then eventually the values of p, l and r in Algorithm 5 will be larger than the length of the longest path without loop, which means there will be loops in these three state sequences $< \vec{s}_0, \ldots, \vec{s}_p >$,$< \vec{s}_{p+1}, \ldots, \vec{s}_{p+l} >$ and $< \vec{s}_{p+l+1}, \ldots, \vec{s}_{p+l+r} >$. Thus, every satisfying assignment of $F'_{PC}(p, l, r, 1)$ also satisfies $F'_{LN}(p, l, r, 1)$, which means $\neg FSAT_{LN}(p, l, r) \wedge FSAT_{PC}(p, l, r)$ is unsatisfiable. This will lead to the termination of Algorithm 5. So, it is a halting algorithm. □

We will then prove the correctness of Algorithm 5.

THEOREM 4.7. *$\neg FSAT_{LN}(p,l,r)$ returned by Algorithm 5 covers and only covers all valuations of $\vec{f}$ that enable $\vec{d}$ to be uniquely determined by a bounded sequence of $\vec{o}$.*

PROOF. Let's first prove the covering case. $FSAT_{LN}(p,l,r)$ covers a set of valuations of $\vec{f}$ that make $\vec{d}$ to be not uniquely determined for some particular p, l and r. So $\neg FSAT_{LN}(p,l,r)$ rules them out and covers all valuations of $\vec{f}$ that enable $\vec{d}$ to be uniquely determined.

We then prove the only covering case. If $\neg FSAT_{LN}(p,l,r)$ covers a valuation of $\vec{f}$ that makes $\vec{d}$ to be **NOT** uniquely determined for some particular p', l' and r', then $FSAT_{LN}(p',l',r')$ also covers this valuation but $FSAT_{LN}(p,l,r)$ does not. But according to Lemmas 4.3, 4.4 and 4.5, this is impossible, because $FSAT_{LN}(p,l,r)$ is the maximal $FSAT_{LN}(p',l',r')$ for all possible p', l' and r'. So $\neg FSAT_{LN}(p,l,r)$ covers no valuation of $\vec{f}$ that makes $\vec{d}$ to be **NOT** uniquely determined. This proves the only covering case. □

5. CHARACTERIZING THE DECODER'S BOOLEAN FUNCTION

In Section 3, the encoder's input vector $\vec{i}$ has been partitioned into two vectors: the flow control vector $\vec{f}$ and the data vector $\vec{d}$. The algorithms to characterize the decoder's Boolean functions that compute $\vec{f}$ and $\vec{d}$ are different, so they are discussed separately in the following two subsections.

5.1. Minimizing the valuation of l and r

As we have increase the value of p,l and r simultaneously in Algorithm 5, there may be some redundancy in the valuation of p,l and r, which may lead to unnecessary overhead in the decoder's circuit area and delay.

For example, assume the encoder is a simple inverter whose $o_i := i_i$. With $l \equiv 0$ and $r \equiv 0$, we can get the simplest decoder that recover i_i by simply inverting o_i. In such a decoder, there is only one inverted and no registers. But with $l \equiv 1$ and $r \equiv 1$, we need an additional register to delay o_{i-1} for one step, and then recover i_i by inverting the delayed o_{i-1}.

The proposed Algorithm 6 is similar to Algorithm 2. There are two differences between them: First, we add the newly inferred predicate $valid(vecf)$ into the formula whose satisfiability is to be checked, to make sure that the input vector $\vec{i}$ can still be unsatisfiable. Second, we do not minimize the value of p, because it does not affect the decoder's area and delay.

To simply the presentation, we still use p, l and r instead of p', l' and r' in the remainder of this paper.

ALGORITHM 6: $RemoveRedundancy(p,d,l)$

```
1 for l' = l → 0 do
2 |   if F_PC(p, l' − 1, r) ∧ valid(f⃗_{p+l'−1}) is satisfiable then
3 |   |   break
4 |
5 for r' = r → 0 do
6 |   if F_PC(p, l', r' − 1) ∧ valid(f⃗_{p+l'}) is satisfiable then
7 |   |   break
8 |
9 return < d', l' >
```

5.2. Characterizing the decoder's Boolean function that computes $\vec{f}$

Each variable $f \in \vec{f}$ can be uniquely determined by a bounded sequence of the encoder's output. So, for each particular valuation of the encoder's output sequence $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$, f_{p+l} cannot be 0 and 1 at the same time. Thus, the decoder's Boolean function that computes f_{p+l} is exactly the Craig interpolant of ϕ_A with respect to ϕ_B:

$$\phi_A := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r} \{(\vec{s}_{m+1}, \vec{o}_m) \equiv T(\vec{s}_m, \vec{i}_m)\} \\ \wedge & f_{p+l} \equiv 1 \end{array} \right\} \tag{15}$$

$$\phi_B := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r} \{(\vec{s'}_{m+1}, \vec{o'}_m) \equiv T(\vec{s'}_m, \vec{i'}_m)\} \\ \wedge & \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \\ \wedge & f'_{p+l} \equiv 0 \end{array} \right\} \tag{16}$$

It is obvious that $\phi_A \wedge \phi_B$ equals $F_{PC}(p, l, r)$ in Equation (1), so it is unsatisfiable. The common variable set of ϕ_A and ϕ_B is $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$. So, a Craig interpolant ITP can be derived by McMillian's algorithm[McMillan 2003] from the unsatisfiability proof of $\phi_A \wedge \phi_B$, which covers all values of $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$ that make $f_{p+l} \equiv 1$. At the same time, $ITP \wedge \phi_B$ is unsatisfiable, so ITP covers nothing that can make f_{p+l} 0. Thus, ITP is the decoder's Boolean function that computes $f \in \vec{f}$.

5.3. Characterizing the decoder's Boolean function that computes $\vec{d}$

Assume that the predicate over $\vec{f}$ inferred by Algorithm 5, is $valid(\vec{f})$. Let's define the following two formulas for each data variable $d \in \vec{d}$:

$$\phi'_A := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r} \{(\vec{s}_{m+1}, \vec{o}_m) \equiv T(\vec{s}_m, \vec{i}_m)\} \\ \wedge & d_{p+l} \equiv 1 \\ \wedge & valid(\vec{f}_{p+l}) \end{array} \right\} \tag{17}$$

$$\phi'_B := \left\{ \begin{array}{cc} & \bigwedge_{m=0}^{p+l+r} \{(\vec{s'}_{m+1}, \vec{o'}_m) \equiv T(\vec{s'}_m, \vec{i'}_m)\} \\ \wedge & \bigwedge_{m=p}^{p+l+r} \vec{o}_m \equiv \vec{o'}_m \\ \wedge & d'_{p+l} \equiv 0 \\ \wedge & valid(\vec{f'}_{p+l}) \end{array} \right\} \tag{18}$$

Each variable $d \in \vec{d}$ can be uniquely determined by the encoder's output only when $valid(\vec{f})$ holds. So, if $valid(\vec{f}_{p+l})$ holds, for each particular valuation of the encoder's output sequence $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$, d_{p+l} cannot be 0 and 1 at the same time. So, $\phi'_A \wedge \phi'_B$ is unsatisfiable. Thus, a Craig interpolant ITP can be derived by McMillian's algorithm[McMillan 2003] from the unsatisfiability proof of $\phi'_A \wedge \phi'_B$, which covers and only covers all valuations of $< \vec{o}_p, \ldots, \vec{o}_{p+l+r} >$ that make $d_{p+l} \equiv 1$. Thus, ITP is the decoder's Boolean function that computes $d \in \vec{d}$.

Furthermore, when $valid(\vec{f}_{p+l})$ does not hold, the data variable $d \in \vec{d}_{p+l}$ cannot be uniquely determined. So, no function can be used to calculate its value. But this is not a problem, because the decoder is supposed to recognize the invalid data vector by computing the value of control flow vector $\vec{f}$, and ignore the exact value of $\vec{d}$.

6. EXPERIMENTAL RESULTS

We have implemented these algorithms and solved the generated SAT instances with Minisat[Eén and Sörensson 2003]. All experiments have been run on a PC with a 2.4GHz Intel Core 2 Q6600 processor, 8 GB memory, and Ubuntu Linux 12.04.

Table I. The input and output variables of the PCI Express 2.0 encoder

	variable name	width	description
Inputs	$TXDATA$	8	The data to be encoded
	$TXDATAK$	1	1 means $TXDATA$ is a controlling character, 0 means $TXDATA$ is normal data
	$CNTL\_TXEnable\_P0$	1	Indicating the validness of $TXDATA$ and $TXDATAK$
Outputs	HSS_TXD	10	The encoded data
	$HSS\_TXELECIDLE$	1	The electrical idle state

By studying the benchmarks used in our previous papers [Shen et al. 2009;2010; 2011; 2012], we found that most of them have built-in flow control mechanisms. This is not a surprise to us, because these benchmarks all come from real industrial projects. We will present the experimental result for them in the following subsections.

On the other hand, we have also found that the benchmarks used in [Tu and Jiang 2013] contain no flow control mechanism, and hence they will not be discussed here.

6.1. PCI Express 2.0 encoder

This encoder is compliant with the PCI Express 2.0 standard [PCI-SIG 2009]. After deleting empty line and comments, its source code has 259 lines of verilog. After being mapped to LSI10K library, it contains 113 AND2 gates, 212 OR2 gates, 68 inverters and 23 registers. And its total area is 879.

The list of input and output variables is shown in Table I. According to the 8b/10b encoding scheme's coding table[Widmer and Franaszek 1983], when $TXDATAK \equiv 0$, $TXDATA$ can be of any value. But when $TXDATAK \equiv 1$, $TXDATA$ can only be 1C, 3C, 5C, 7C, 9C, BC, DC, FC, F7, FB, FD and FE. So, we write an assertion to rule out those combinations that are not in this coding table. This assertion is embed into the transition function T, so that it can be enforced at every step in the unrolled state sequences.

Algorithm 3 costs 0.924754 seconds to identify the flow control variable $CNTL\_TXEnable\_P0$. And then Algorithm 5 costs 2.067509 seconds to infer the predicate $CNTL\_TXEnable\_P0 \equiv 1$ that enables the data vector to be uniquely determined. Finally, with the inferred predicate, generating the decoder's Boolean functions for $CNTL\_TXEnable\_P0$, $TXDATA$ and $TXDATAK$ costs 3.121821 seconds. After being mapped to LSI10K library, the decoder contains 614 AND2, 198 OR2 and 22 registers. Its total area is 1778.

The major breakthrough of this paper's algorithms is their ability to handle invalid data vector. So, it should be very interesting to show how the invalid data vector is mapped to output variable vector $\vec{o}$. By studying the source code of this encoder, we find that, when and only when $CNTL\_TXEnable\_P0 \equiv 0$ holds, that is, $TXDATA$ and $TXDATAK$ are invalid, the output electrical idle variable $HSS\_TXELECIDLE$ becomes 1. So, the decoder can use the output variable $HSS\_TXELECIDLE$ to uniquely determine the value of flow control variable $CNTL\_TXEnable\_P0$.

6.2. 10G Ethernet encoder

This encoder is compliant with clause 48 of IEEE 802.3 standard [IEEE 2012]. After deleting empty line and comments, this encoder has 214 lines of verilog. After being mapped to LSI10K library, it contains 65 AND2 gates, 192 OR2 gates, 75 inverters and 17 registers. Its total area is 708.

The list of input and output variables is shown in Table II. This encoder also employs an 8b/10b encoding scheme[Widmer and Franaszek 1983] with two inputs: the 8-bit $encode\_data\_in$ to be encoded and 1-bit $konstant$ indicating a controlling character. According to the coding table in [Widmer and Franaszek 1983], when $konstant \equiv 0$,

$encode\_data\_in$ can be of any value. But when $konstant \equiv 1$, $encode\_data\_in$ can only be 1C, 3C, 5C, 7C, 9C, BC, DC, FC, F7, FB, FD and FE. So, we write an assertion to exclude those combinations that are not in this table and embed it into the the transition function T.

Algorithm 3 costs 0.619508 seconds to identify the flow control variable bad_code. And then Algorithm 5 costs 1.443065 seconds to infer the predicate $bad\_code \equiv 0$ that enables the data vector to be uniquely determined. Finally, generating the decoder's Boolean functions for bad_code, $encode\_data\_in$ and $konstant$ costs 2.202401 seconds. After being mapped to LSI10K library, the decoder contains 597 AND2, 174 OR2 and 30 registers. Its total area is 1752.

Although this encoder uses the same coding mechanism as does the PCI Express 2.0 encoder mentioned above, the way it handles the invalid data vector is different. This encoder does not have a separate output variable to indicate the validness of the output data; instead, the validness and exact value of all input variables are both encoded in $encode\_data\_out$. By studying this encoder's source code, we find that when and only when $bad\_code \equiv 1$, that is, $encode\_data\_in$ and $konstant$ are invalid, the output variable $encode\_data\_out$ will become 0010111101. So the decoder can use the output variable $encode\_data\_out$ to uniquely determine the value of the flow control variable bad_code.

6.3. UltraSPARC T2 Ethernet encoder

This encoder comes from the UltraSPARC T2 open source processor designed by Sun Microsystems. It is compliant with clause 36 of IEEE 802.3 standard [IEEE 2012]. After deleting empty line and comments, this encoder's source code has 864 lines of verilog. After being mapped to LSI10K library, it contains 344 AND2 gates, 649 OR2 gates, 128 inverters and 53 registers. Its total area is 2485.

The list of input and output variables is shown in Table III. This encoder also employs an 8b/10b encoding scheme[Widmer and Franaszek 1983], but with yet another style of flow control mechanism that is significantly different from that of the above two encoders. The data to be encoded is the 8-bit txd, but there is no standalone variable to indicate the control symbol. But only a 4-bit $tx\_enc\_ctrl\_sel$ used to define the action to be performed, as shown in Table IV. It is obvious that the functionalities of the control symbol indication and flow control mechanism are combined in $tx\_enc\_ctrl\_sel$. The last four cases in Table IV can never be uniquely determined, because they cannot be distinguished from the case of 'PCS_ENC_DATA. So we write an assertion to rule them out.

Algorithm 3 costs 11.750317 seconds to identify the flow control variables $tx\_enc\_ctrl\_sel$, tx_en and tx_er. And then Algorithm 5 costs 27.456717 seconds to infer the predicate $tx\_enc\_ctrl\_sel \equiv `PCS\_ENC\_DATA$ that enables the data vector to be uniquely determined. Finally, generating the decoder's Boolean functions for txd, $tx\_enc\_ctrl\_sel$, tx_en and tx_er costs 22.156704 seconds. After being mapped to LSI10K library, the decoder contains 2245 AND2, 794 OR2 and 22 registers. Its total area is 6232.

Table II. The input and output variables of the 10G Ethernet encoder

	variable name	width	description
Inputs	$encode\_data\_in$	8	The data to be encoded
	$konstant$	1	1 means $encode\_data\_in$ is a special character, 0 means $encode\_data\_in$ is normal data
	bad_code	1	Indicating the validness of $konstant$ and $encode\_data\_in$
Outputs	$encode\_data\_out$	10	The encoded data

Table III. The input and output variables of the UltraSPARC T2 Ethernet encoder

	variable name	width	description
Inputs	txd	8	The data to be encoded
	$tx\_enc\_ctrl\_sel$	1	Refer to Table IV
	tx_en	1	Transmission enable
	tx_er	1	Transmitting an error character
Outputs	$tx\_10bdata$	10	The encoded data
	$txd\_eq\_crs\_ext$	10	Transmitting an special error character with $tx\_er \equiv 1$ and $txd \equiv 8'h0F$
	tx_er_d	1	Transmitting an error character
	tx_en_d	1	Transmission enable
	$pos\_disp\_tx\_p$	1	Indicating positive parity

As shown in the last column of Table IV, the first 5 cases have their own particular control symbol values assigned to $tx\_10bdata$, so the decoder can recover the value of the flow control variable $tx\_enc\_ctrl\_sel$ from $tx\_10bdata$.

7. RELATED PUBLICATIONS

7.1. Complementary synthesis

The first complementary synthesis algorithm was proposed by [Shen et al. 2009]. It checks the decoder's existence by iteratively increasing the bound of unrolled transition function sequence, and generates the decoder's Boolean function by enumerating all satisfying assignments of the decoder's output. Its major shortcomings are that it may not halt and that it has large runtime overhead in building the decoder.

Shen et al.[2011] and Liu et al.[2011] tackled the halting problem independently by searching for loops in the state sequence, while the runtime overhead problem was addressed in [Shen et al. 2012; Liu et al. 2011] by Craig interpolant[McMillan 2003].

Shen et al.[2012] automatically inferred an assertion for configuration pins, which can lead to the decoder's existence. It can be seen as a special case of Algorithm 5 in Section 4, with the restriction that the inferred assertion must hold on all steps. Our Algorithm 5, on the other hand, is the first algorithm that allows states with and without the inferred assertion to be interleaved freely with each other, which make it possible to handle encoder with flow control mechanism.

Tu and Jiang [2013] proposed a break-through algorithm based on property directed reachability analysis[Bradley 2011; Eén et al. 2011] that can take the encoder's initial state into consideration, so that the infinite history of the encoder and the decoder can be used to generate the decoder's output. This algorithm can handle some special encoders that cannot be handled by the state-of-the-art algorithms. But for the encoders with flow control mechanism used in our experiments, our algorithm is enough, and therefore we have not implemented their algorithm in our framework.

Table IV. Actions to be performed in UltraSPARC T2 Ethernet encoder

The name of action	The meaning of action
'PCS_ENC_K285	sending K28.5 control symbol
'PCS_ENC_SOP	sending K27.7 control symbol
'PCS_ENC_T_CHAR	sending K29.7 control symbol
'PCS_ENC_R_CHAR	sending K23.7 control symbol
'PCS_ENC_H_CHAR	sending K30.7 control symbol
'PCS_ENC_DATA	sending the encoded txd
'PCS_ENC_IDLE2	sending D16.2 data symbol following K28.5
'PCS_ENC_IDLE1	sending D5.6 data symbol
'PCS_ENC_LINK_CONFA	sending D21.5 data symbol following K28.5
'PCS_ENC_LINK_CONFB	sending D2.2 data symbol following K28.5

7.2. Program inversion

According to Gulwani[2010], program inversion involves deriving a program P^{-1} that negates the computation of a given program P. So, the definition of program inversion is very similar to complementary synthesis.

The initial work on deriving program inversion used proof-based approaches[Dijkstra 1979], which could handle only very small programs and very simple syntax structures.

Glück et al. [2005] inverted first-order functional programs by eliminating nondeterminism with LR-based parsing methods. But, the use of functional languages in that work is incompatible with our complementary synthesis.

Srivastava et al. [2011] assumed that an inverse program was typically related to the original program, and so the space of possible inversions can be inferred by automatically mining the original program for expressions, predicates, and control flow. This algorithm inductively rules out invalid paths that cannot fulfill the requirement of inversion to narrow down the space of candidate programs until only the valid ones remain. So, it can only guarantee the existence of a solution, but not the correctness of this solution if its assumptions do not hold.

7.3. Protocol converter synthesis

Protocol converter synthesis is a process that automatically generates a translator between two different communication protocols. This is relevant to our work, because both focus on synthesizing communication circuits.

Avnit et al. [2008; 2009] first defined a general model for describing different protocols, and then provided an algorithm to decide whether there is some functionality of a protocol that cannot be translated into another. Finally, they synthesized a translator by computing the greatest fixed point for the update function of the buffer's control states. Latter, they [2009] improved their algorithm with a more efficient design space exploration algorithm.

7.4. Satisfying Assignments Enumeration

Some algorithms enumerate all satisfying assignments by trying to enlarge the complete satisfying assignments, so that a large state set that contains more complete satisfying assignments can be obtained.

The first approach of this kind is proposed by K. L. McMillan [McMillan 2002]. He constructs an alternative implication graph in SAT solver, which records the reasoning relation that leads to the assignment of a particular object variable. All variables outside this graph can be ruled out from the complete assignment. Kavita Ravi et al.[Ravi and Somenzi 2004] and P. P. Chauhan et al.[Chauhan et al. 2004] remove those variables whose absence can not make $obj \equiv 0$ satisfiable one by one. Shen et al.[Shen et al. 2005] and HoonSang Jin et al.[Jin and Somenzi: 2005; Jin et al. 2005] use an conflict analysis based approach to remove multiple irrelevant variables in one SAT run. Orna Grumberg et al.[Grumberg et al. 2004] divides the variable set into an important subset and an unimportant subset. Variables in the important subset have higher decision priority than those unimportant ones. Thus, the important subset forms a search tree, with each leaf being another search tree for the unimportant set. Cofactoring [Ganai et al. 2004b] qualifies out unimportant variables by setting them to constant value returned by the SAT solver.

Other algorithms tries to construct an Interpolation to cover all satisfying assignments. The first such algorithm was proposed by Jiang et al. [Jie-Hong Roland Jiang 2009]. It construct a first formula with another formula that contradicts with it to get an unsatisfiable formula, from which an interpolation can be derived and used

as an over-approximation of the first formula. Hana et al.[Chockler et al. 2012] generates interpolation with an framework similar to the iterative enumerating and enlarging approaches mentioned above. But there are two enlarging steps, each for the two formulas involving in computing interpolation. This make it the first paper that constructs interpolation without proof.

7.5. Logic synthesis with Craig interpolation

Lee et al.[Lee et al. 2007; Lee et al. 2008] proposed to solving the functional dependency and logic decomposition problems by formulating the base Boolean functions' output bits as the input bits to an unknown Boolean function, and characterize this unknown function by Craig interpolation. This algorithm is also used in our paper [Shen et al. 2012] to find out all the possible decoders.

Wu et al.[Wu et al. 2010] proposed to generate ECO with Craig interpolation.

Jiang et al. [Jie-Hong Roland Jiang 2009] proposed the first algorithm to characterize a Boolean function from a Boolean Relation. It propose two different algorithms: The first one handle a general non-deterministic Boolean relation that can not uniquely determined its output, The second one is a special case of the first one that handles a deterministic relation that can uniquely determine its output by Craig interpolation. The second one is used in [Shen et al. 2012].

This paper also need to handle a non-deterministic Boolean relation, which seems to be similar to that one handled by the first algorithm of [Jie-Hong Roland Jiang 2009]. But our case is much more complicated, because the Boolean relation to be handled is an unrolled transition relation with unknown length. That is, we must first find out the value of p, l and r. But these value must be determine together with finding out the set of flow control variables. So the way we handle non-determinism is significantly different from that of [Jie-Hong Roland Jiang 2009]. But after we got the value of p, l and r, together with the flow control variables $\vec{f}$ and the predicate $valid(\vec{f})$, we can characterize the decoder's Boolean function with an algorithm similar to the second one in [Jie-Hong Roland Jiang 2009].

8. CONCLUSIONS

In this paper, we propose, for the first time, a framework to handle flow control mechanism in complementary synthesis problem. Experimental results indicate that our framework can always successfully handle many complex encoders from real industrial projects, such as PCI Express [PCI-SIG 2009] and Ethernet [IEEE 2012].

ELECTRONIC APPENDIX

The electronic appendix for this article can be accessed in the ACM Digital Library.

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Online Appendix to: Complementary Synthesis for Encoder with Flow Control Mechanism

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