# Curriculum vitae

Name : ShengYu Shen

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Summary :

I am an associated professor of National University of Defense Technology (NUDT) leading a formal method research team that focuses on model checking, theorem proving and static analysis. And I have published lots of papers on top tanked journals and conferences, such as TCAD, TODAES, ICCAD, DATE, ASPDAC, FMCAD, VMCAI and CHARM.

**Education:**

2005  Ph.D.,  Computer Science, National University of Defense Technology(NUDT)

2000  M.S.,   Computer Science, National University of Defense Technology(NUDT)

1997  B.S.,   Computer Science, National University of Defense Technology(NUDT)

**Skills:**

- Formal verification algorithms, including model checking, theorem proving, static analysis, SAT/SMT, BDD and Craig interpolant;
- Formal method tools, including theorem prover Coq, static analyzer Frama-C, SMT solver Z3, SAT solver minisat, computational algebra system GAP and Singular.
- Programming languages including C++, OCaml, TCL and Perl;
- Unix and Linux tools, including awk, m4, sed, vim, make, flex and bison;
- Good English communication skills, both written and verbal;

**Academic Research Experience:**

**2007-2014:**   Developing complementary synthesis algorithm [1-7] that automatically generates decoder from encoders of communication protocols, such as Ethernet and PCI Express. It parses the encoder's source code, iteratively unrolls its transition relation, decides the decoder's existence by iteratively building the monotonically converging over-approximation and under-approximations of the state space, and generates the decoder's Boolean function with Craig interpolant. Please refer to https://github.com/shengyushen/compsyn for these algorithms.

**2001-2006:**   Developing counterexample minimizing algorithms[8-12] used in counterexample-guided abstraction and refinement framework. It backtracks the implication graph of the SAT solver to find out the relevant clauses, which leads to a smaller counterexample.

**1997-2000:**   Developing wave pipelining algorithm that boosting circuit frequency by balancing latency along different paths.

**Academic Publications:**

**Journals:**

1.   ShengYu Shen: **Inferring Assertion for Complementary Synthesis**. IEEE Transactions on CAD of Integrated Circuits and Systems 31(8): 1288-1292 (2012)

2.   ShengYu Shen: **A Halting Algorithm to Determine the Existence of the Decoder**. IEEE Transactions on CAD of Integrated Circuits and Systems 30(10): 1556-1563 (2011)

3.   ShengYu Shen: **Synthesizing Complementary Circuits Automatically**. IEEE Transactions

on CAD of Integrated Circuits and Systems 29(8): 1191-1202 (2010)

4. Ying Qin, ShengYu Shen: **Complementary Synthesis for Encoder with Flow Control Mechanism**. ACM Transactions on Design Automation of Electronic Systems (TODAES) Volume 21 Issue 1, November 2015.Article No. 12

**Conferences:**

5. ShengYu Shen: **Inferring assertion for complementary synthesis**. ICCAD 2011: 404-411

6. ShengYu Shen: **A halting algorithm to determine the existence of decoder**. FMCAD 2010: 91-99

7. ShengYu Shen: **Synthesizing complementary circuits automatically.** ICCAD 2009: 381-388

8. ShengYu Shen: **A fast counterexample minimization approach with refutation analysis and incremental SAT**. ASP-DAC 2005: 451-454

9. ShengYu Shen: **Minimizing Counterexample of ACTL Property**. CHARME 2005: 393-397

10. ShengYu Shen: **A Faster Counterexample Minimization Algorithm Based on Refutation Analysis**. DATE 2005: 672-677

11. ShengYu Shen: **Minimizing Counterexample with Unit Core Extraction and Incremental SAT**. VMCAI 2005: 298-312

12. ShengYu Shen: **Localizing Errors in Counterexample with Iteratively Witness Searching**. ATVA 2004: 456-469

**Honors and Awards:**

1. Distinguished Award of National Science and Technology Progress, for developing TianHe supercomputer, 2014.

2. Distinguished Doctoral Thesis at NUDT, 2007.

**Research Grants:**

1. Automatically Complementary Synthesis for Communication Application (Sponsored by Chinese NSF, 2011-2013)

2. Fixing Program with Counterexample Minimization(Sponsored by Chinese NSF, 2007-2009)

**Seeking Jobs:**

1. Research staff or lead engineer developing formal method tools.

**Frequently asked questions:**

Q: All my previous efforts were focused on hardware verification, can I work effectively on developing software verification tools?

A: Yes I can. The only major difference between software and hardware verification is in their front-end representation, while their background concept, flow and algorithm are similar. And I am pretty familiar with such algorithms, including counterexample-guided abstraction and refinement, property directed reachability and so on.

Q: It seems I have only worked in academic community, can I work effectively in a leading edge industrial project?

A:   Yes I can. Nowadays academic research can't be done with only pencil and paper, it require me to develop and integrate many algorithms and tools, to resolve a totally new problem. So it means lots of coding work. Please refer to https://github.com/shengyushen/compsyn for my works on complementary synthesis algorithm.

Q:   It seems I am a scientist, can I lead a team?
A:   Yes I can. Actually I have led such a team in the last 10 years in the two NSF grants. This team include about 5 members, some of them are associated professors or lecturers, while others are PhD and master candidates.