

17-1-17

C50 tutorial - 2

- 6 + 3 in : 11100

1's comp: 1001

$$\begin{array}{r} + 0011 \\ \hline 1100 \end{array}$$

$$\Rightarrow -(3)$$

2's comp: 1010

$$\begin{array}{r} + 0011 \\ \hline 1101 \end{array}$$

$$\Rightarrow -(0011)$$

$$= -3$$

1. Sign

Extension

2. Left shift / Right shift

3. Native / Cross comp

4. Source + source

5. Simulation, Emulation

6. ARM S, MIPS .

7. Objdump

8. Codes.

Sign Extension

32 bits.

int x = -1

1	1	1	1	1	1	1	1
---	---	---	---	---	---	---	---

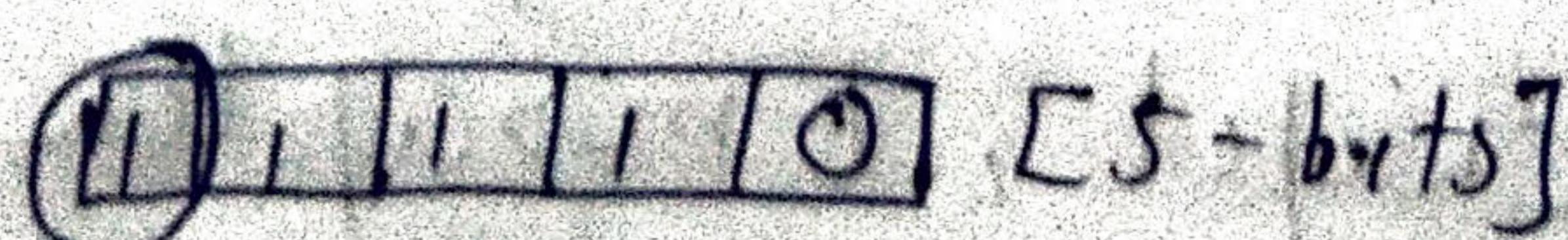
long long y = x. What will be y?

This topic answers the above question.

smaller eg :

Unsigned representation: Add 0's to all the significant bits.

Signed rep: just put the sign bit to all the significant bits.



We added
'1' in the end

Shifts

Left shift: Add 0's in the end.

Right Shift

Logical

Put 0's to the left.

→ Unsigned

Arithmetic

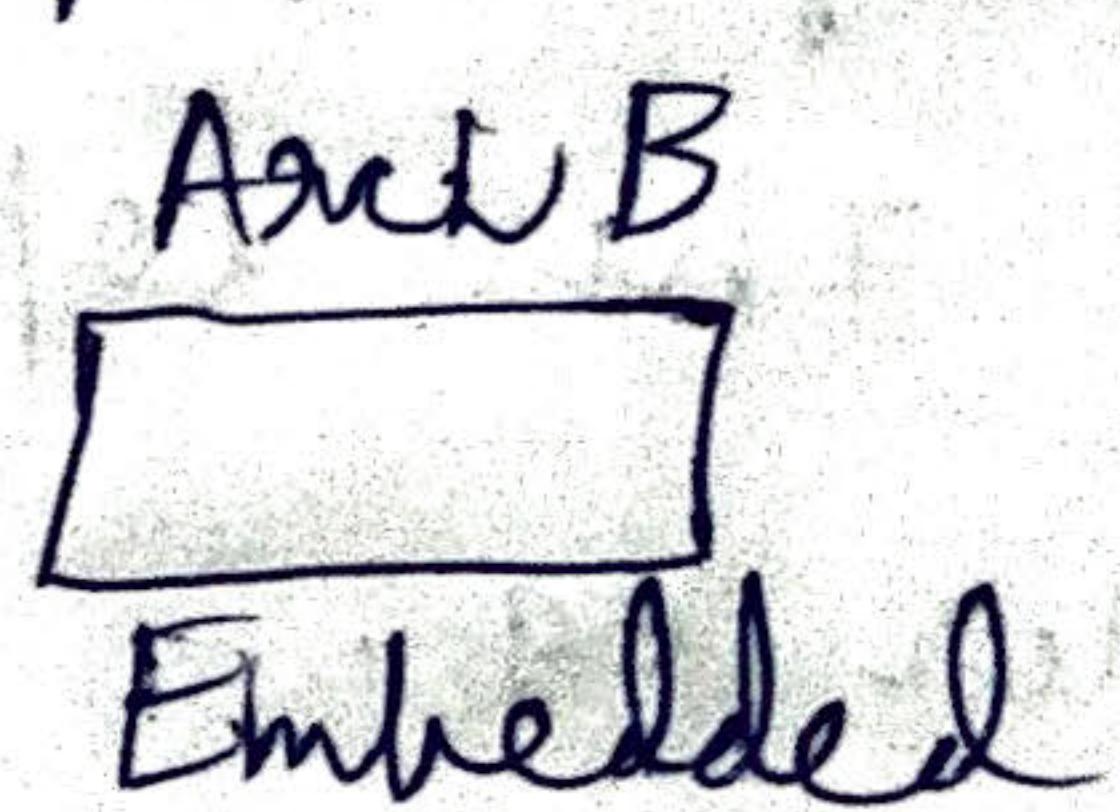
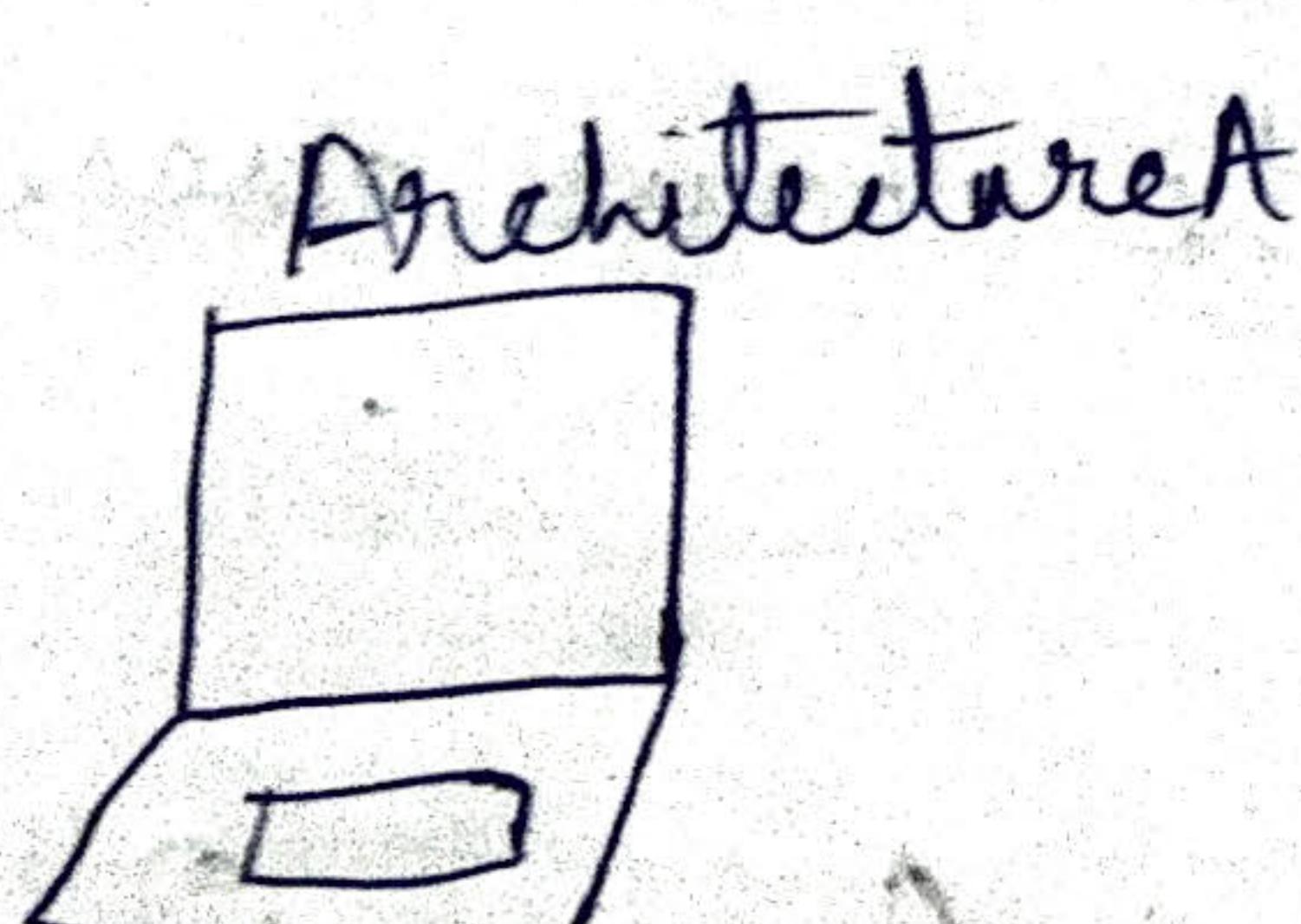
Copy the sign bit.

→ signed.

Embedded system: Less memory, limited processing power
↳ Not enough memory for editors, etc.

How do we build applications on these systems?

We use our laptops and a cross compiler.



Compiler used for running prog.

on same computer: Native compiler

coffee script, chisel, Emscripten: Source to Source compiler.

One Lang to Other

For compiling in other machine: Cross compiler

simulation, Emulator

↓
Simulates

→ Actual implementation
of hardware is done
things: Output is same.
Implementation is not ^{in an} actual ~~way~~
proper way.

Qemu: Emulator.

Virtual Machine: Emulation

ARM, MIPS: 2 different architectures.

Their Instruction set is diff for both
the architectures.

Generally we have x86-64 architectures.

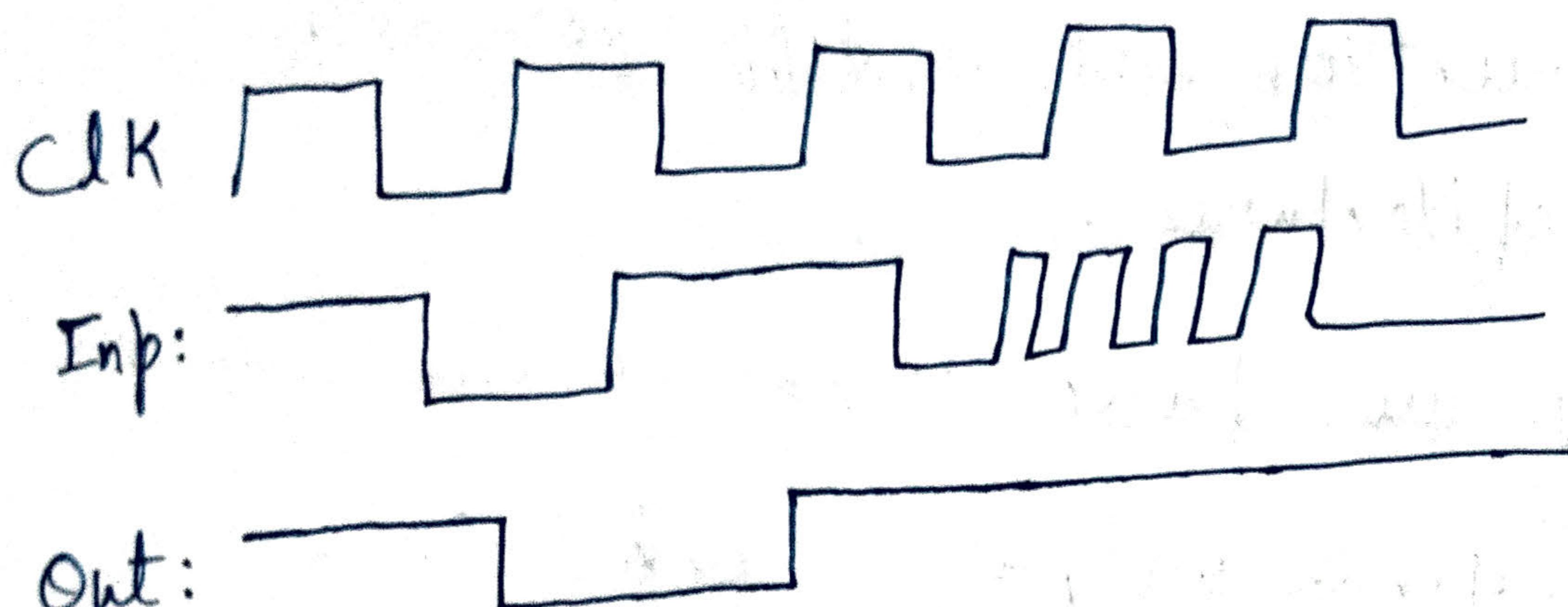
∴ #x gives output in Oct form.

0x fff → 00000 f f f

Quiz:

1. Codes
 2. Signed - Unsigned
 3. Timing diagrams
1. Read handout.
 2. Notes

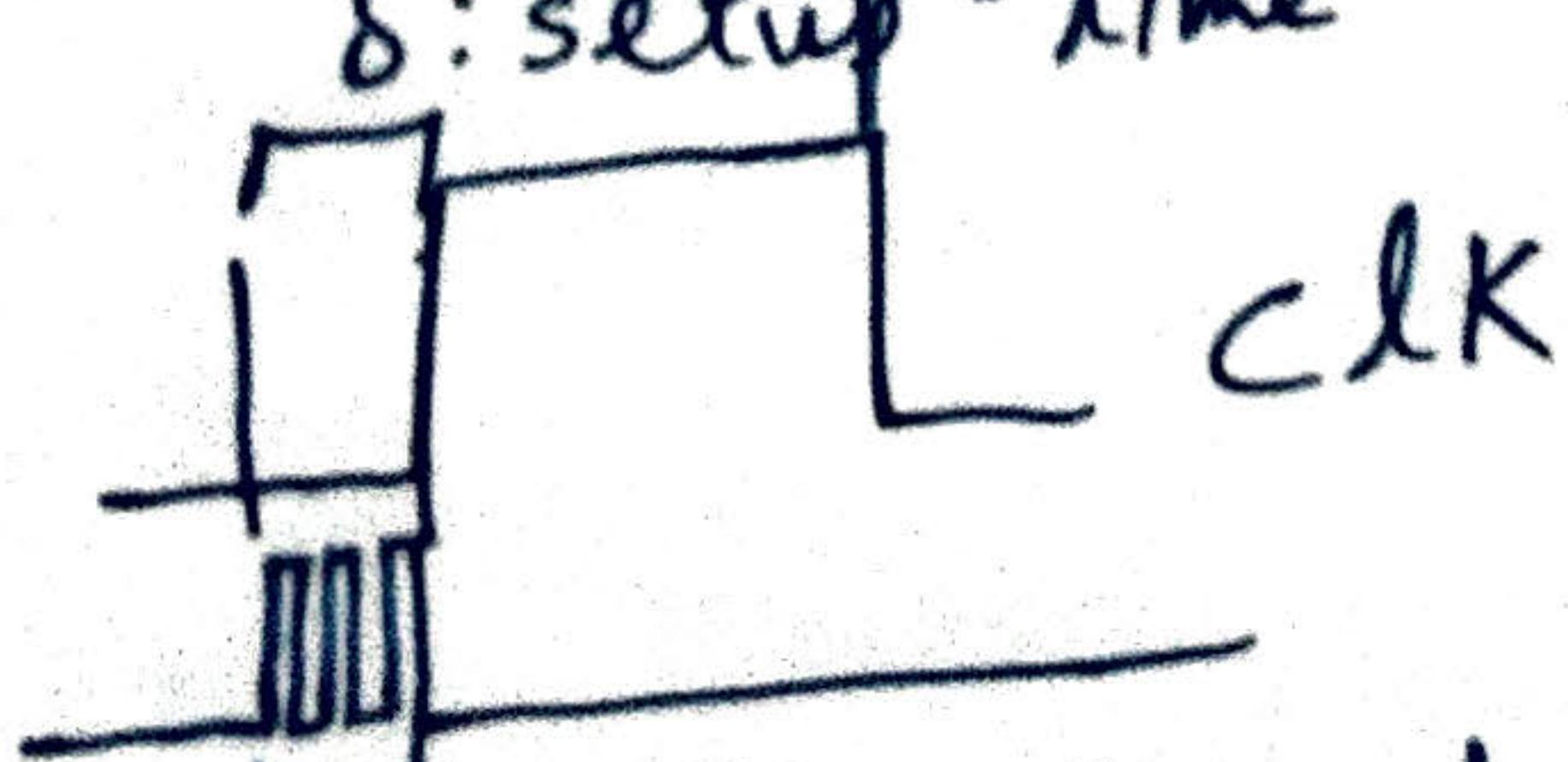
D-Flip flop [$y = Q(t)$]



In reality, the values don't change automatically:

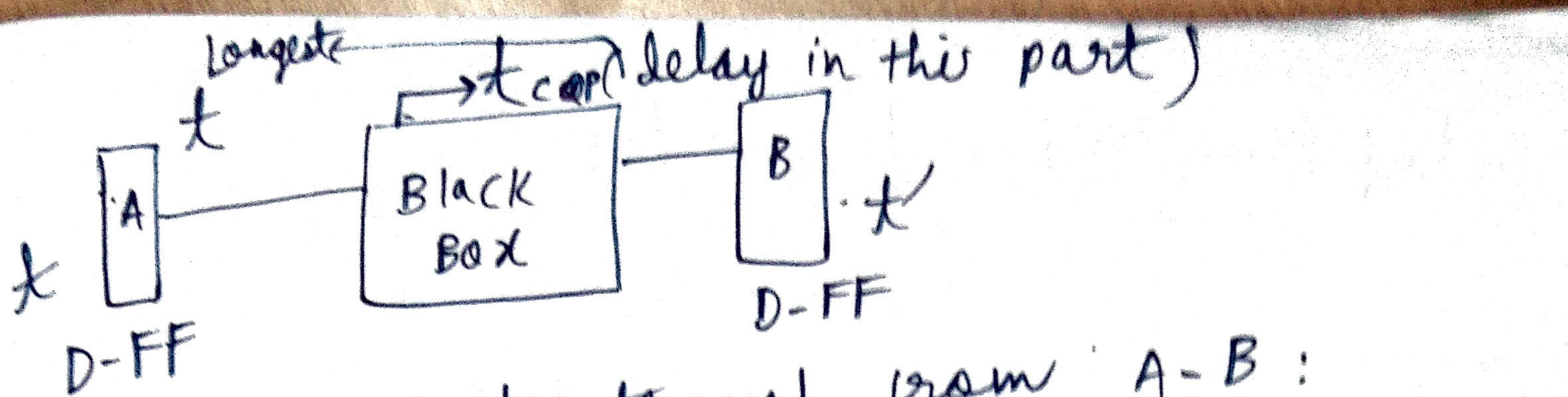
1. Setup-time:

We don't want the input signal to change δ before the rising edge.



2. Hold -Time: $t + \delta'$ (Input should be stable for δ' time after the rising edge).

3. Clock to Q time: time taken for the output to appear on the output line.



time taken to travel from A-B :

critical : ^{v path between}
Longest in the black box

[Decididing time].

$$t + t_{C2Q_i} + t_{CP} \leq t - t_{SP}$$

$\rightarrow t + \delta$ ^{Time}
^{pd}
^{of CLK}

If this is violated, setup time

$$\text{violati} \Rightarrow \delta \geq t_{C2Q} + t_{CP} + t_{SP}$$

Hold time constraint:

~~$t + t_{C2Q_i} + t_{CP} \geq t_h + t$~~

Setup time constraint can't be violated
in same clock cycle.

Hold time should be considered in the
same clock cycle.

$$t + t_{C2Q} + t_{CL} \geq t + t_{HT}$$

$$\Rightarrow t_{C2Q} + t_{CL} \geq t_{HT}$$

Clock Skew

A: t It will reach B at $t + \gamma$.

if $\gamma > t_{HT}$, hold time constraint
need not be considered.

$$\text{on Setup time: } t + t_{C2Q} + t_{CP} \leq t + \gamma - t_{SP}$$

$$\gamma \geq t_{C2Q} + t_{CP} + t_{SP}.$$

Eg: (a) $t_{C2Q} : 100\text{ms}$

$t_{ht} : 150\text{ms}$

$t_{st} : 50\text{ms}$

Current $s = 100\text{ms}$

B·B02:

$$t_{CP} = 45$$

AND 10

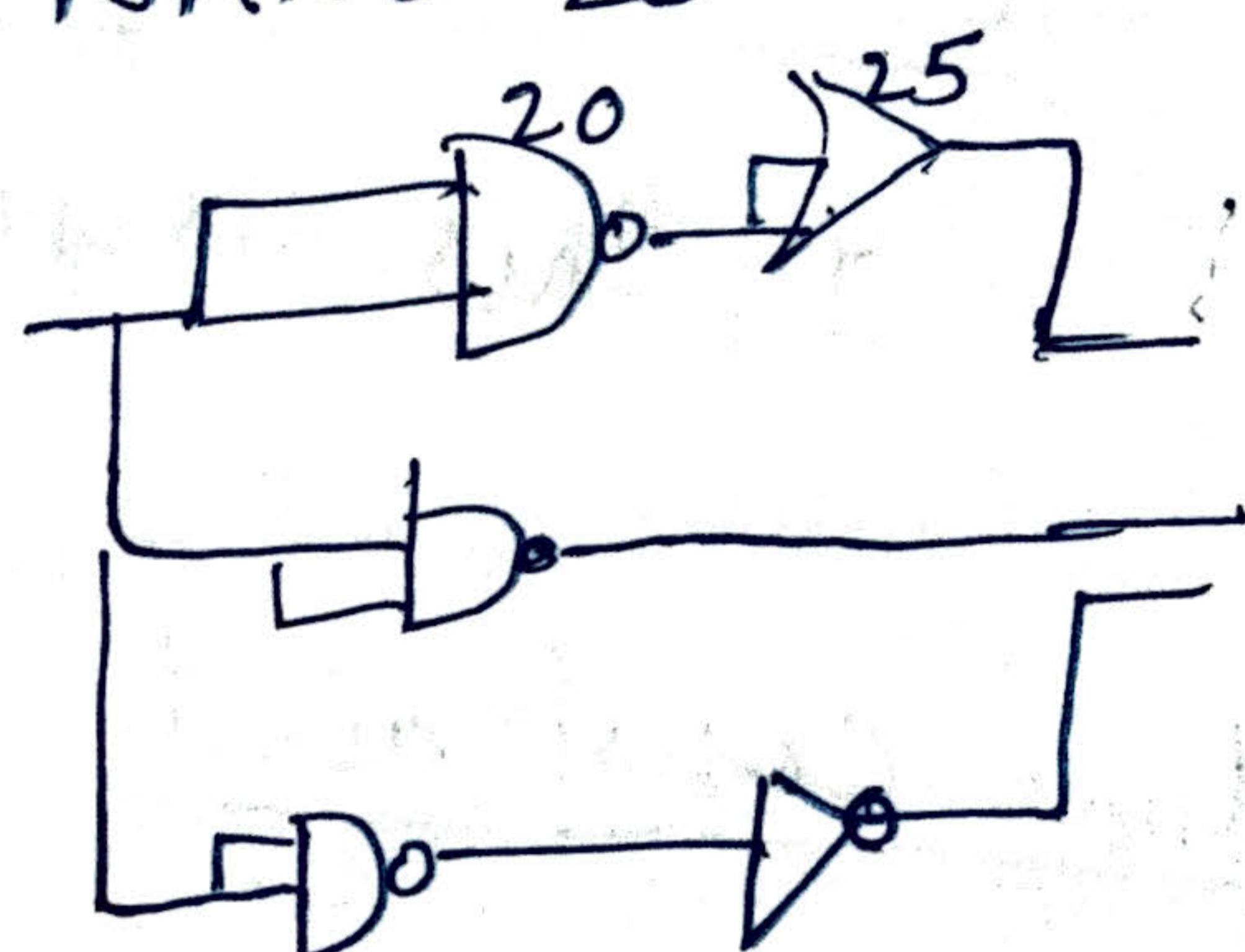
NOT 10

NOR 5

~~NOR~~ 25

NAND 20

Net given:
5ms



(I) constraints: $t_{st} = 50$

Timeprd

$$t_{CP} = 45$$

~~$$(t + 100 + 45) \leq (\gamma + s) - \frac{50}{2}$$~~

$$s \geq 195\text{ ms}$$

(II) constraints: ~~t_{st}~~

$$t + 100 + 45 \geq 150 + t$$

t_{ht} violated.

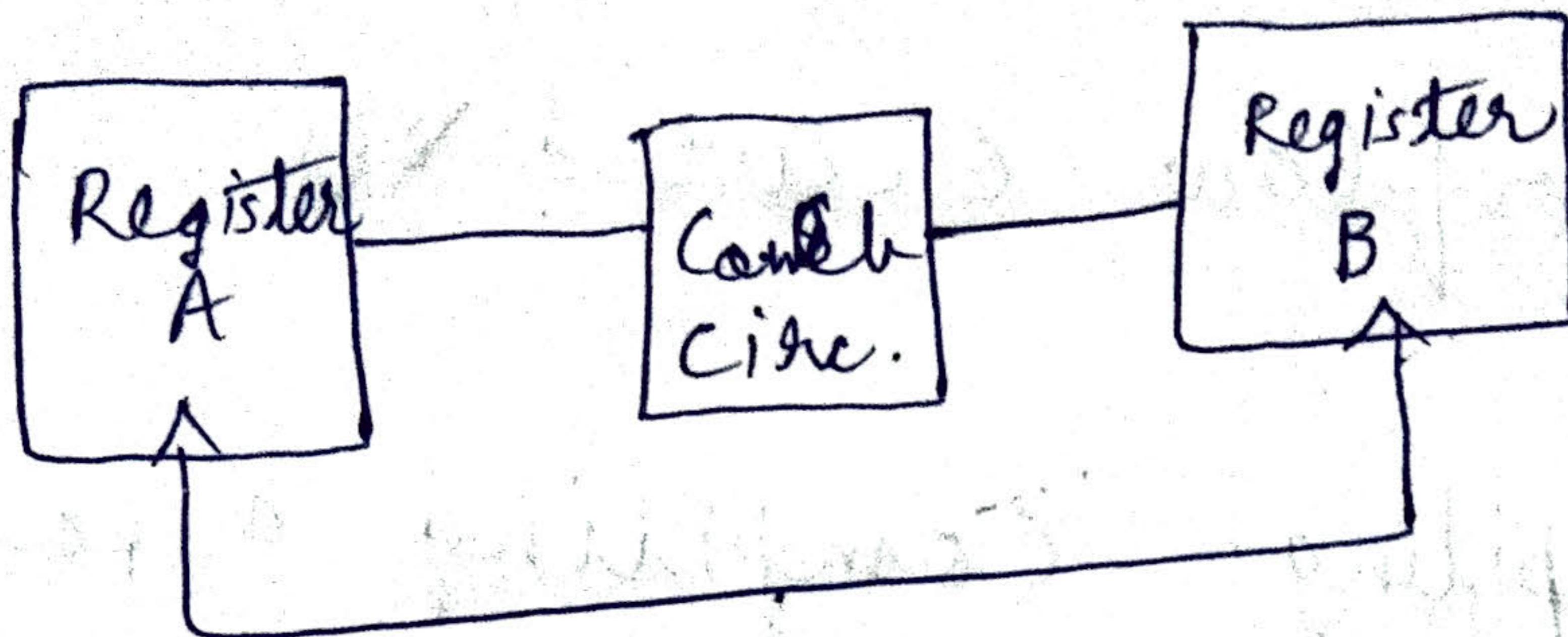
$$t + 100 + 45 \leq t + 100 - 50$$

t_{st} violated.

Tutorial - 4

1. Setup time : largest path
2. hold time : Shortest path.

Clock Skew



The falling edge doesn't occur at the same time for both the registers. The diff. in occurrence of rising edges/falling edges: $t_{\text{clock skew}}$

$$\text{setup } t + t_{C2Q} + t_{\substack{\text{delay} \\ \text{longest}}} \leq t + \gamma - t_{\text{setup}}$$

Clock Skew

$$\text{hold } t_{C2Q} + t + t_{\substack{\text{shortest} \\ \text{path}}} \geq t + \gamma + t_{\text{Ht}}$$

$$\Rightarrow t_{C2Q} + t_{\text{sp}} \leq t_{\text{Ht}} + \gamma. \text{ (Violation)}$$

if there is no γ ; $t_{\text{Ht}} \geq t_{C2Q} + t_{\text{sp}}$
which has to be true.
so γ doesn't affect ^{the} _{in the same} circ.

clock cycle.

Quiz

2(I) 1.

$$\begin{array}{r}
 \text{Ox } \overset{1}{\cancel{F}} \ F \ F \ F \ F \ F \ F \\
 \text{Ox } \cancel{F} \ F \ F \ F \ F \ F \ F \\
 \hline
 \text{Ox } \overset{1}{\cancel{F}} \ F \ F \ F \ F \ F \ E
 \end{array}$$

Ans: Unsigned overflow occurred ~~so~~

2(I)(a) Native compiling: Compiling a code in a machine with arch A for the same architecture A. [Compiling for the same machine].

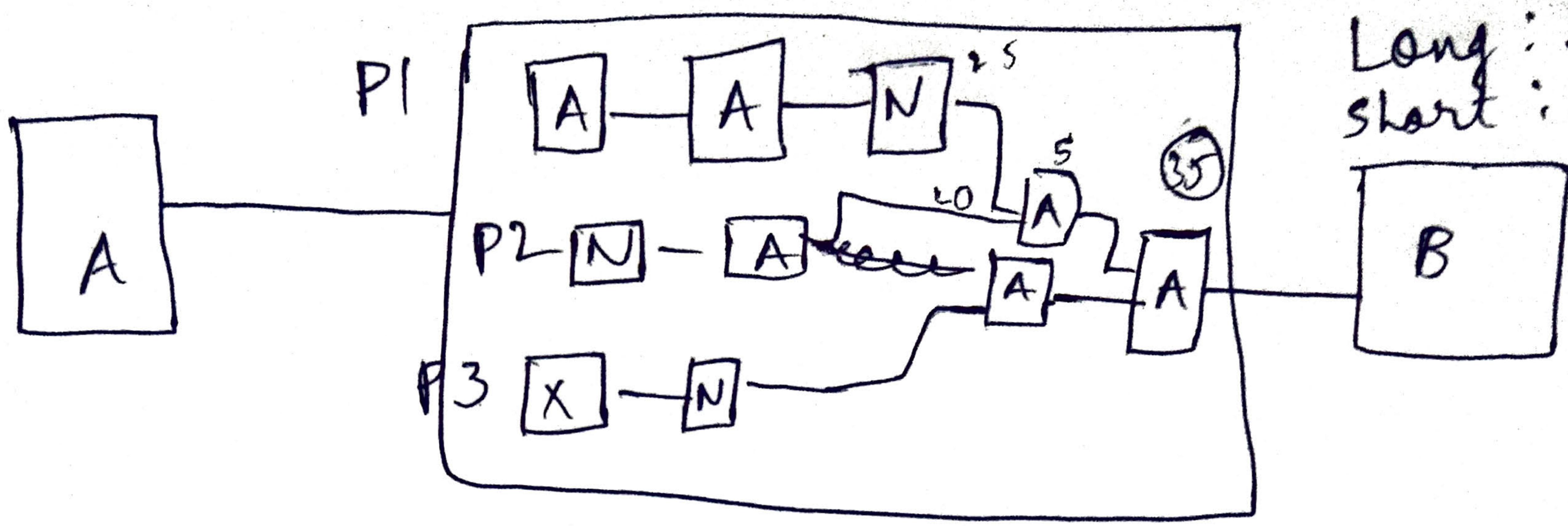
(b) Cross Compiling: Compiling a code in machine with an archit A for executing it in another ~~so~~ machine with a different architecture.

III). Arith. Right Shift: • For Unsigned: Put 0's to most significant bits for each shift.

• Signed: copy the signed bit.

Logical Right Shift: Put 0 in the MSB. irrespective of whether it is signed or unsigned.

3.

Long : 35
Short : 30

$$\begin{array}{l|l|l}
 X \rightarrow 10 \text{ ms} & t_{C2Q} : 1 \text{ ms} & \text{Skew:} \\
 A \rightarrow 5 \text{ ms} & t_{Ht} : 2 \text{ ms} & 5 \text{ ms.} \\
 N \rightarrow 15 \text{ ms} & t_{Setup} : 4 \text{ ms.} & \\
 & \text{Buffer} : 5 \text{ ms} &
 \end{array}$$

(a) No clock skew:

Setup: $t + t_{delay} + t_{C2Q} \leq t + \delta - t_{Setup}$

$$35 + 1 \leq \delta - 4$$

$$\delta \geq 40 \text{ ms.}$$

Hold: $t + t_{delay}^{short} + t_{C2Q} \geq t + t_w$

$$30 + 1 \geq 2$$

$$31 \geq 2$$

No need of buffer.

(b). Setup: $t + t_{delay} + t_{C2Q} \leq t + \delta - t_{Setup}$