ASIC Image Processing SoC

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Design Overview

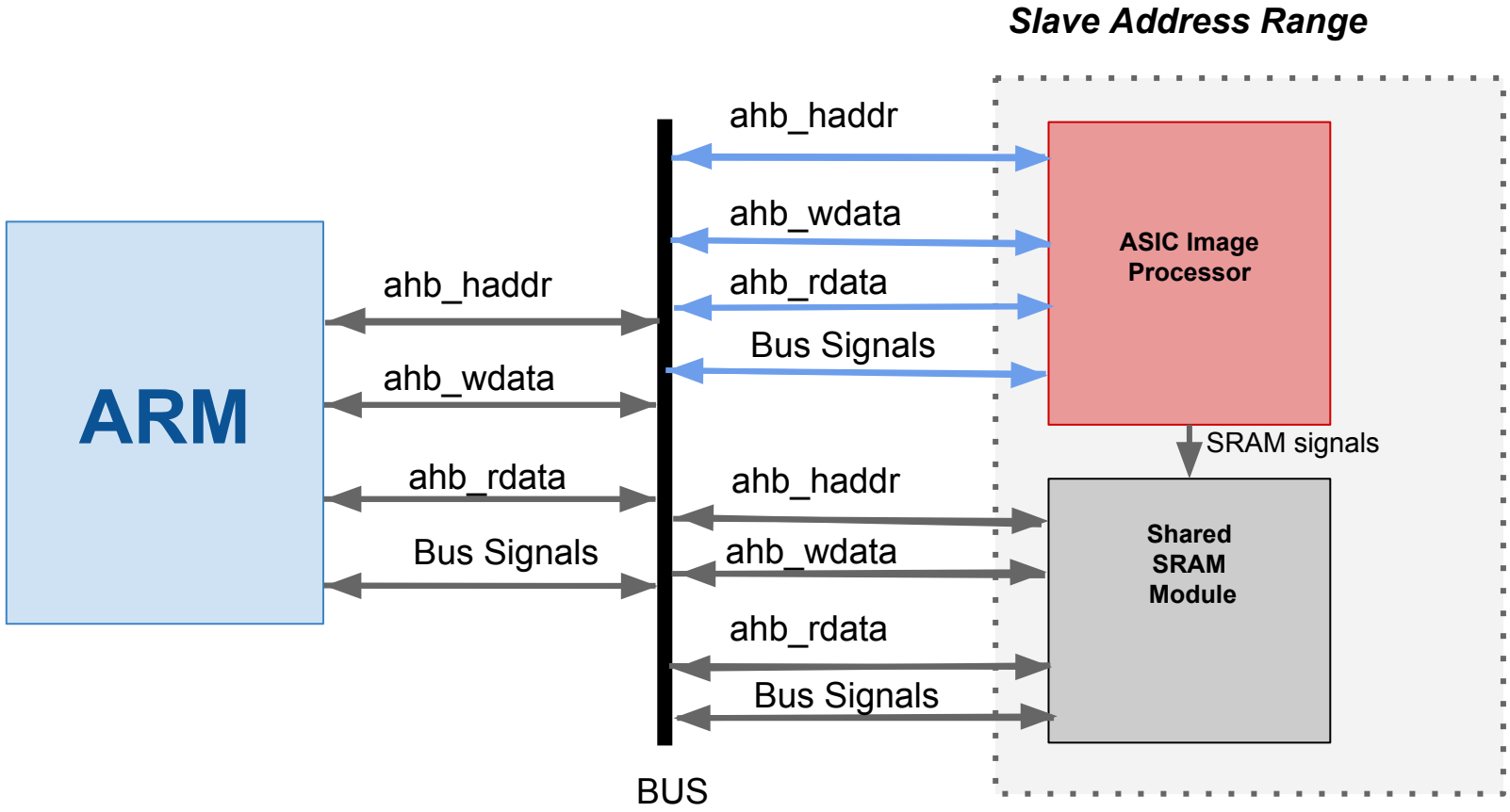
We are designing an image processing unit that implements **Canny Edge Detection** and **Gaussian Blur** filter. The circuit is designed as an auxiliary unit as a part of ARM system-on-chip.

Design Features:

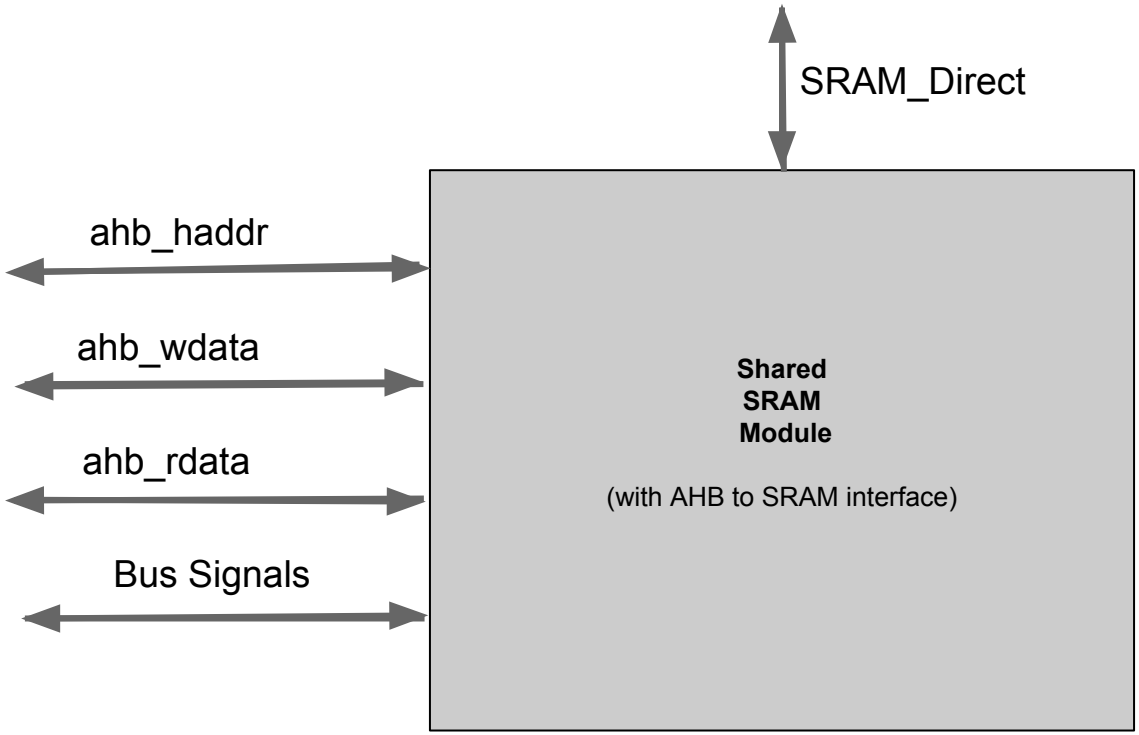
- It detects the edge and extracts the features of an image
- It can be used to interface over AHB bus on a system powered by ARM-based microprocessor
- It provides a “real-time” processing capability.
- Correctly communicate with slave SRAM device over AHB Bus.

System Overview

- AHB Bus
- On/Off Chip SRAM
- Pipelined System


Slave Address Range
ARM
ahb_haddr
ahb_wdata
ahb_rdata
Bus Signals
ahb_haddr
ahb_wdata
ahb_rdata
Bus Signals
BUS
ahb_haddr
ahb_wdata
ahb_rdata
Bus Signals
ASIC Image Processor
SRAM signals
Shared SRAM Module

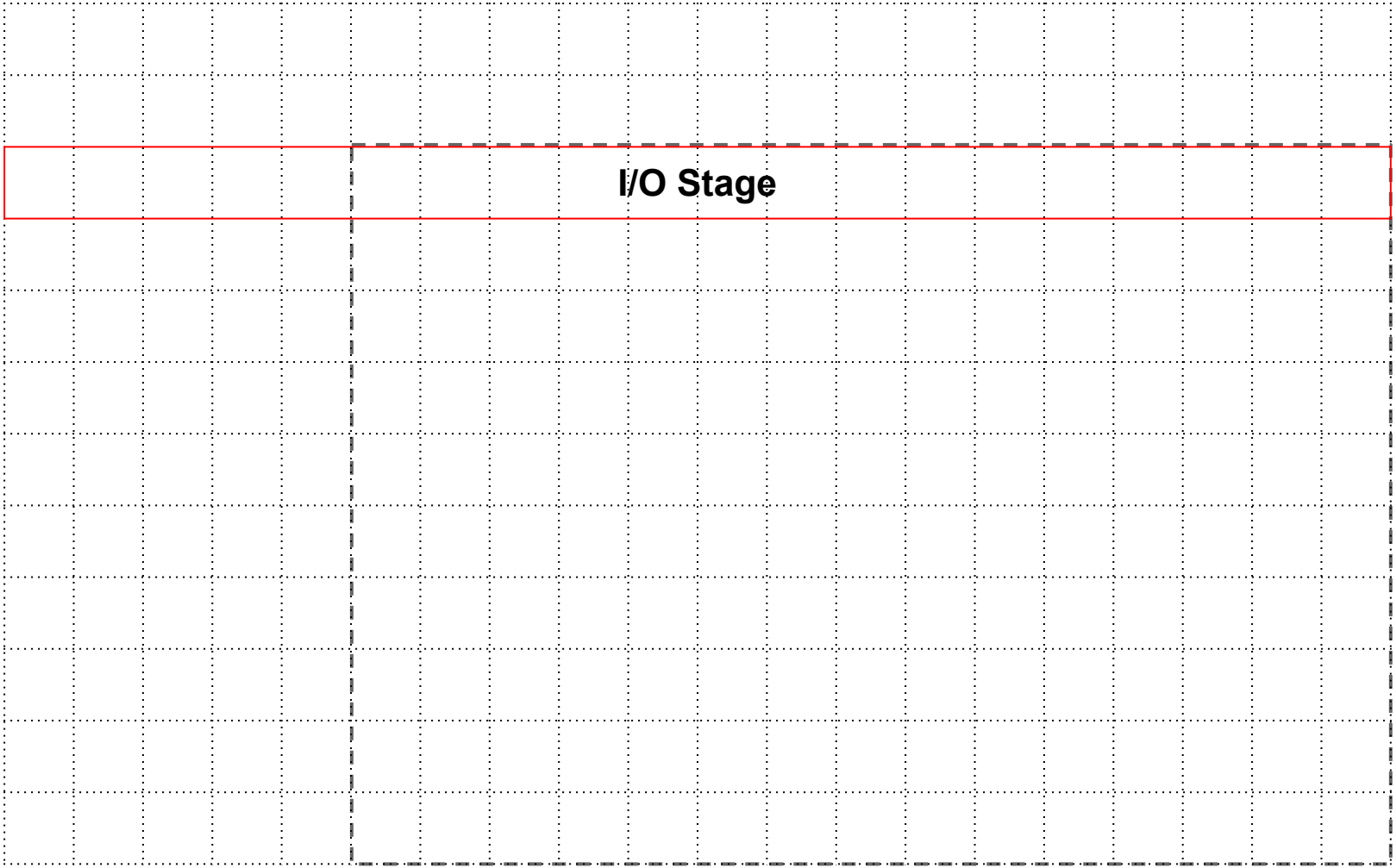
SRAM Duality

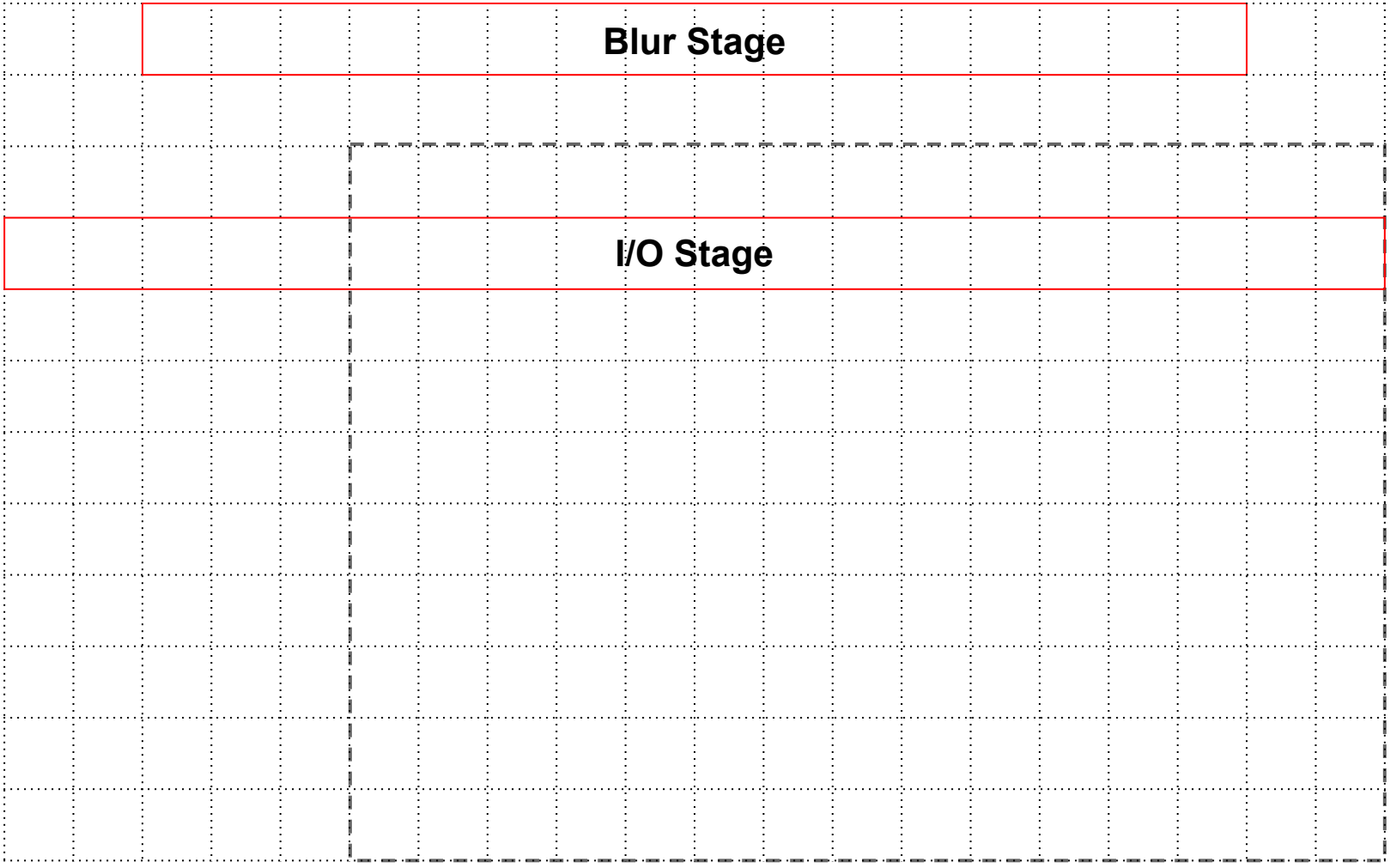


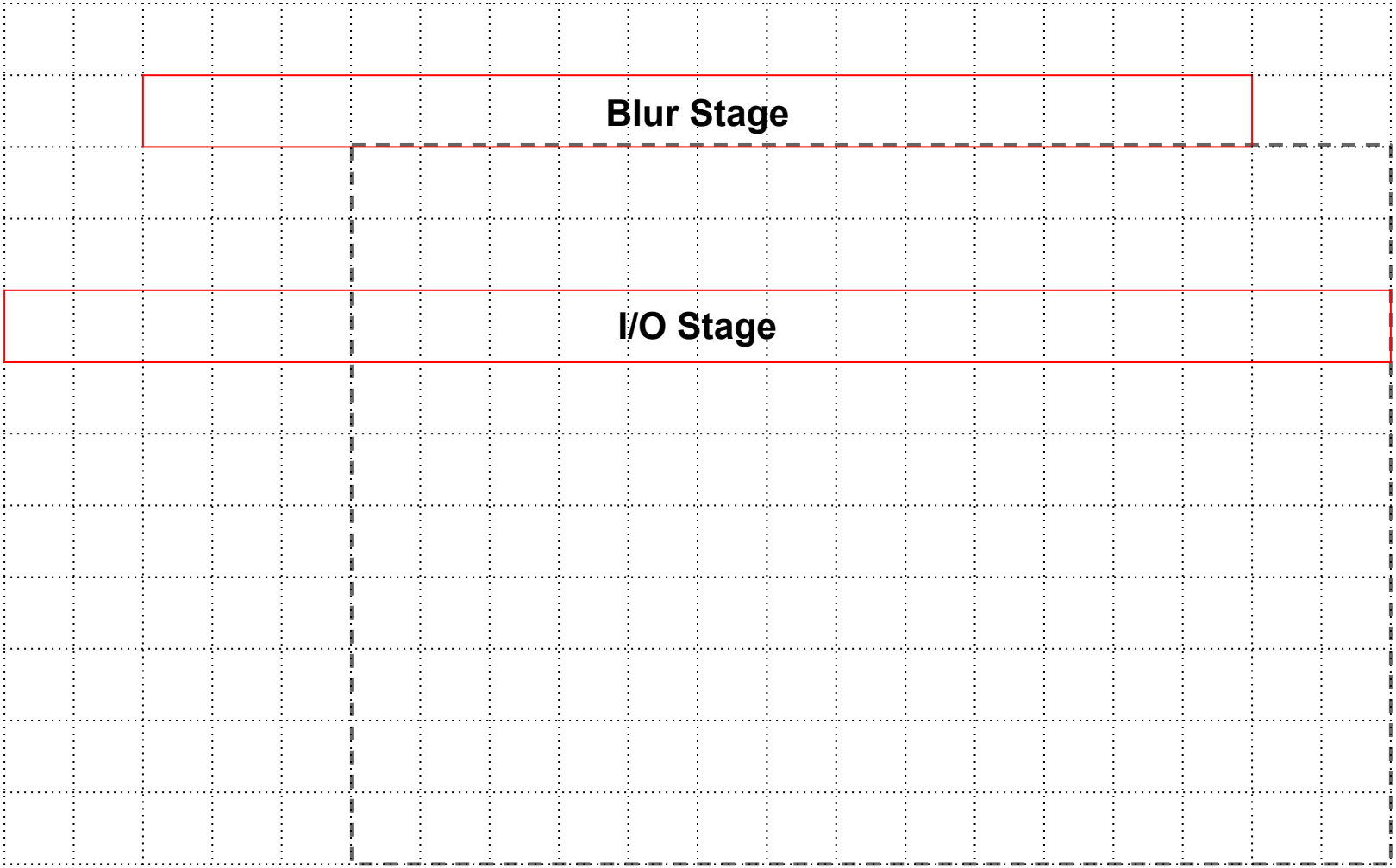
Pipelined Architecture

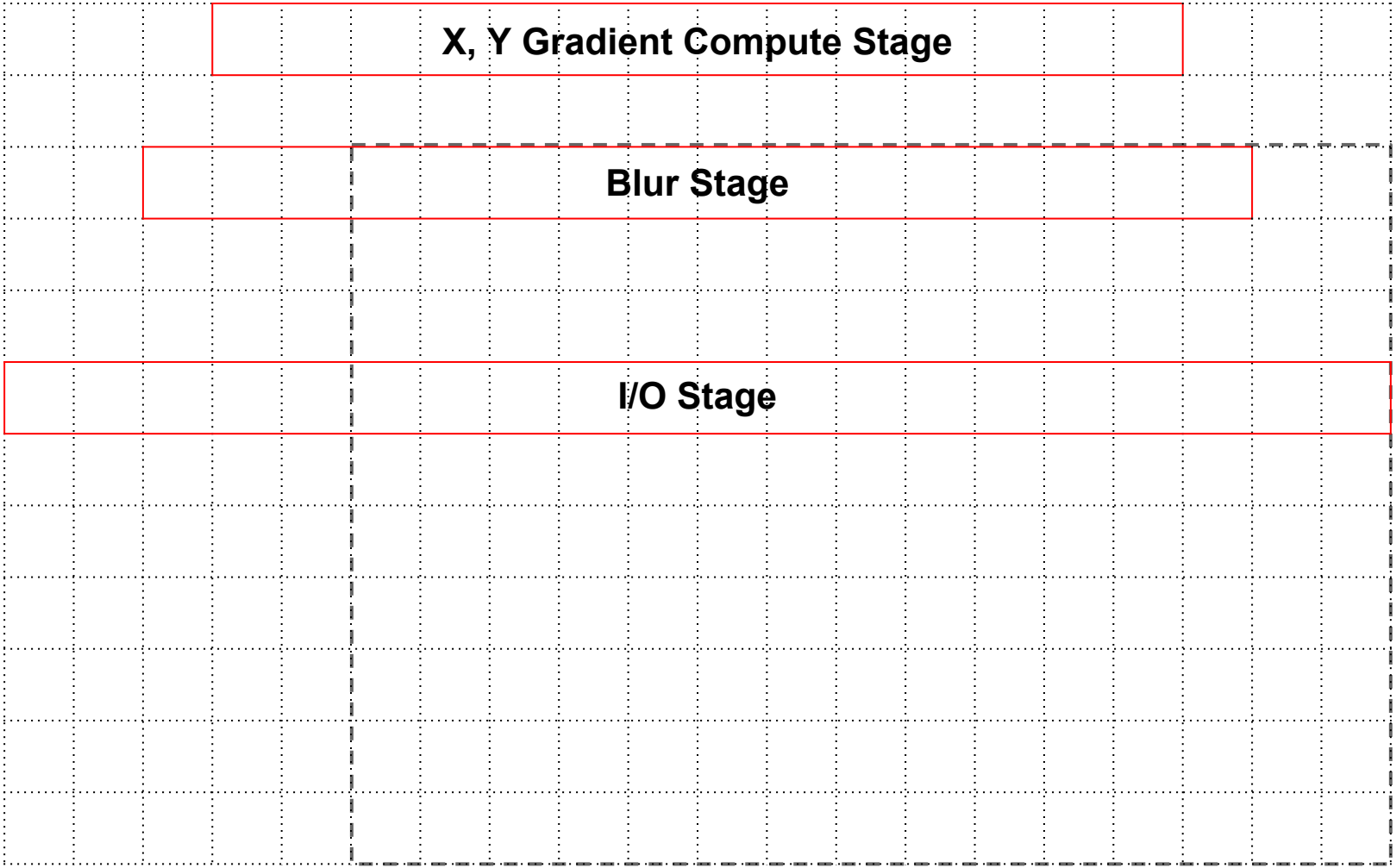
Stages:

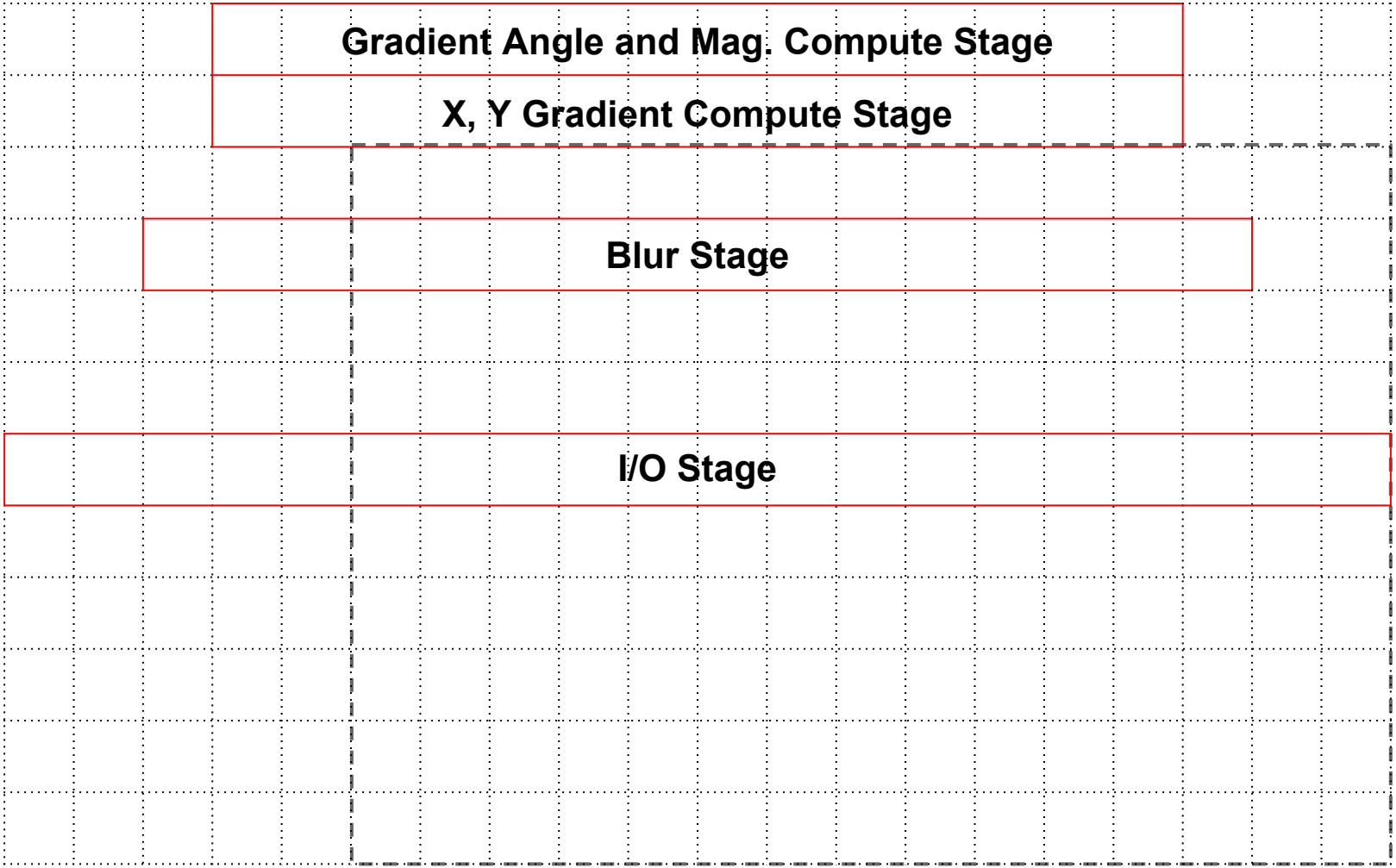
- I/O Stage
- Blur Stage
- X, Y Gradient Compute Stage
- Gradient Angle and Magnitude Compute Stage
- Non Maximal Suppression Stage
- Hysteresis

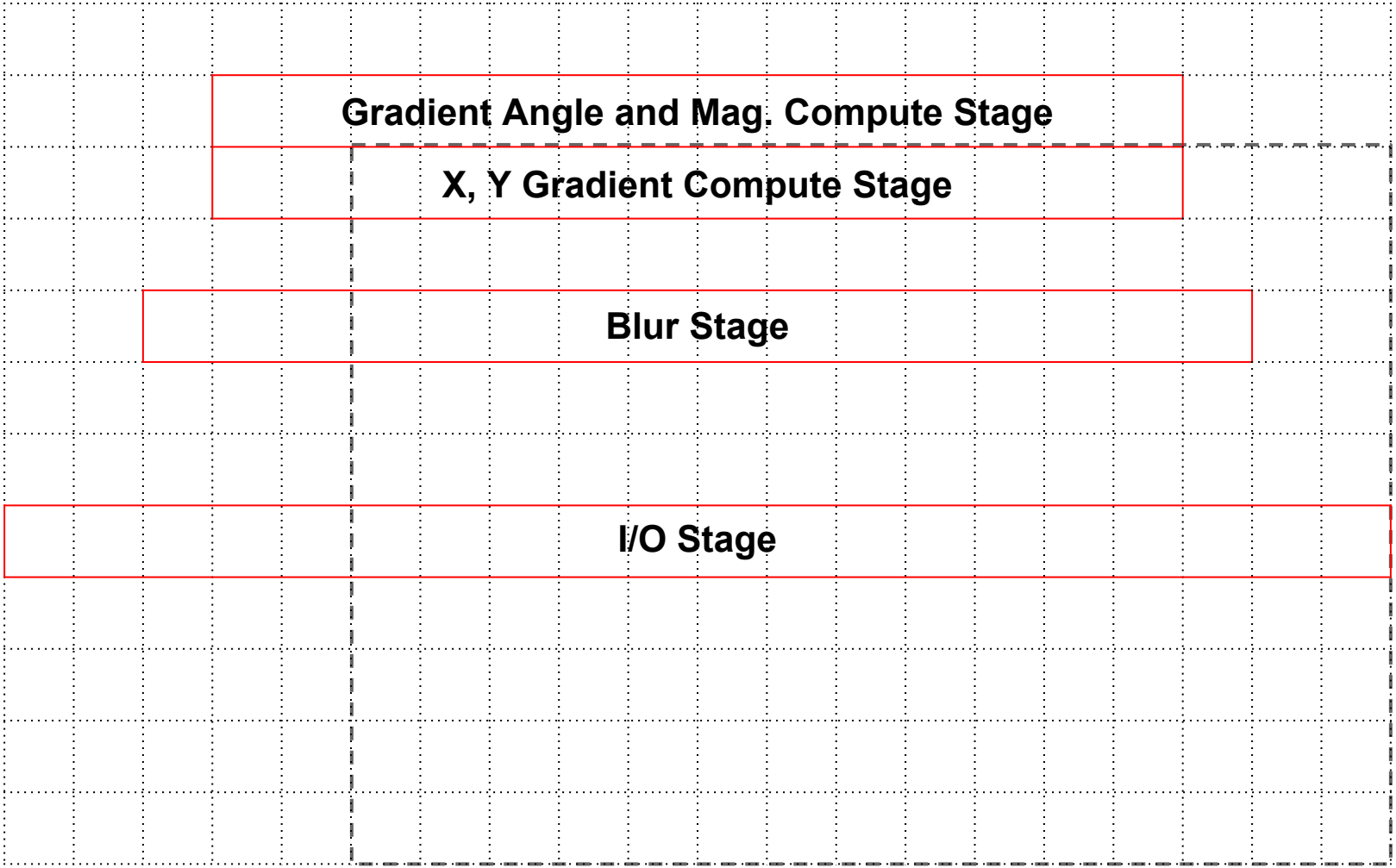

I/O Stage

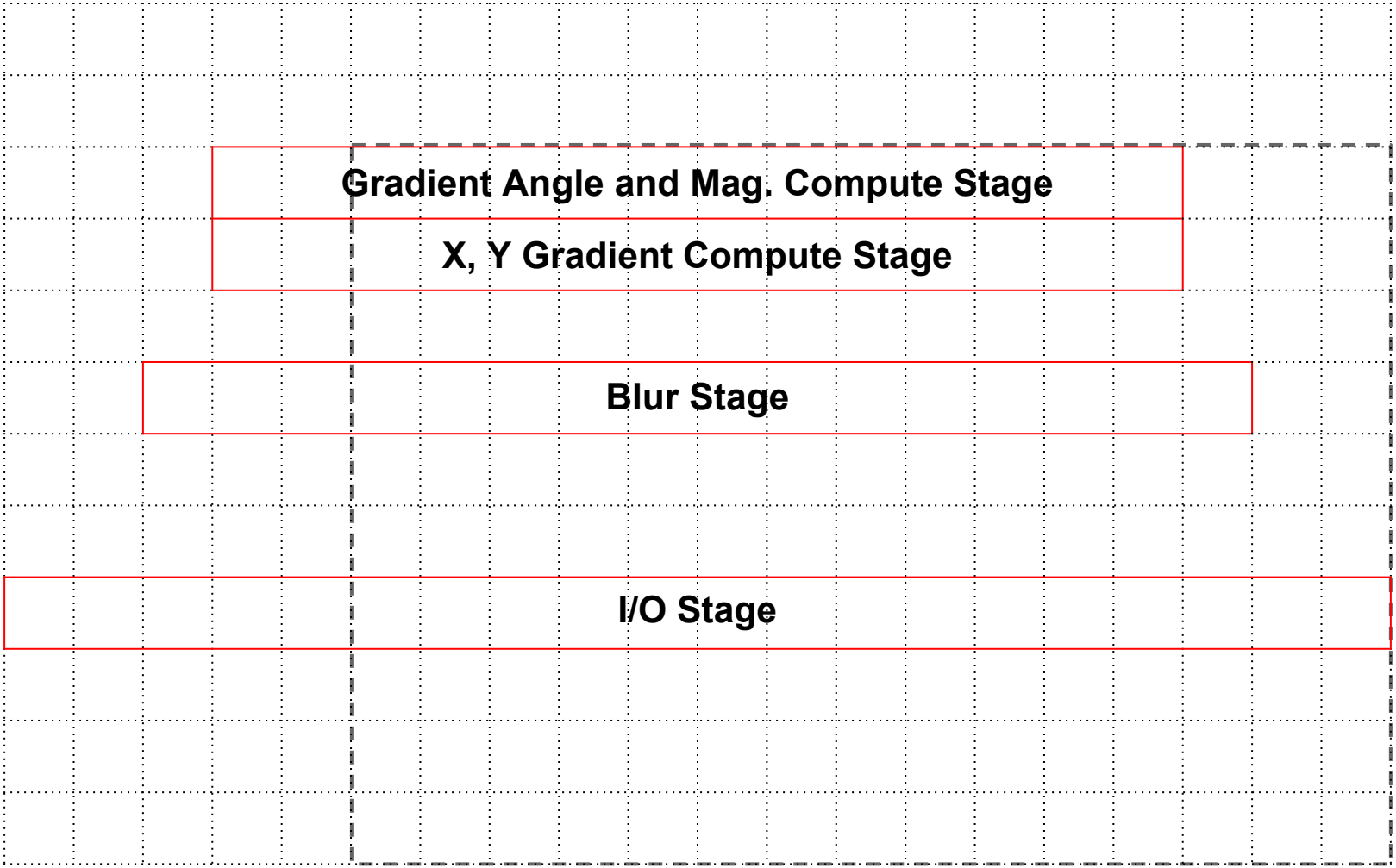

Blur Stage
I/O Stage

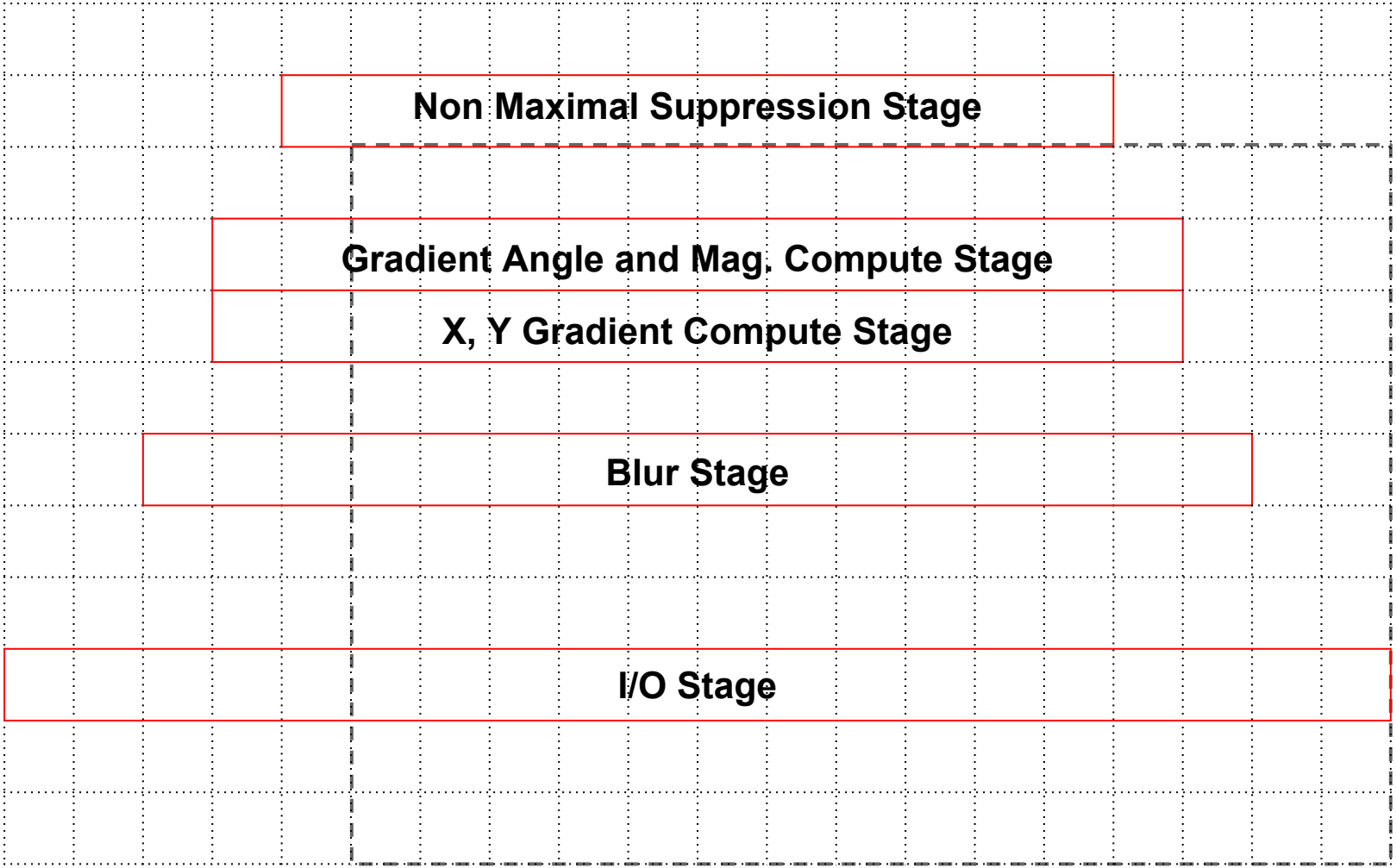

Blur Stage
I/O Stage

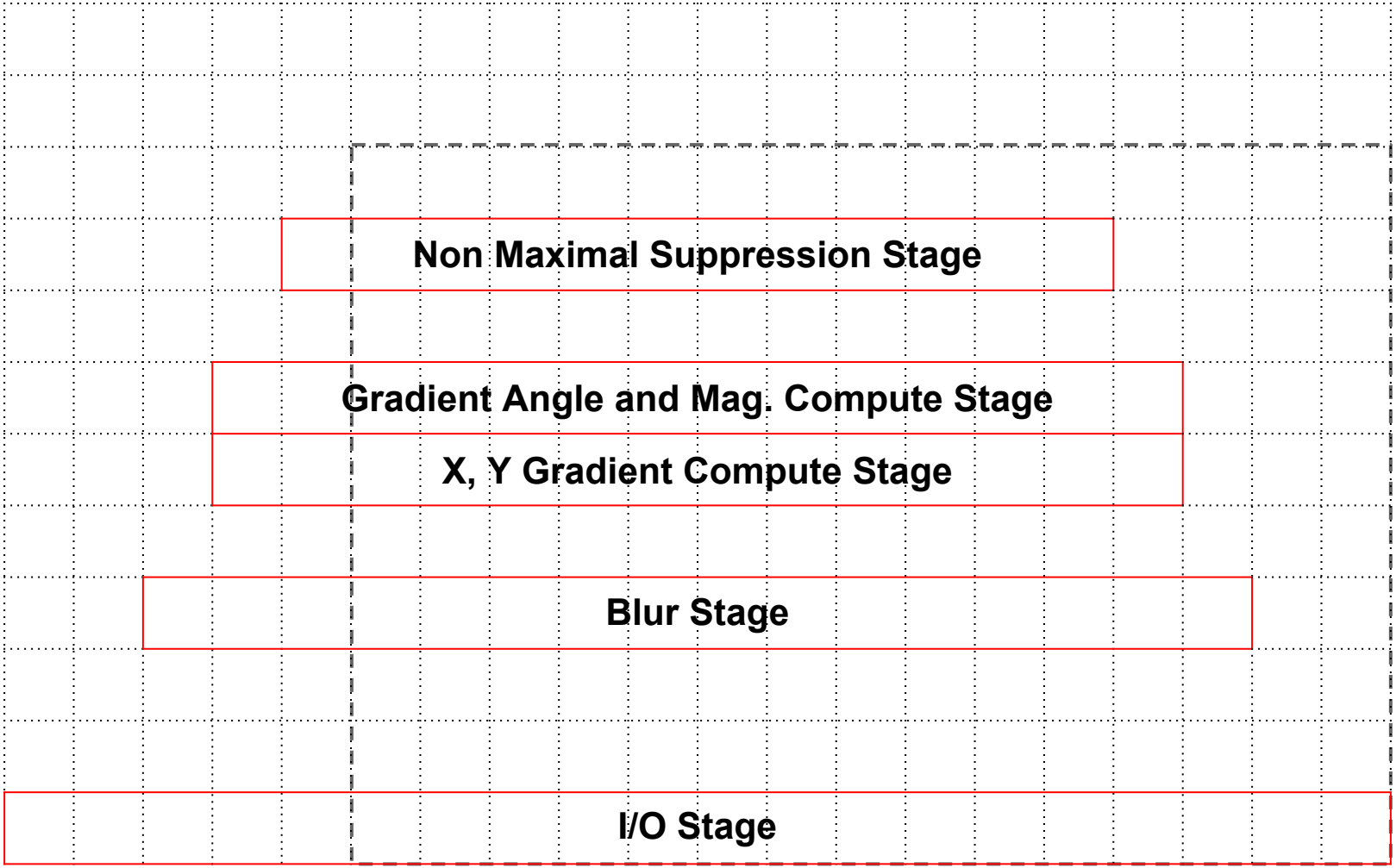

X, Y Gradient Compute Stage
Blur Stage
I/O Stage

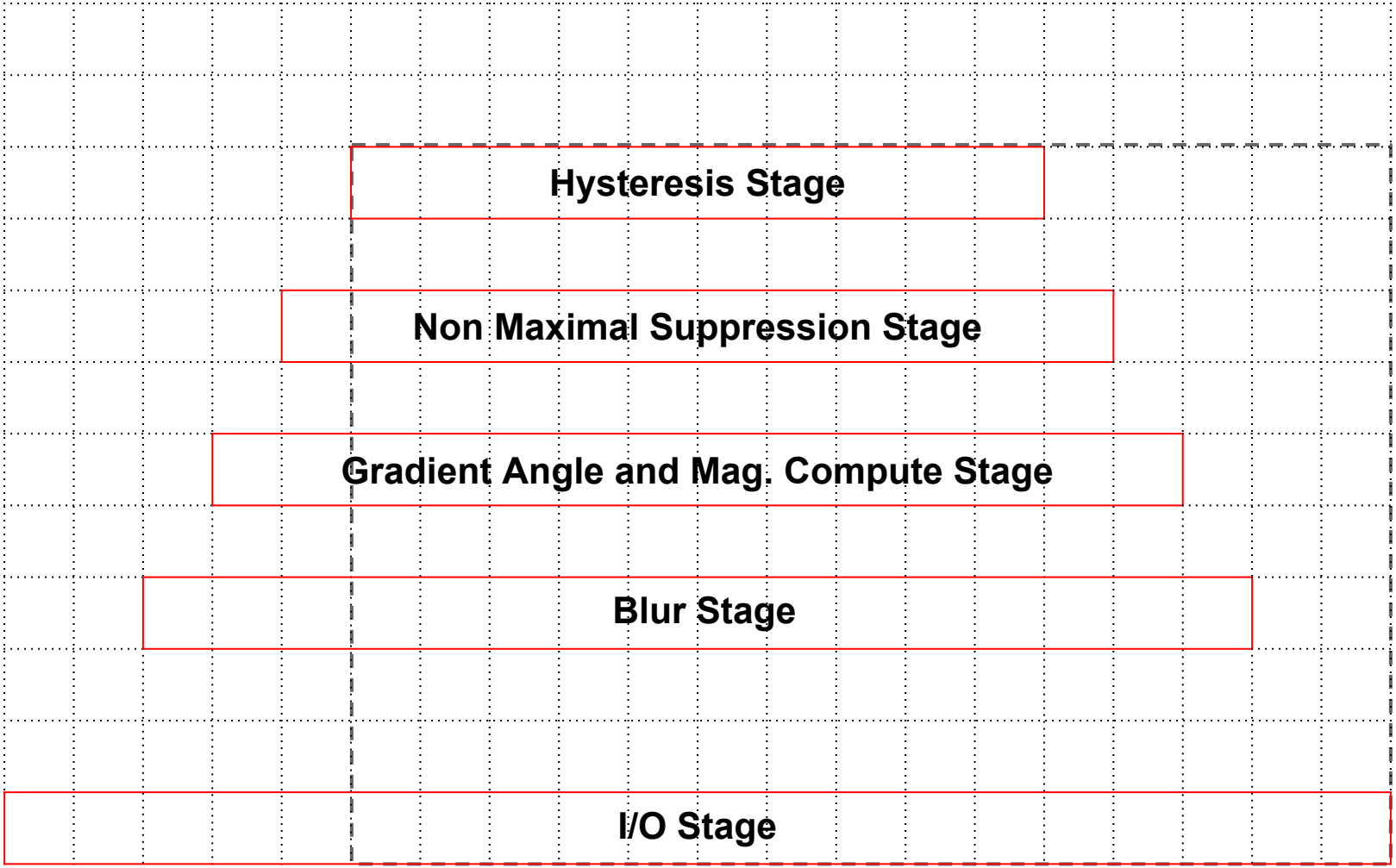

Gradient Angle and Mag. Compute Stage
X, Y Gradient Compute Stage
Blur Stage
I/O Stage

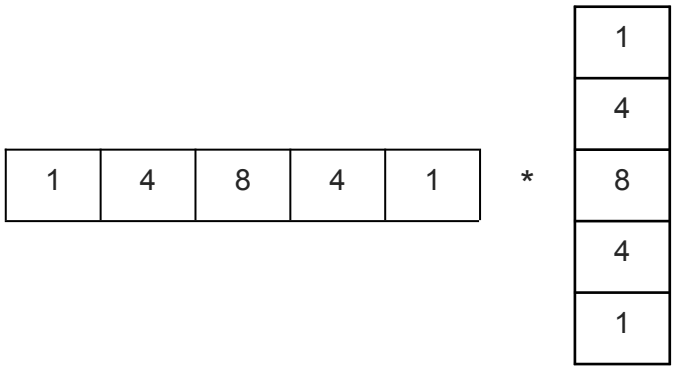

Gradient Angle and Mag. Compute Stage
X, Y Gradient Compute Stage
Blur Stage
I/O Stage


Gradient Angle and Mag. Compute Stage
X, Y Gradient Compute Stage
Blur Stage
I/O Stage


Non Maximal Suppression Stage
Gradient Angle and Mag. Compute Stage
X, Y Gradient Compute Stage
Blur Stage
I/O Stage


Non Maximal Suppression Stage
Gradient Angle and Mag. Compute Stage
X, Y Gradient Compute Stage
Blur Stage
I/O Stage


Hysteresis Stage
Non Maximal Suppression Stage
Gradient Angle and Mag. Compute Stage
Blur Stage
I/O Stage


1
4
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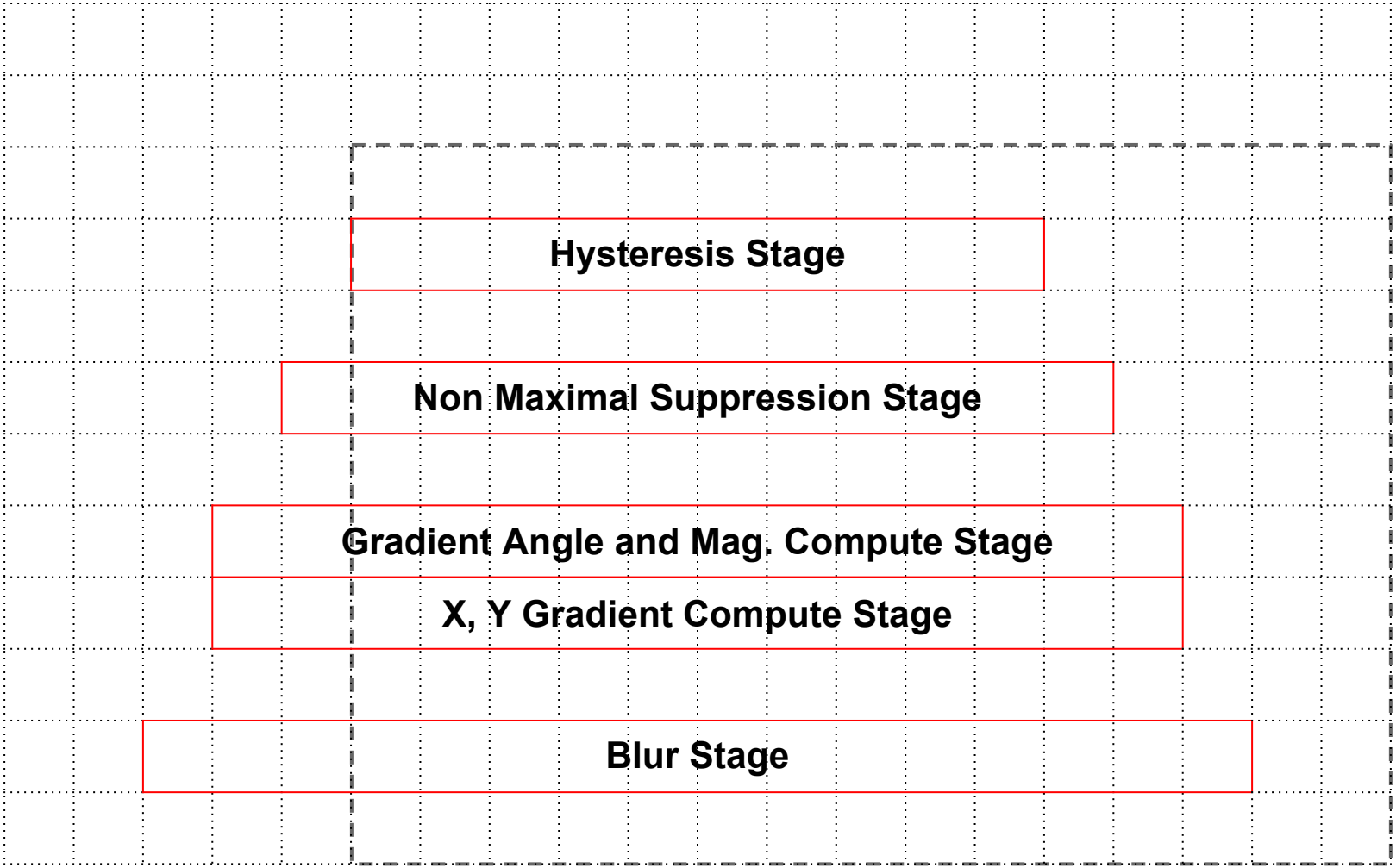

Hysteresis Stage
Non Maximal Suppression Stage
Gradient Angle and Mag. Compute Stage
X, Y Gradient Compute Stage
Blur Stage

Success Criteria

1. Respond to processor's image processing request.

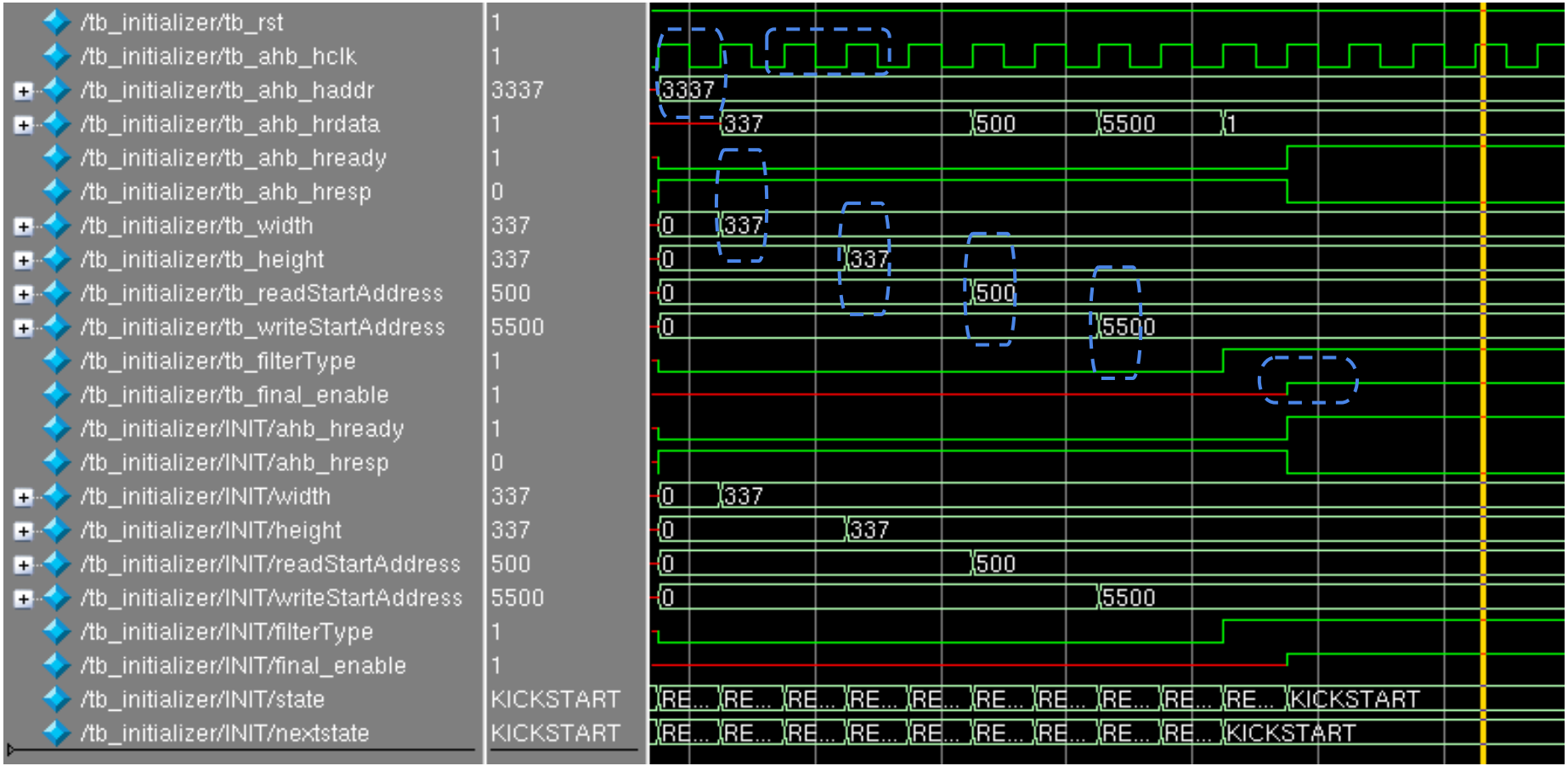
2. Process input images according to settings.

3. Gaussian blur is performed correctly.

4. Edge detection is performed correctly.

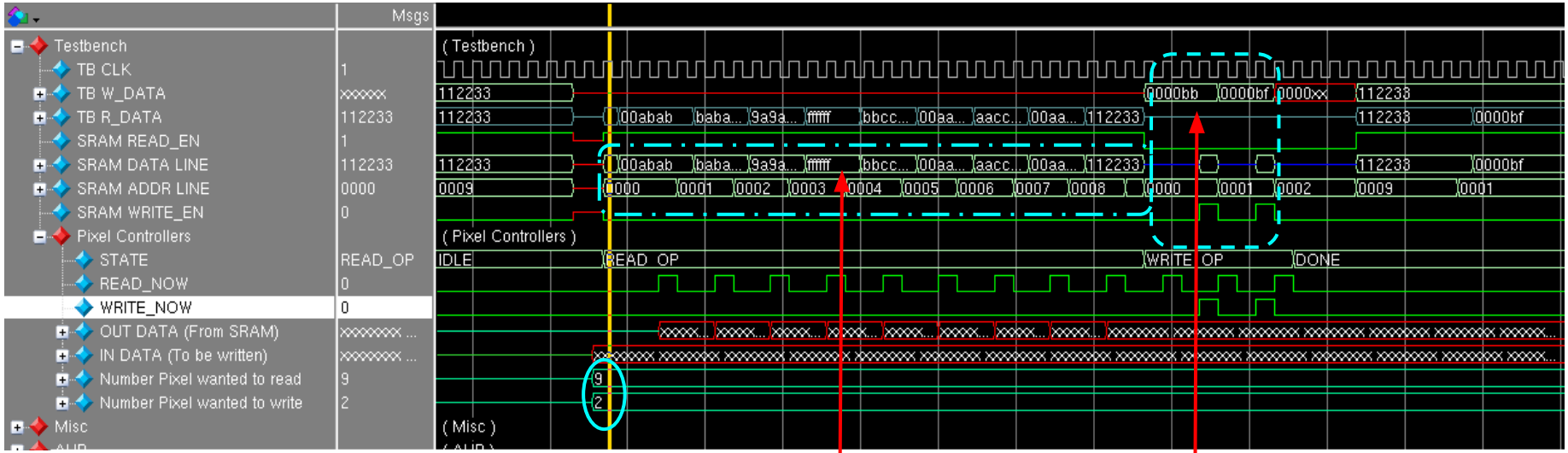
5. Respond to relevant AHB bus signals.

Initializer



Pixel IO

Continuous Read/Write operations

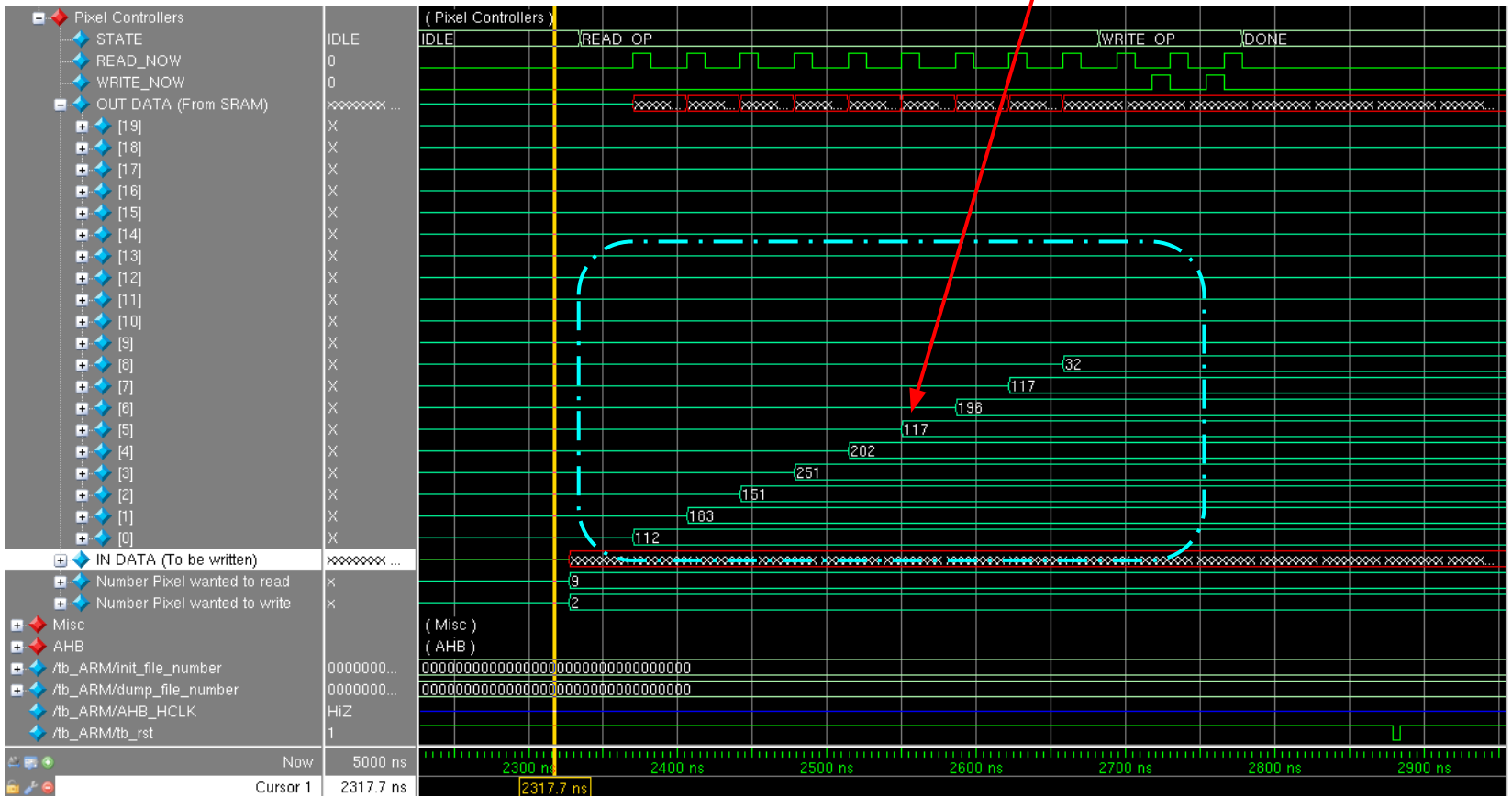


24 bits RGB

8 bits grayscale write

Pixel IO

RBG to Grayscale



Pixel IO

SRAM Dumps

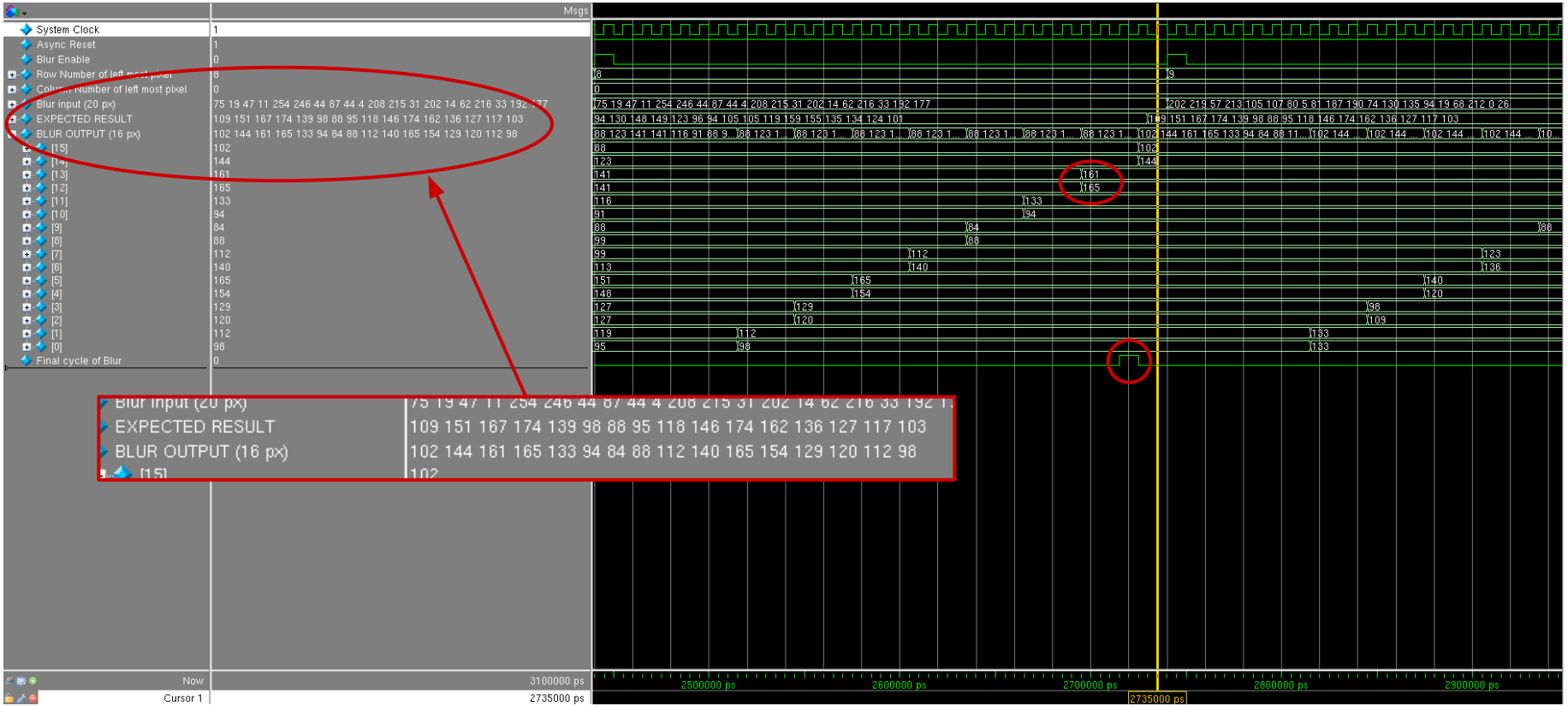
24 bits word size

One RBG pixel (24 bits) per memory location

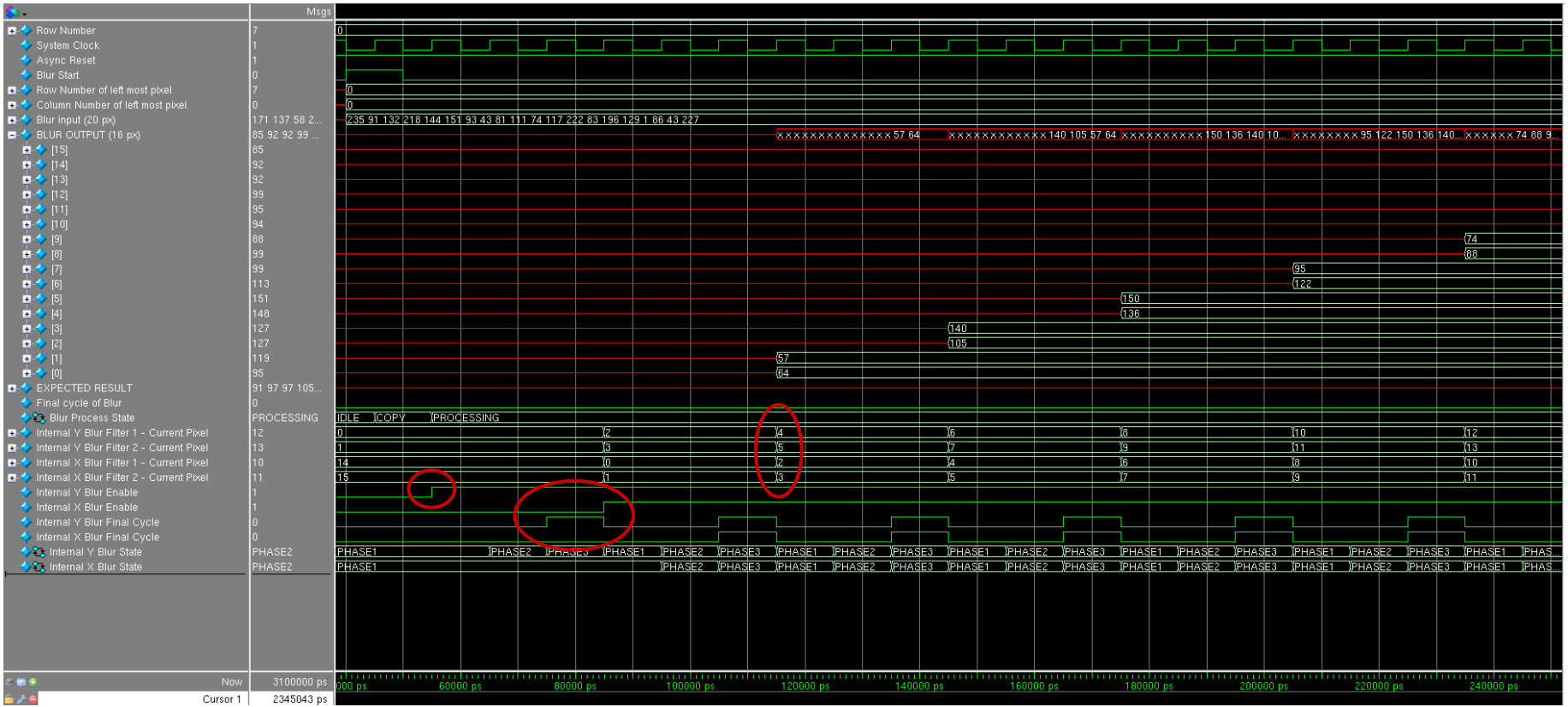
Pre-Write SRAM	Post-Write SRAM
0:00ABAB;	0:0000BB;
1:BABABA;	1:0000BF;
2:9A9A9A;	2:9A9A9A;
3:FFFFFF;	3:FFFFFF;
4:BBCCDD;	4:BBCCDD;
5:00AABB;	5:00AABB;
6:AACCDD;	6:AACCDD;
7:00AABB;	7:00AABB;
8:112233;	8:112233;

Writes grayscale pixel (8 bits) per memory location

Gaussian Blur



Gaussian Blur



Conclusion

- Challenges
  - Performance
  - Chip Area
- If starting over...
  - Realize the power of ASIC better
  - More Parallelization
- If given more time…
  - Image Format support