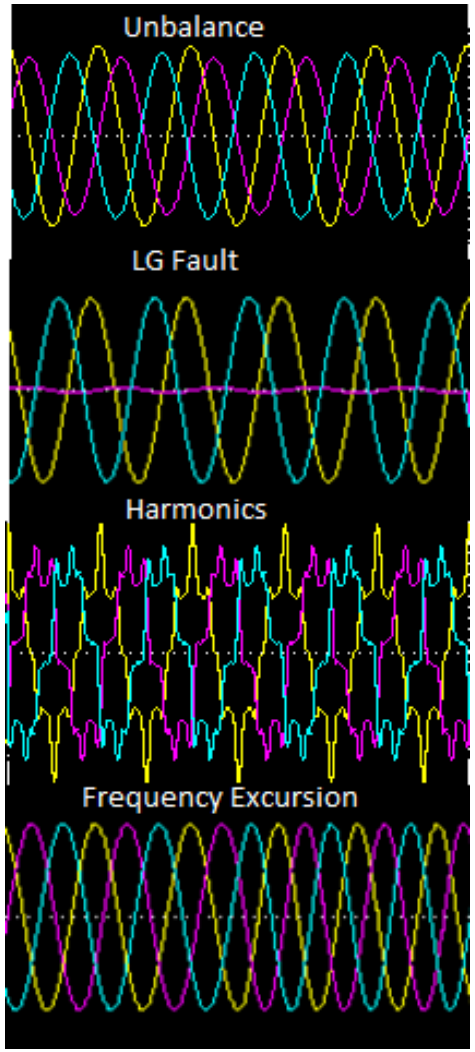
The design and performance optimization of 3-phase PLLs for phase tracking under grid imperfections



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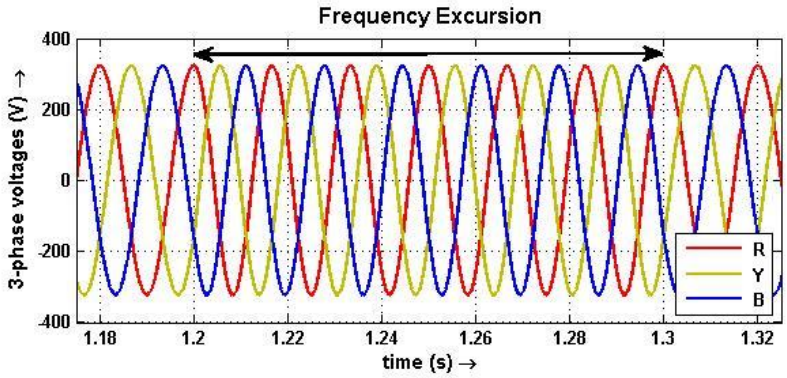
Objective:
Phase tracking

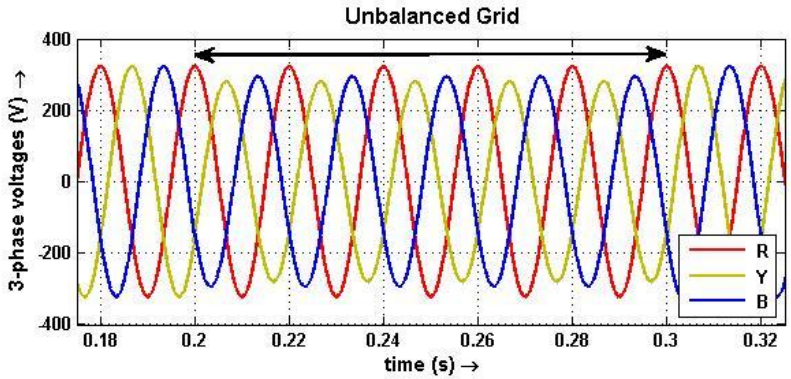
Depth of work:

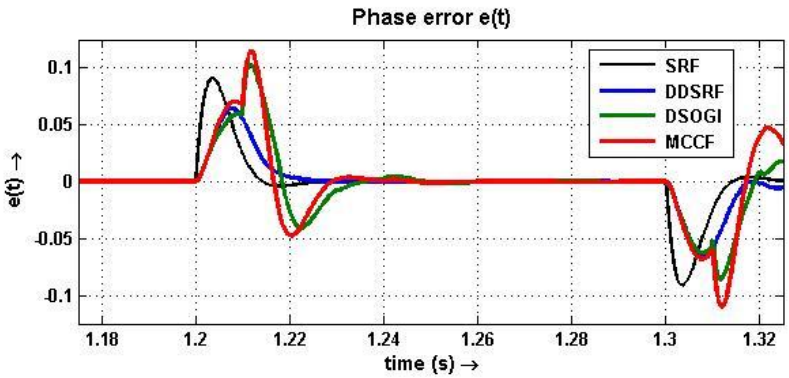
1. **Detailed analysis of 4 PLL schemes in literature** (SRF, DDSRF, DSOGI, MCCF)
   i. Mathematical modeling
   ii. Simulation to match results from literature
   iii. Intuitive plot program for comparison between schemes
2. **Novel loop filter design**
   i. Self-consistent model based approach
   ii. Comparisons of existing design schemes with the proposed scheme
   iii. Development of a 3D lookup table
3. **Experimentation** (in progress)

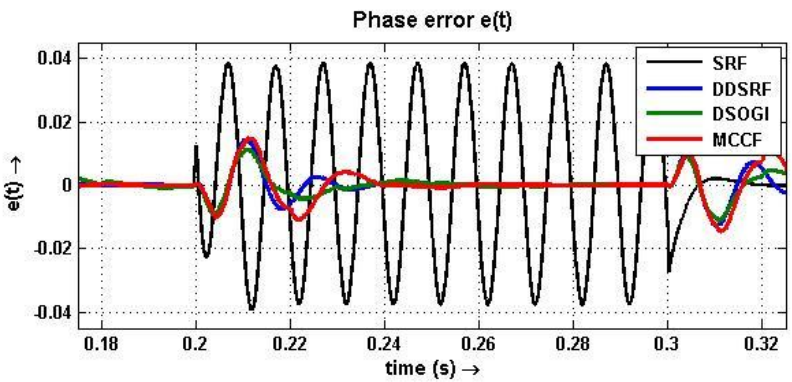
Detailed analysis of 4 PLL schemes in literature

1. PLL schemes developed: SRF, DDSRF, DSOGI, MCCF
   - SRF – Synchronous Reference Frame PLL
   - DDSRF – Decoupled Double Synchronous Reference Frame PLL
   - DSOGI – Dual Second Order Generalized Integrator based 3-phase PLL
   - MCCF – Multiple Complex Coefficient Filter based 3-phase PLL
2. Comprehensive Simulink models
3. Intuitive plot program (at least 200 comparisons possible!!)



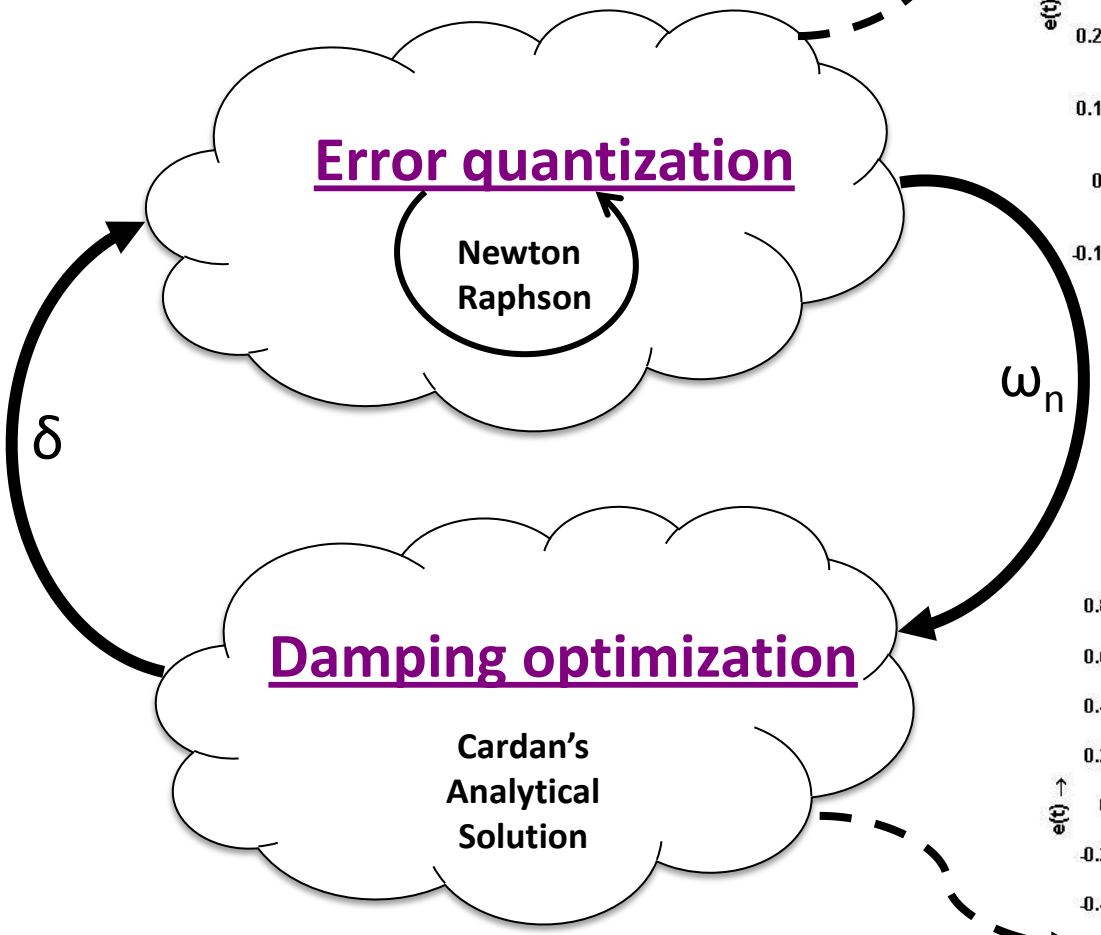


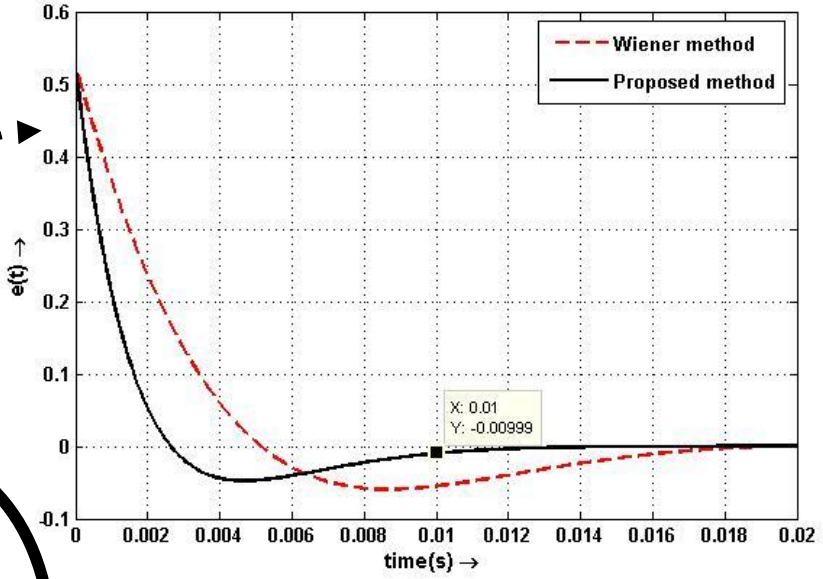


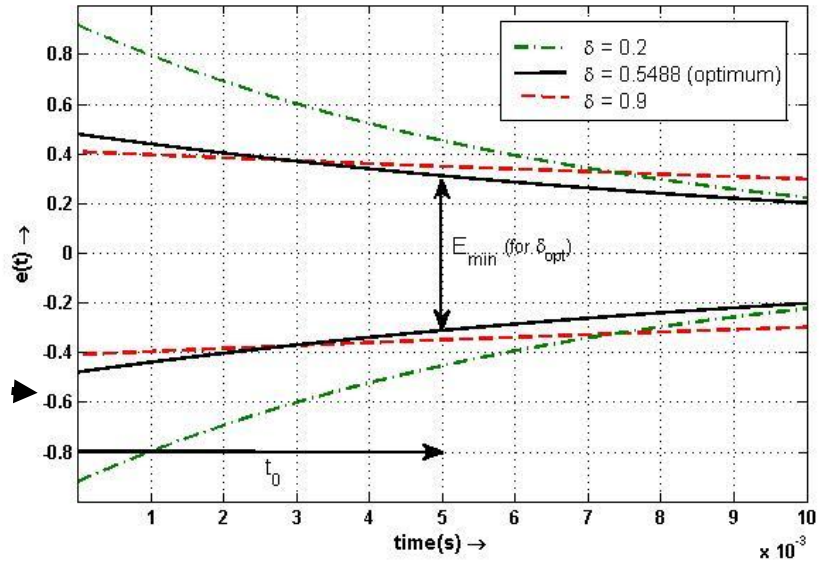


Novel loop filter design

Need: decoupling of dynamic performance and filtering characteristic



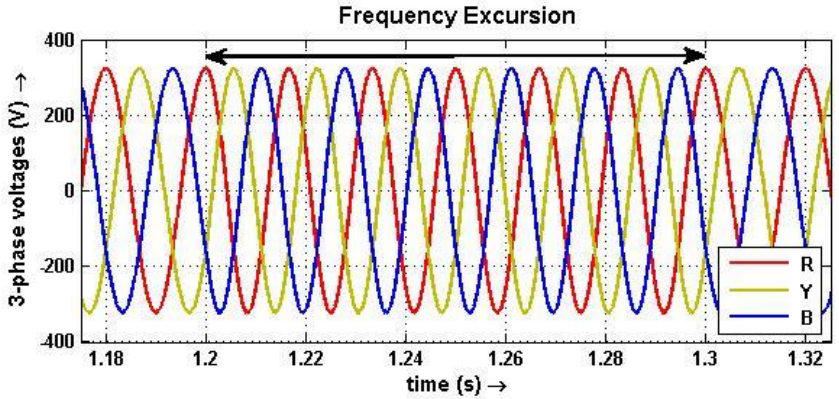


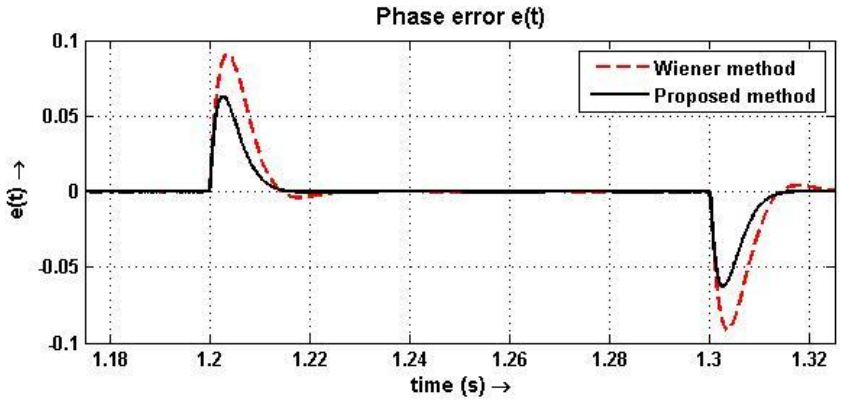


Gives a unique set of loop filter parameters k_p and k_i - no trial and error

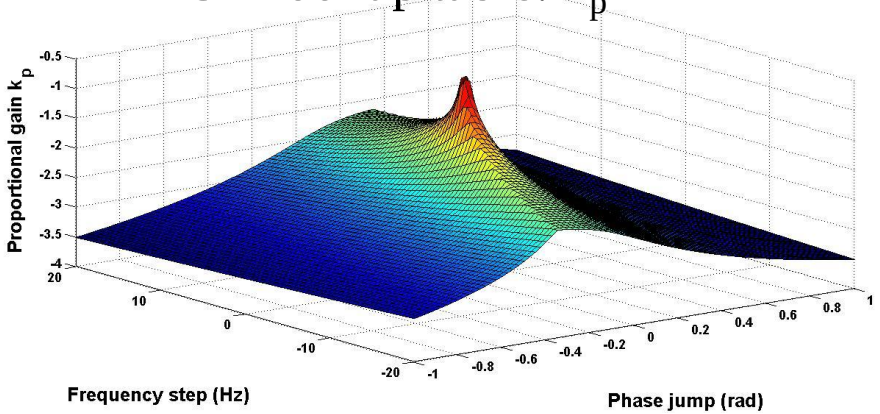
Novel filter design (continued)

1. Comparisons with Wiener method
   i. Better dynamic performance
   ii. Extremely convenient from user's perspective
2. Development of a 3D lookup table
   i. Theoretical aspect:
   Can be used as an educational tool to make notable inferences
   ii. Practical aspect:
   Eliminate constraints on the speed and computing power of the micro-controller/ DSP

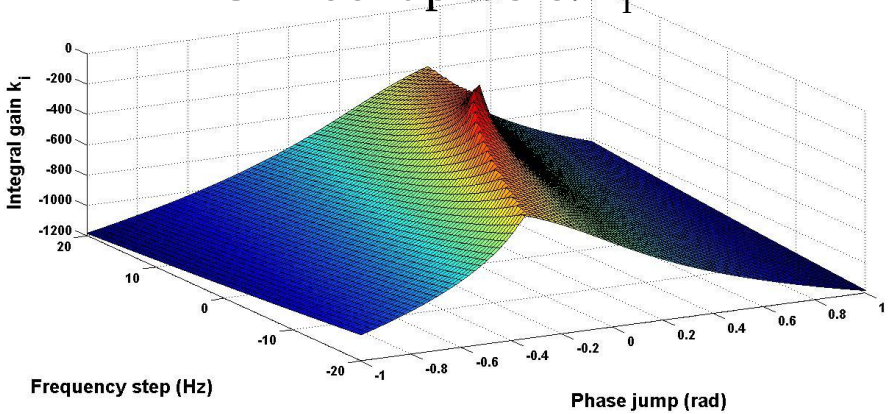




3D lookup table: k_p



3D lookup table: k_i



Conclusions

1. Analysis and in-depth understanding of 4 existing PLL schemes
2. Development of a generalized software applet
   - Excellent learning tool
   - Easy to use
   - To find out which scheme tackles a particular issue better
   - Additions of other schemes (if required) can be easily done
3. Novel self-consistent model based loop filter design
   - No trial and error as a unique (k_p , k_i) pair for a particular grid condition
   - Both error and damping is optimized
   - 3D lookup table for easy hardware implementation
4. Hardware implementation
   - MSP430 Launchpad is used and the ADC and PWM modules are interfaced
   - Yet to create a frequency excursion to test the SRF PLL implementation

Future work

- Use of the 3D lookup table for re-configurable filter design
- Hardware testing of the proposed design on the other PLL schemes

Thank you

Conventional SRF PLL

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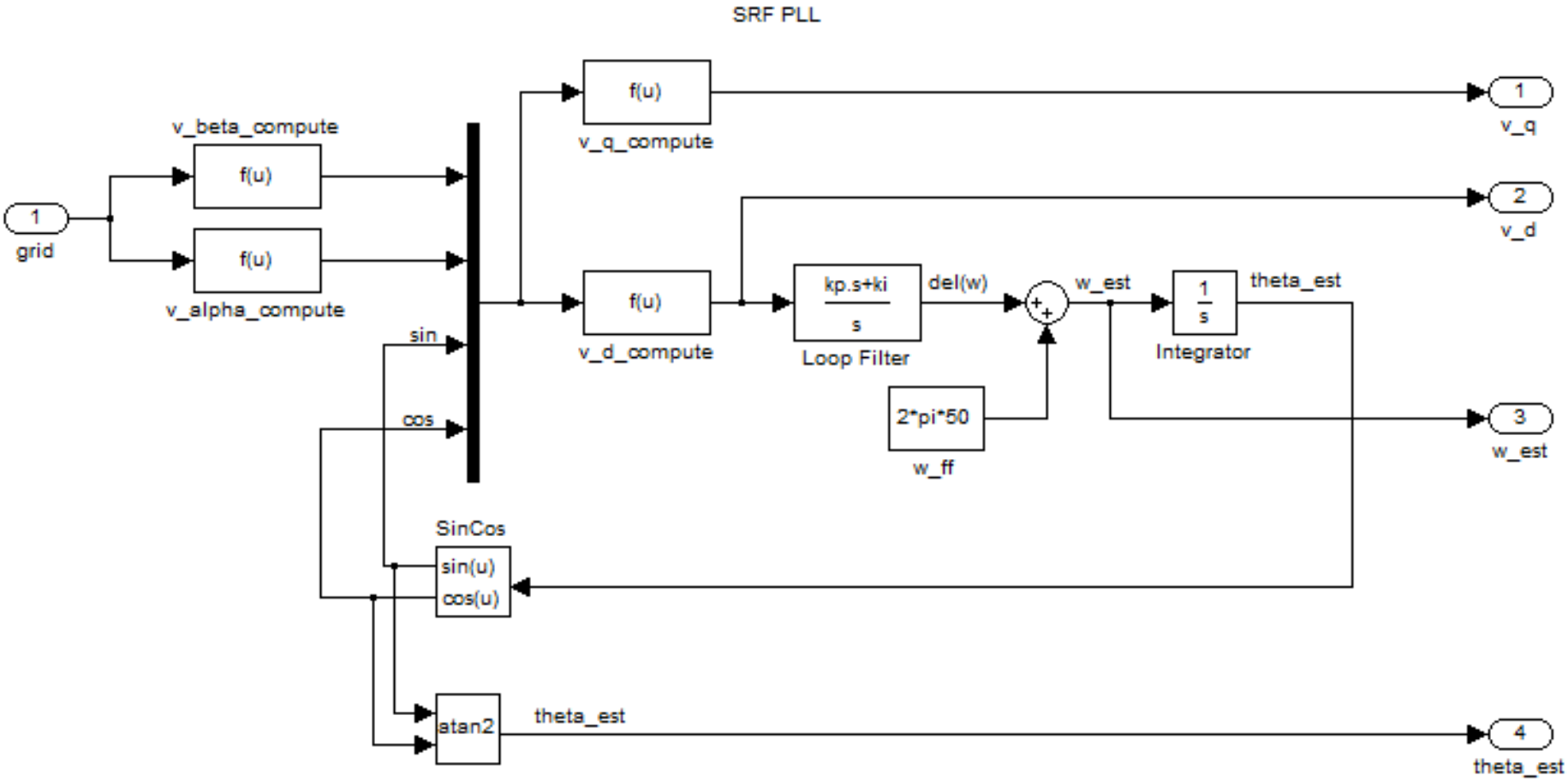

DDSRF PLL

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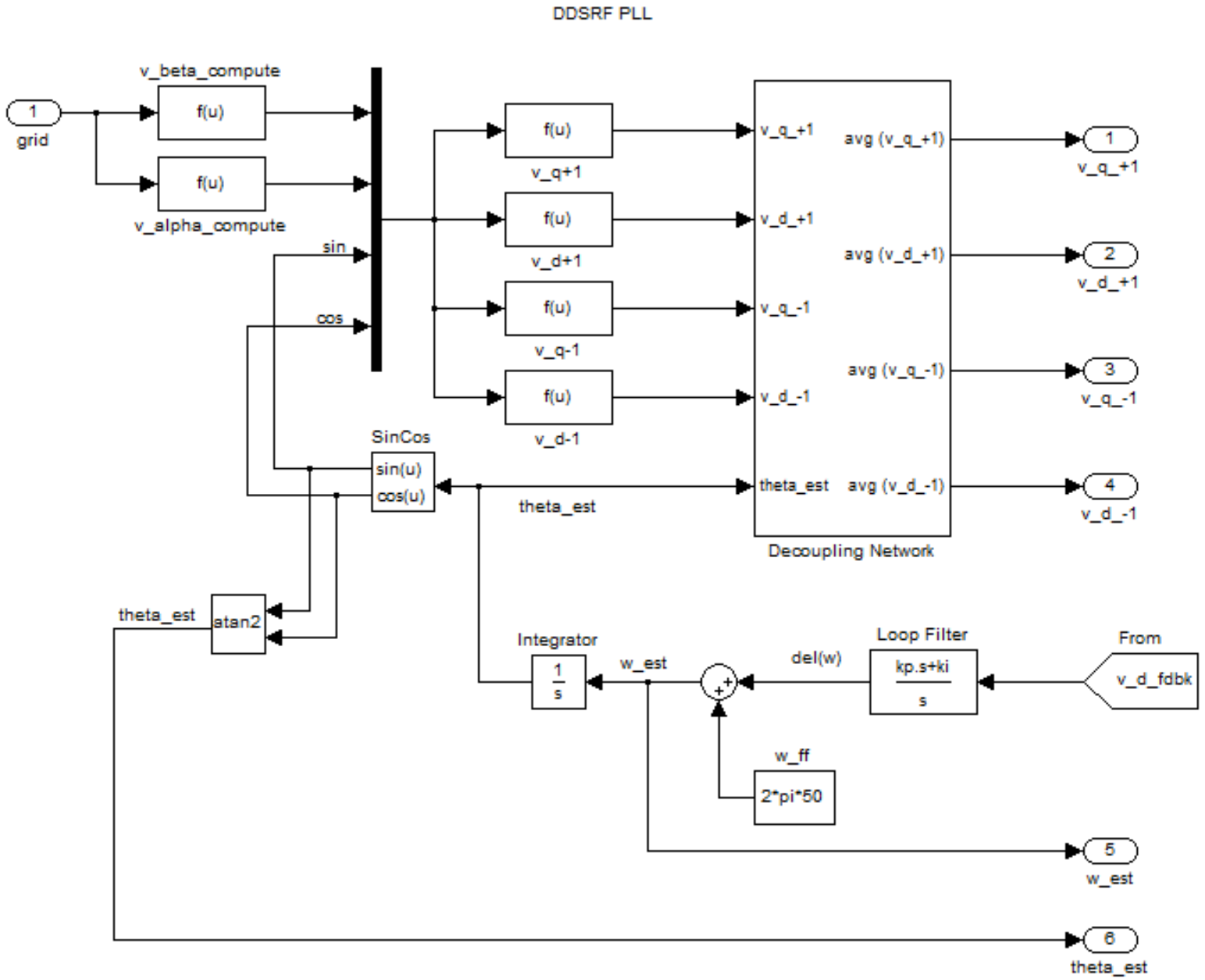

DSOGI PLL

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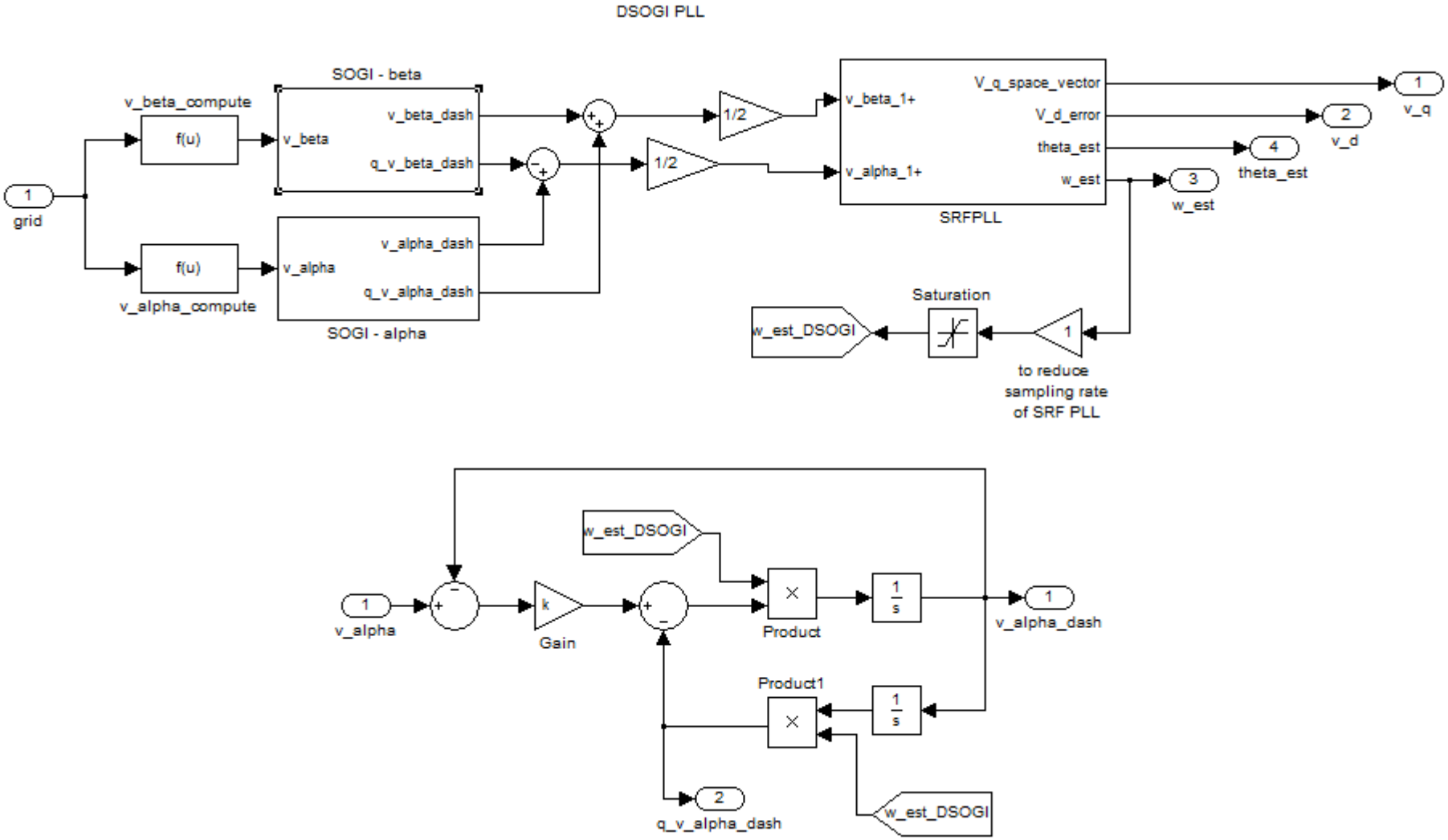

MCCF PLL

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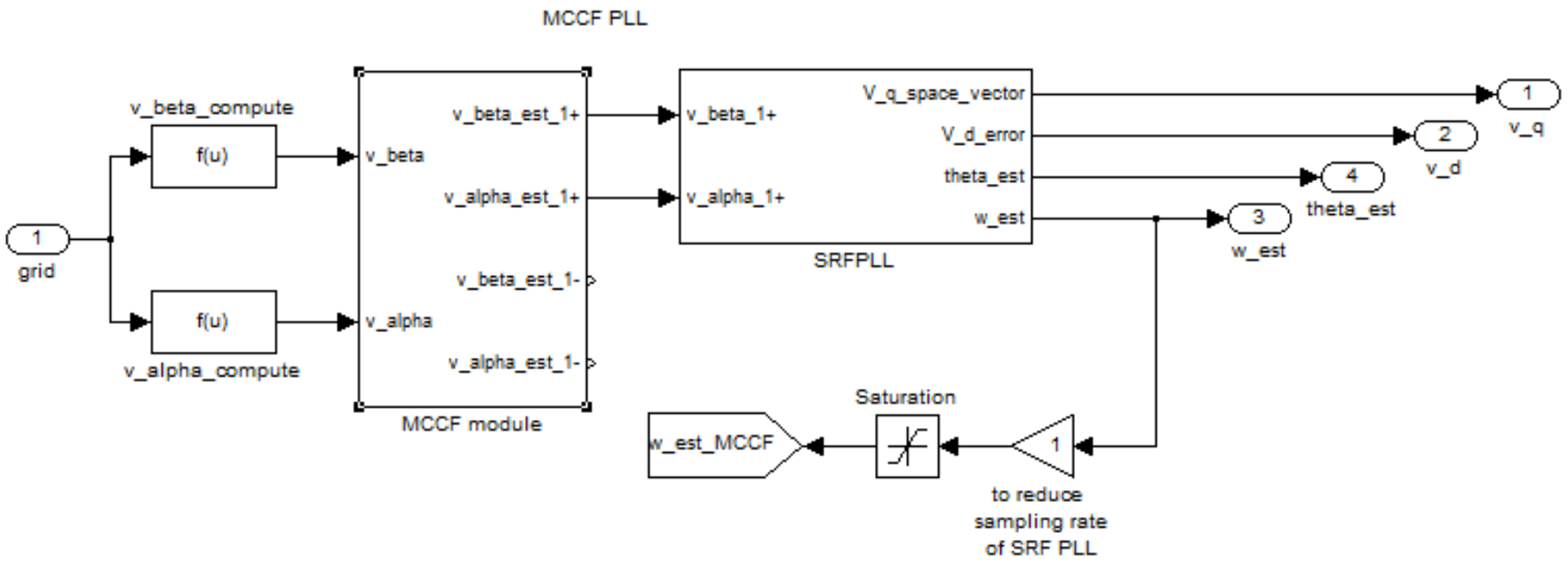
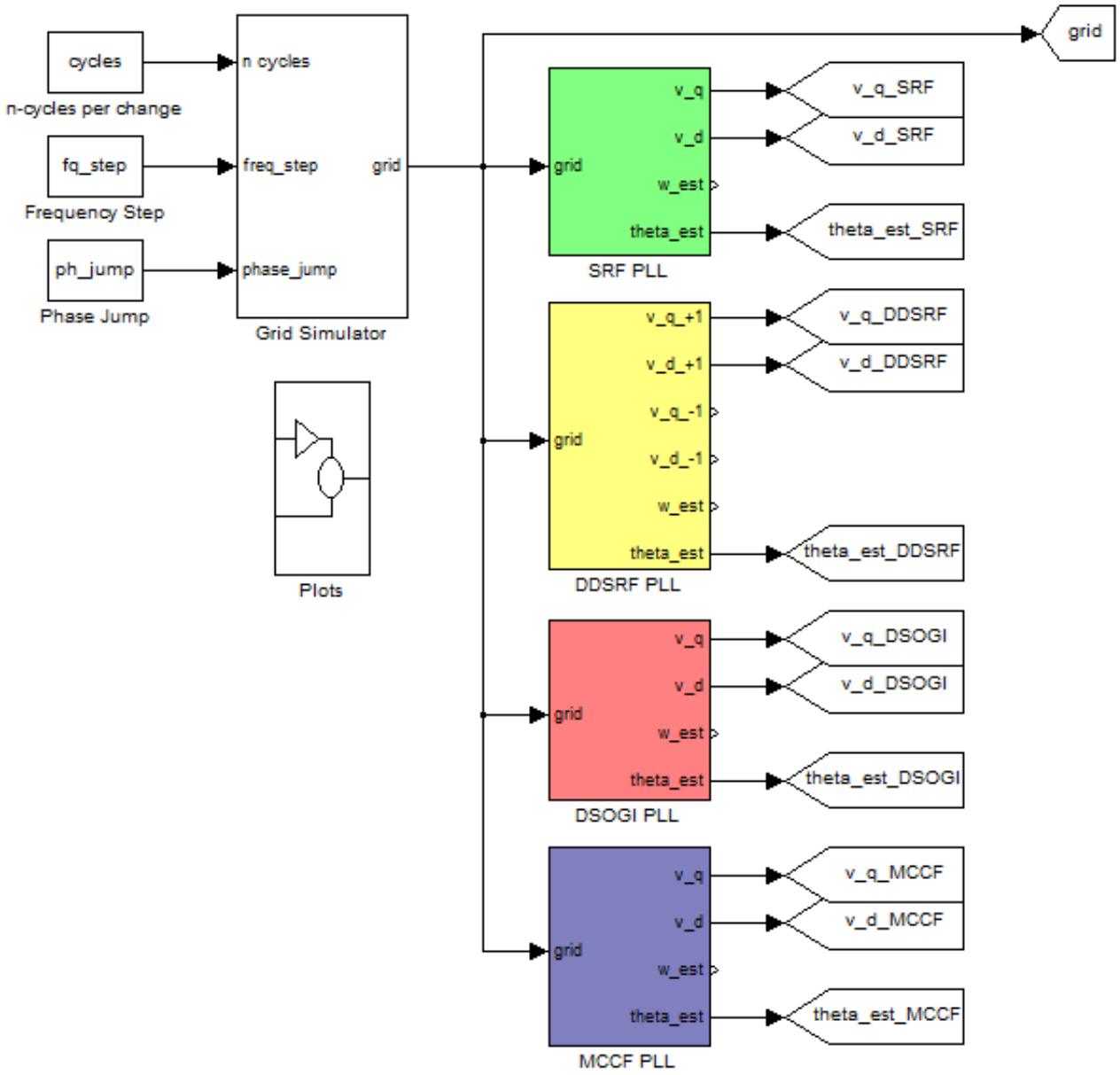


4 PLLs simulated on a single model



The grid simulator used to create imperfect grid conditions

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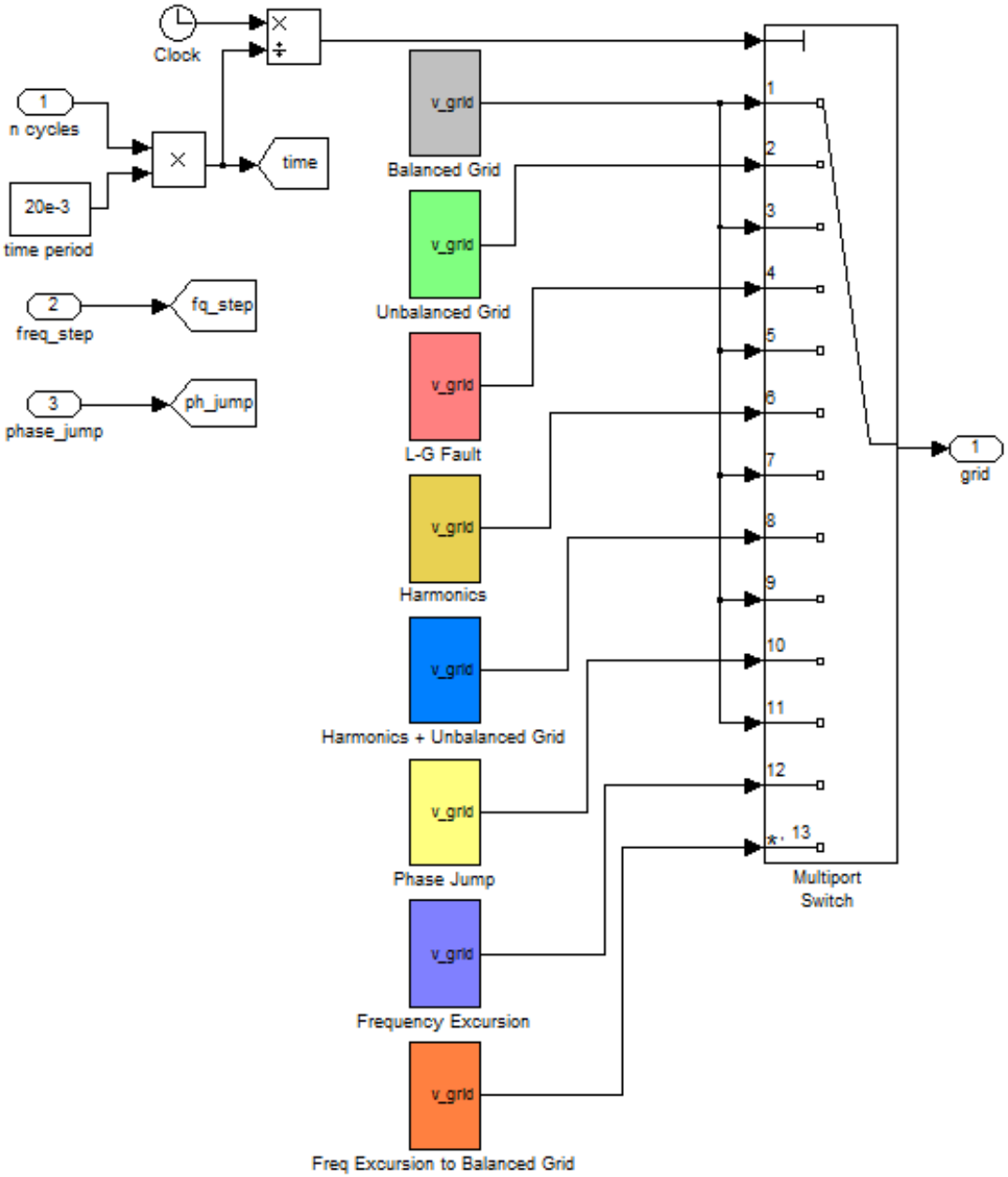

Intuitive plot program results

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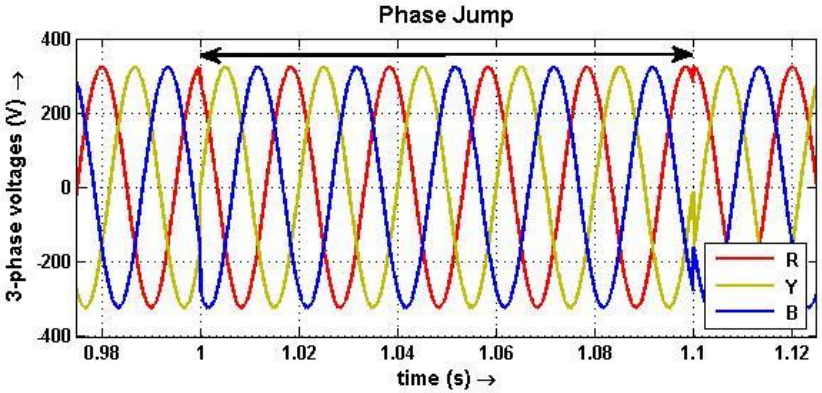

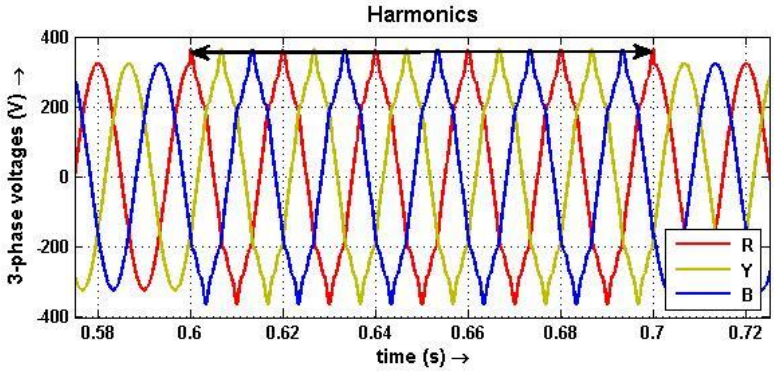

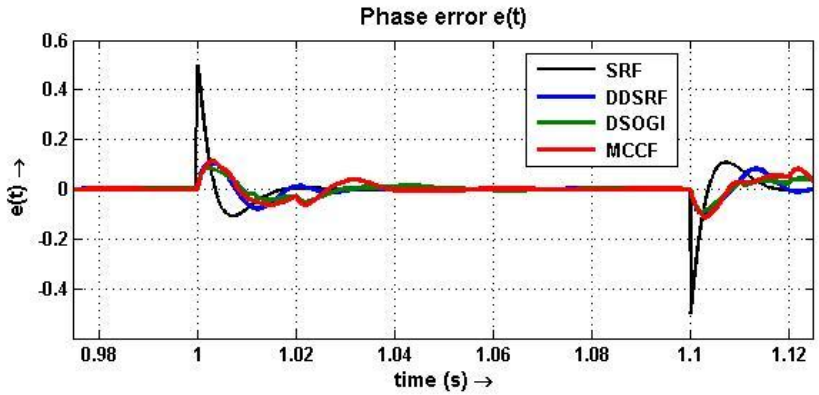

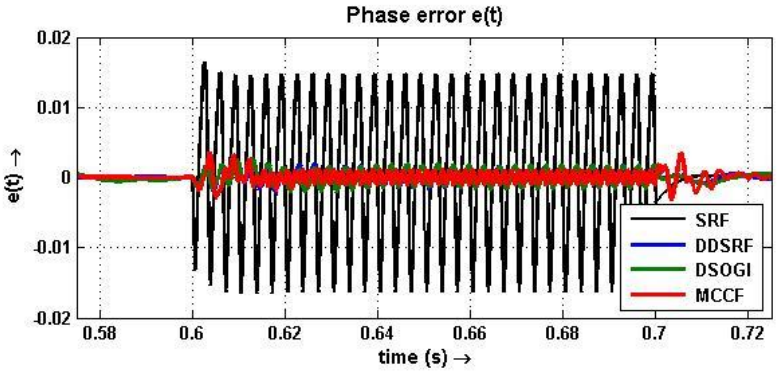

Error quantization

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$$E = \frac{2e^{-\delta\omega_n t_0}}{\omega_n\sqrt{1-\delta^2}}\sqrt{\Delta\omega_{step}{}^2 + \phi^2\omega_n{}^2 - 2\Delta\omega_{step}\phi\omega_n\delta}$$

Damping optimization

Back

$$(-2\omega_n t_0 c_2)\delta^3 + (-c_2 + \omega_n t_0 c_1)\delta^2 + (c_1 + 2\omega_n t_0 c_2)\delta + (-c_2 - \omega_n t_0 c_1) = 0$$

$$\text{where} \qquad c_1 = \Delta\omega_{step}{}^2 + \phi^2 \omega_n{}^2$$

$$c_2 = \Delta\omega_{step}\phi\omega_n$$

Filtering characteristic v/s Dynamic response

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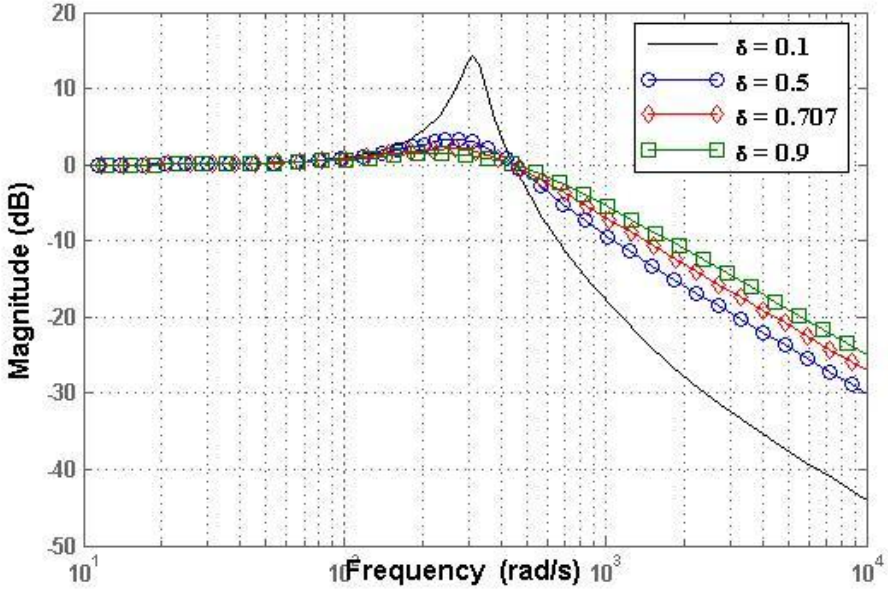
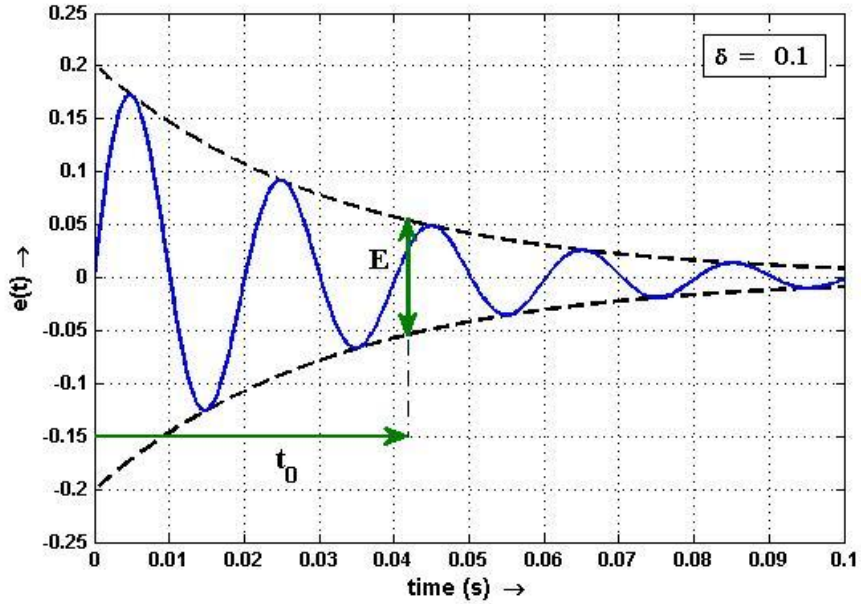




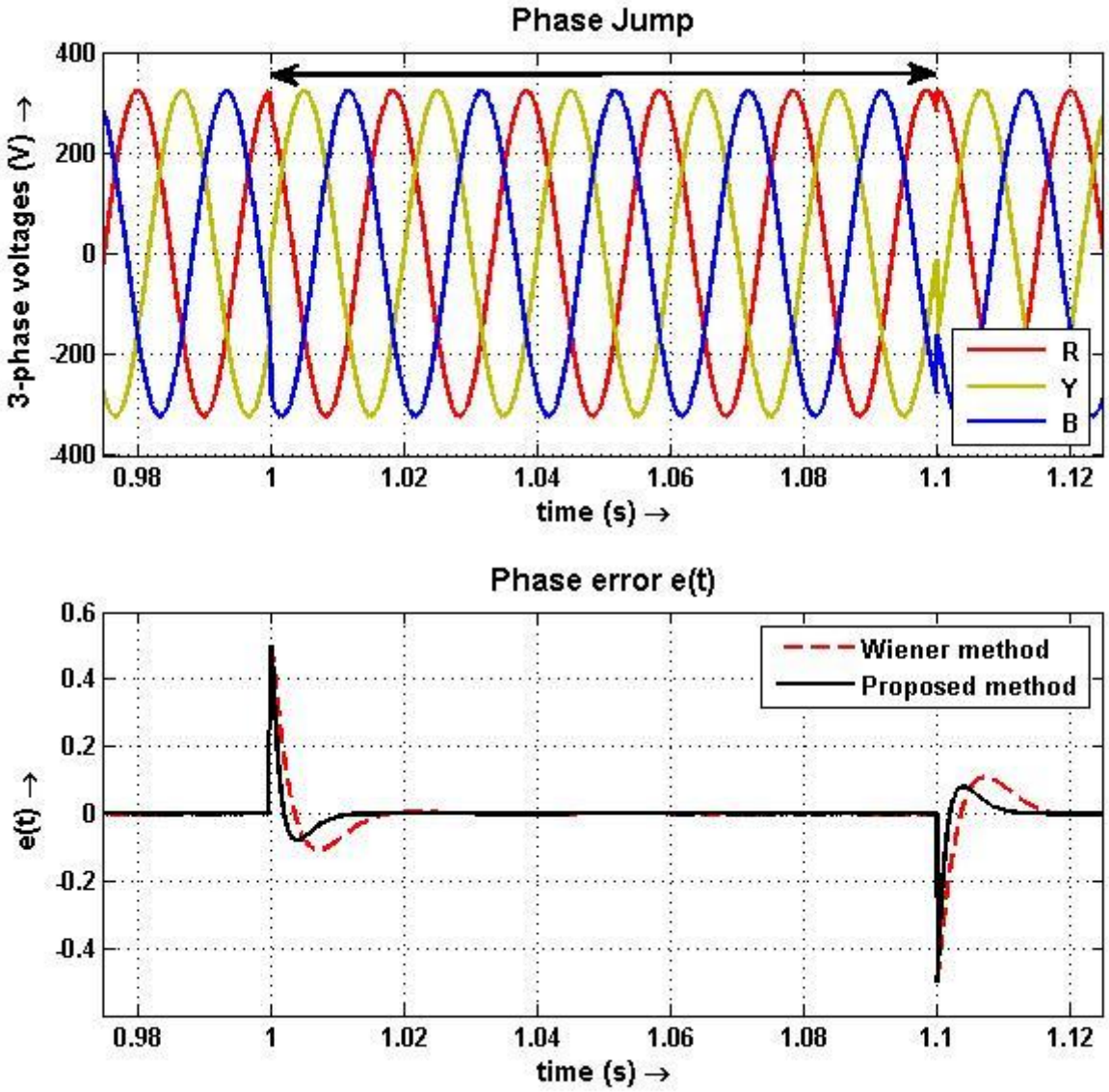
$$Filtering \rightarrow \frac{1}{Bandwidth}$$

Dynamic performance → Bandwidth

Wiener method: good trade-off between filtering and dynamic response

Proposed method: focus is on dynamic response

Comparisons – SRF PLL on phase jump



Comparisons

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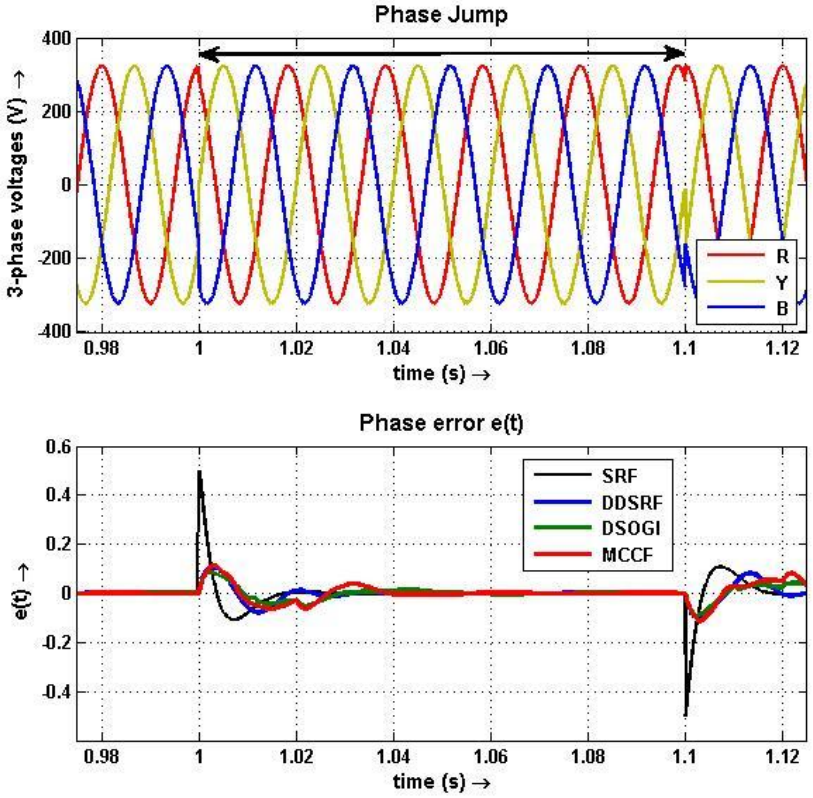
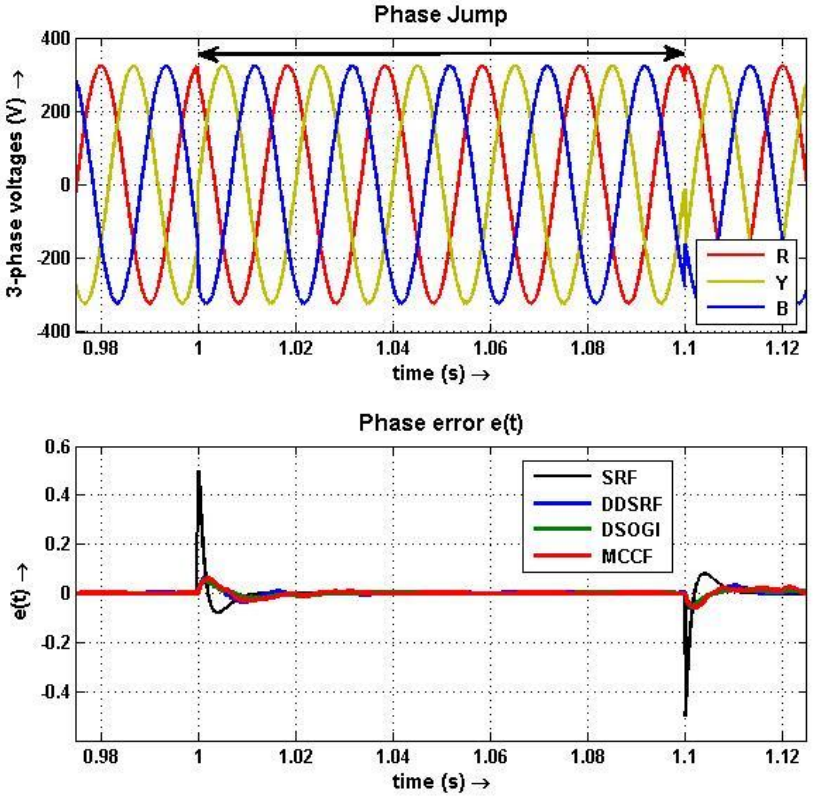
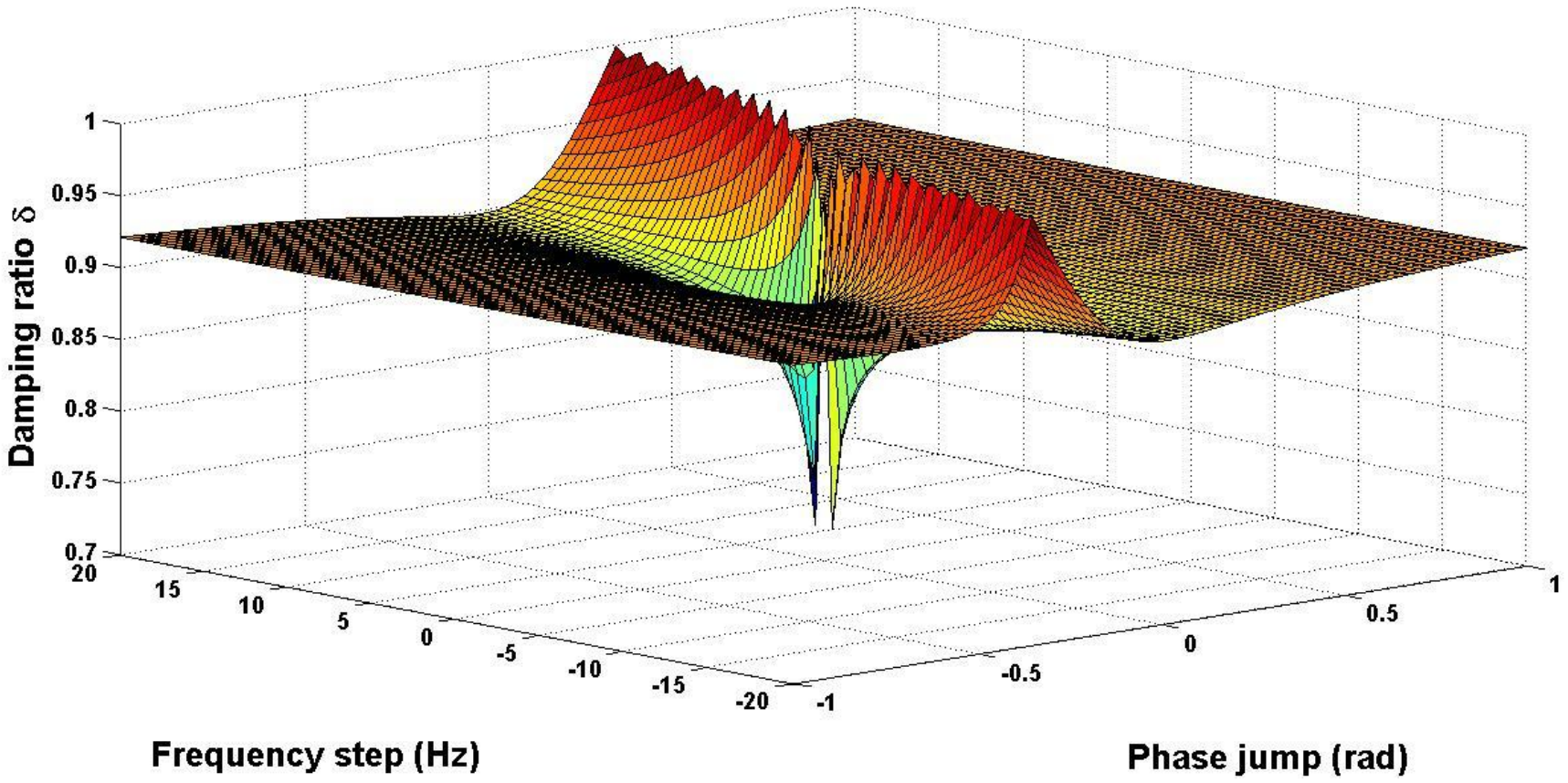


Wiener method

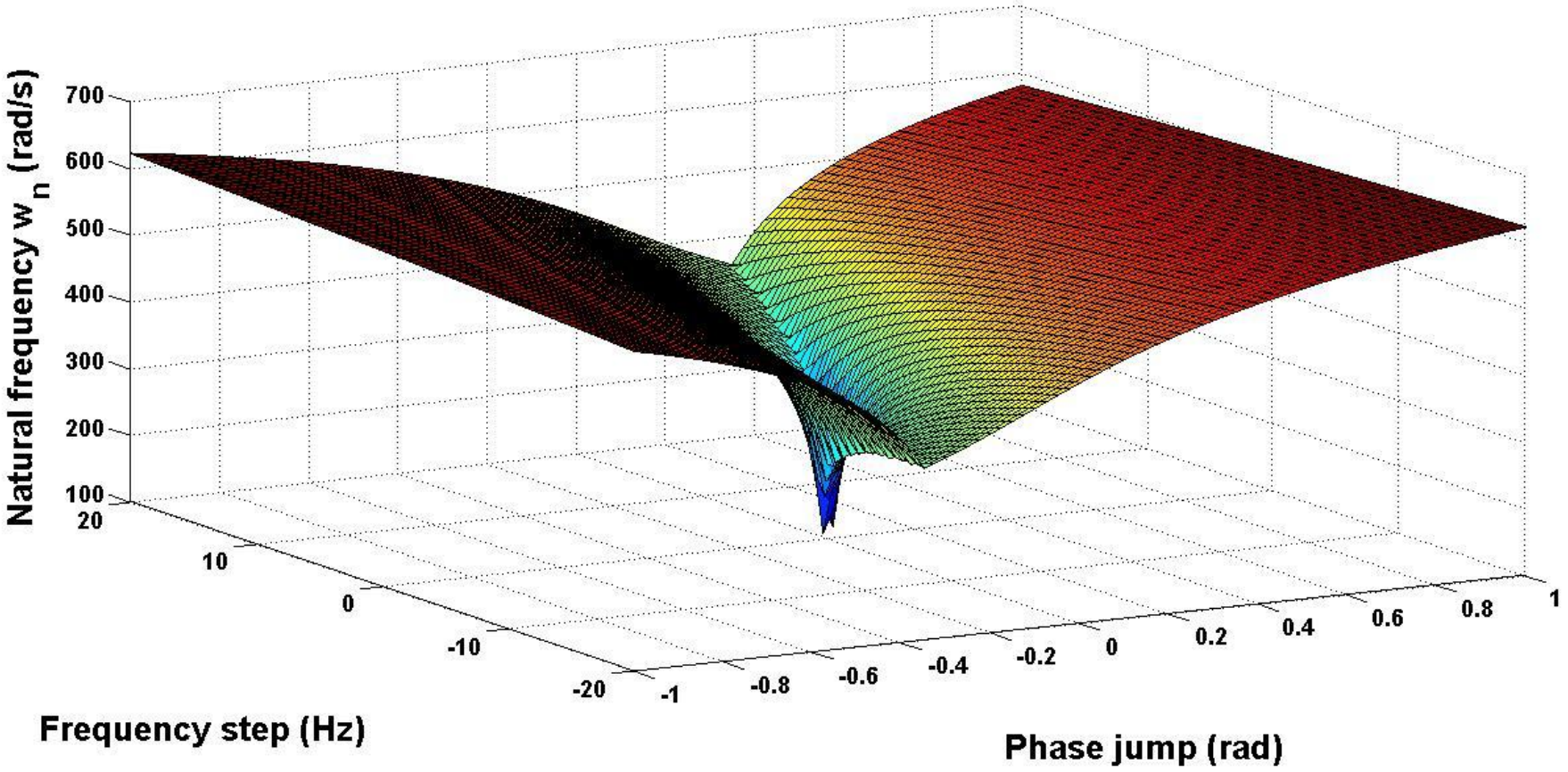


Proposed method

3D lookup table – optimized δ



3D lookup table – optimized ω_n



3D lookup table – optimized τ

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