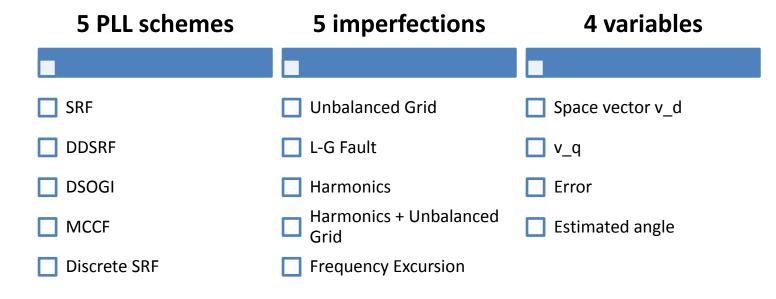
Recap

- SRF, DDSRF, DSOGI, MCCF, Discrete SRF
 - SRF: conventional PLL tracks changes in frequency and phase
 - DDSRF: attacks the issue of unbalanced grid
 - DSOGI, MCCF: deal with harmonics and unbalanced grid
- The above algorithms were studied from literature, mathematically analyzed and implemented using MATLAB Simulink

Algorithms

- SRF Stationary to synchronous reference frame
 - » Loop Filter, Integrator, Closed loop system
- DDSRF Decoupling network is the major improvement
 - » Enables tracking in unbalanced situation through decoupling of positive and negative sequence voltages
- <u>DSOGI</u> Second order generalized integrator type filter
 - » Filters out the fundamental component in the stationary reference frame
- MCCF Multiple Complex Coefficient Filters
 - » Requires two modules for eliminating every harmonic component
- <u>Discrete SRF</u> Discretized version of the SRF PLL
 - » Input is sampled, transfer functions in z-domain

- Formulating a common convention
 - All existing PLLs are modifications of the conventional SRF PLL
 - Different conventions are followed in literature
 - Single platform between different schemes requires a common convention
- Simulation of each scheme required an in-depth understanding since mathematical models had to be re-designed to suit to our convention
- Each scheme was modeled and tested individually and these models were clubbed into a single <u>self-consistent model</u> for comparison
- Complexity involved more than 600 comparisons!!



- Development of an applet (learning tool)
 - Parts
 - Initialization program
 - Simulink models
 - Intuitive program to plot
 - Demo
 - Importance of the applet
 - Excellent tool for learning <u>How</u>?
 - Easy to use
 - To <u>find out</u> which scheme tackles a particular issue better
 - Additions of other schemes (if required) can be easily done

Future work

- Design optimization aimed at achieving a faster dynamic performance
- Verification of results through practical setup

Thank you

Synchronous Reference Frame PLL (SRF)

Situations:

- 1. Frequency Excursion
- 2. L-G Fault
- 3. Harmonics
- 4. Unbalanced Grid
- 5. Harmonics + Unbalanced Grid

Other PLL scheme comparisons

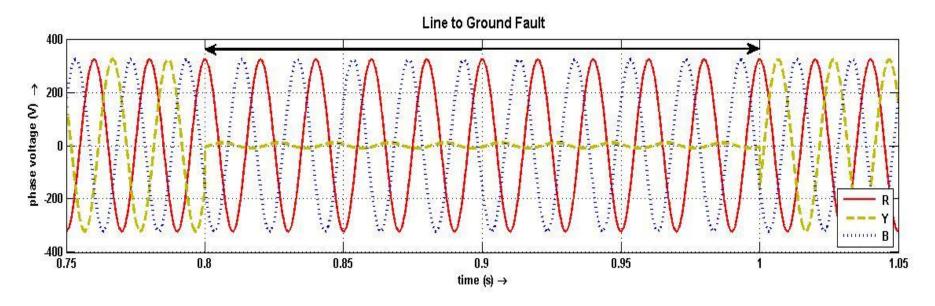
Situations:

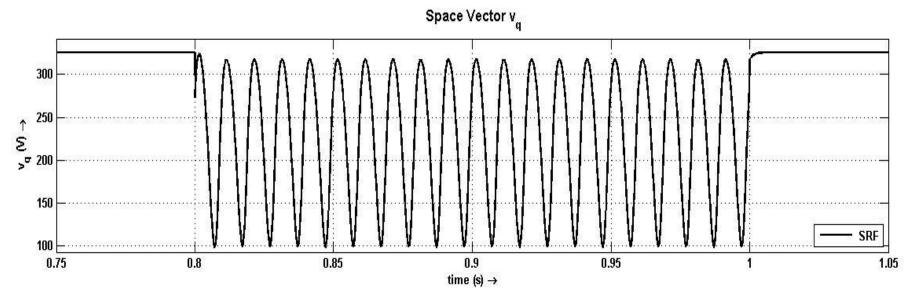
- 1. Frequency Excursion
- 2. L-G Fault
- 3. Harmonics
- 4. Unbalanced Grid
- 5. Harmonics + Unbalanced Grid

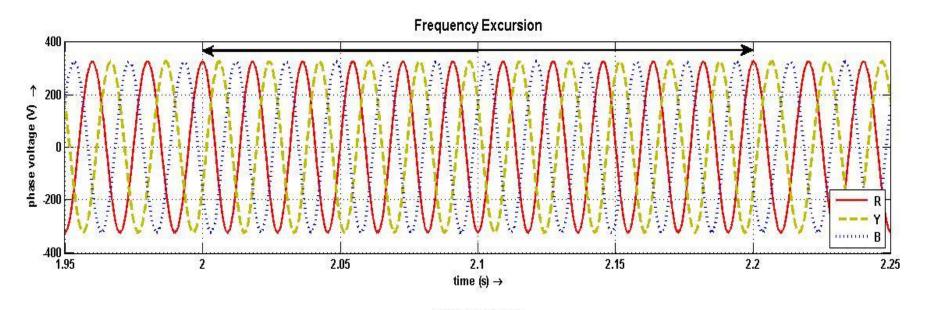
Discrete PLL

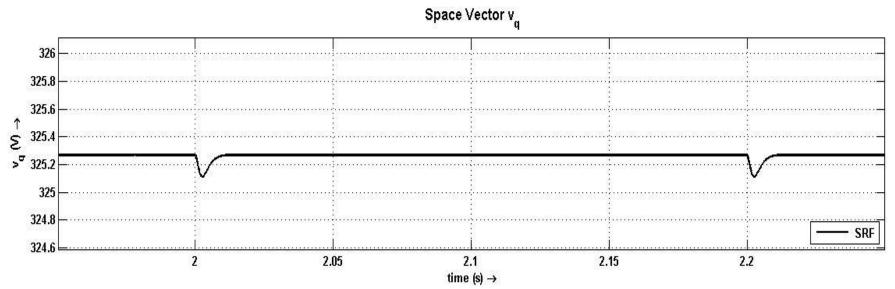
Situations:

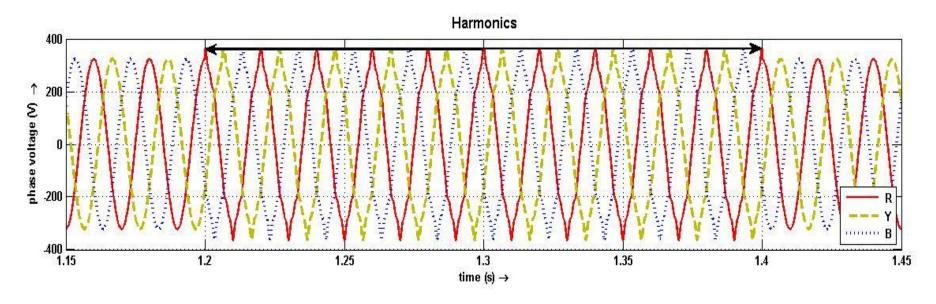
- 1. Frequency Excursion
- 2. L-G Fault
- 3. Harmonics
- 4. Unbalanced Grid
- 5. <u>Harmonics + Unbalanced Grid</u>

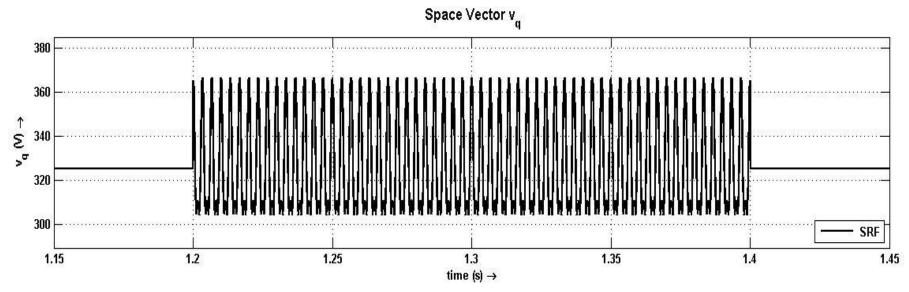


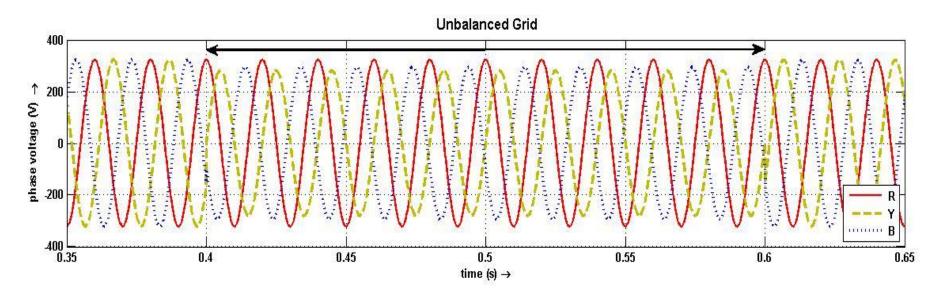


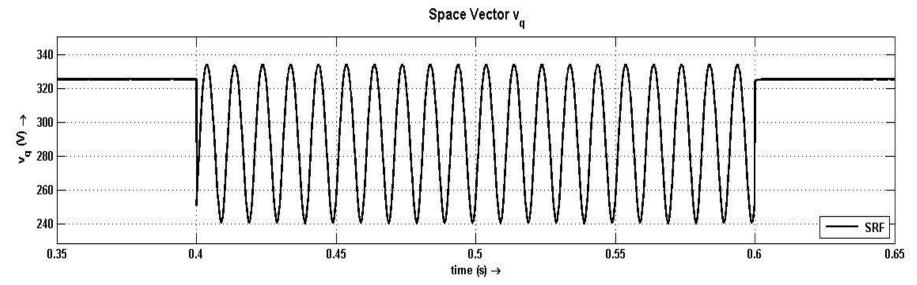


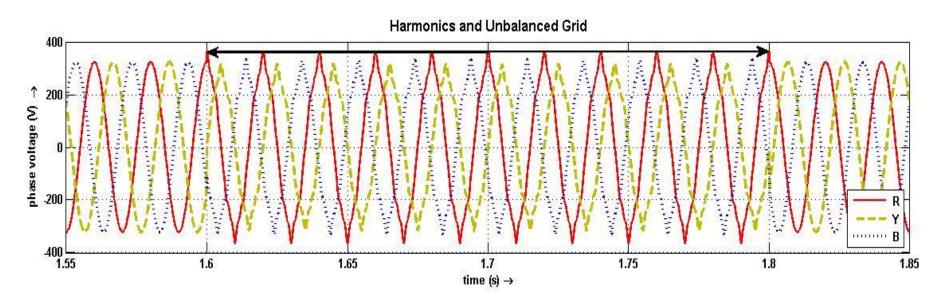


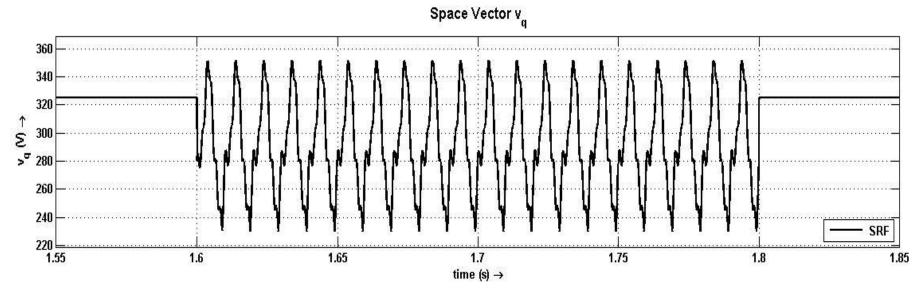


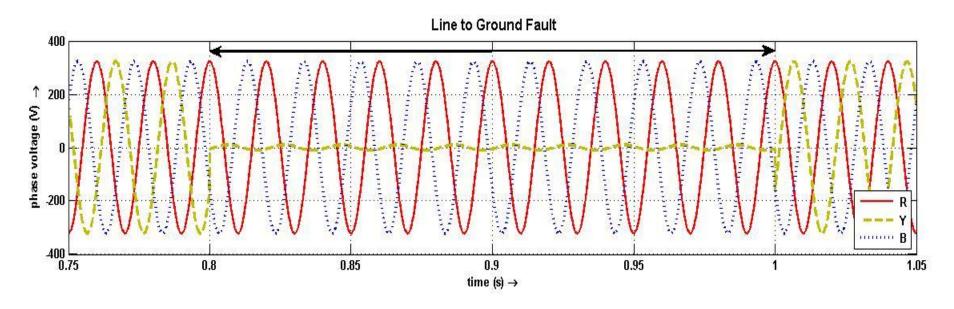


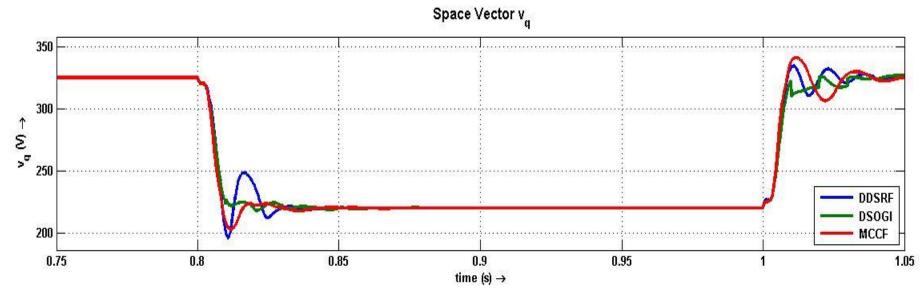


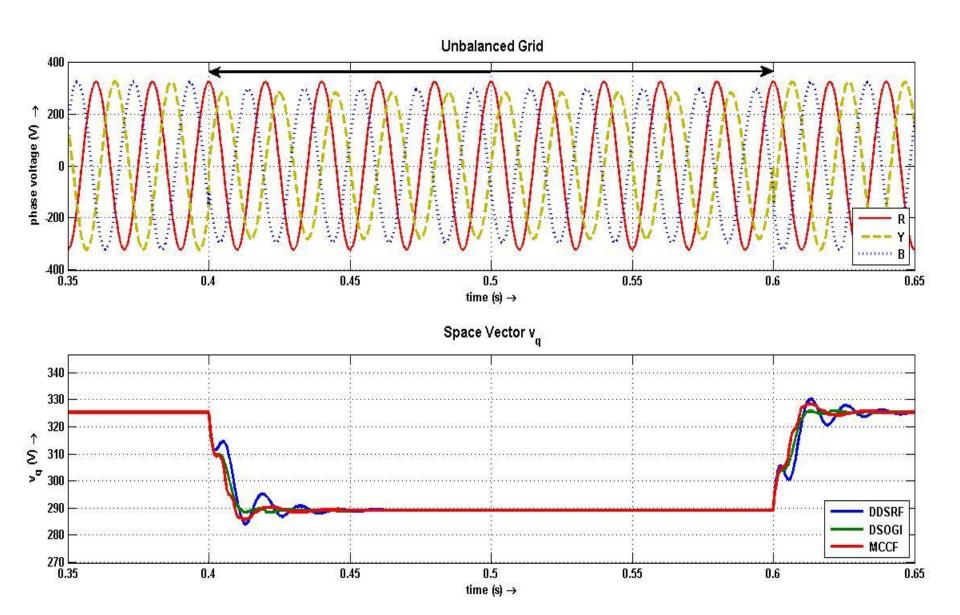








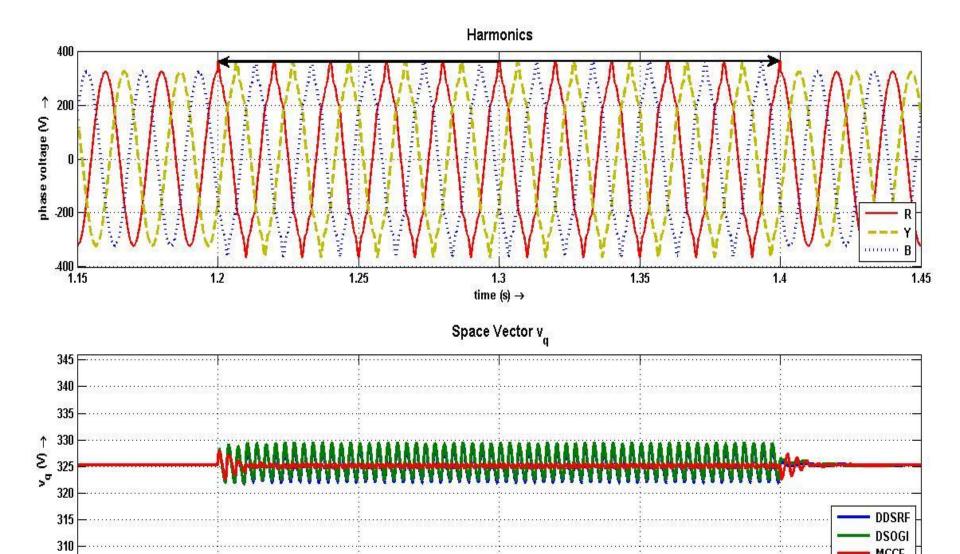




1.15

1.2

1.25

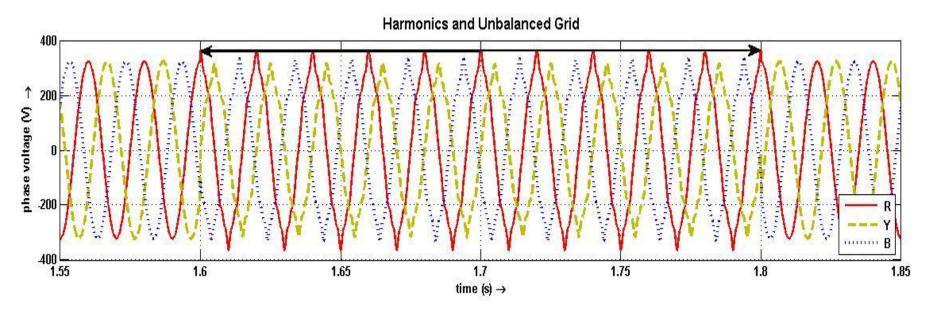


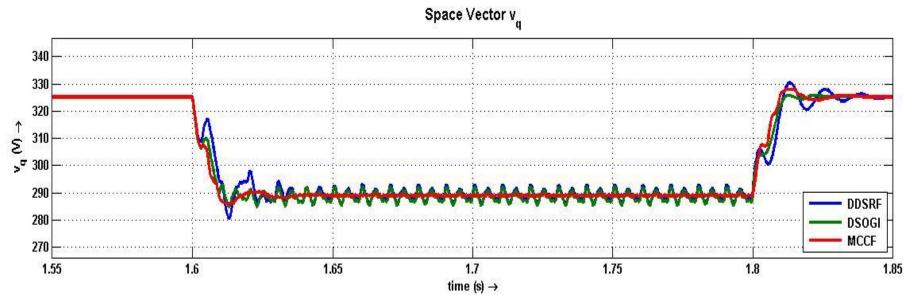
1.3

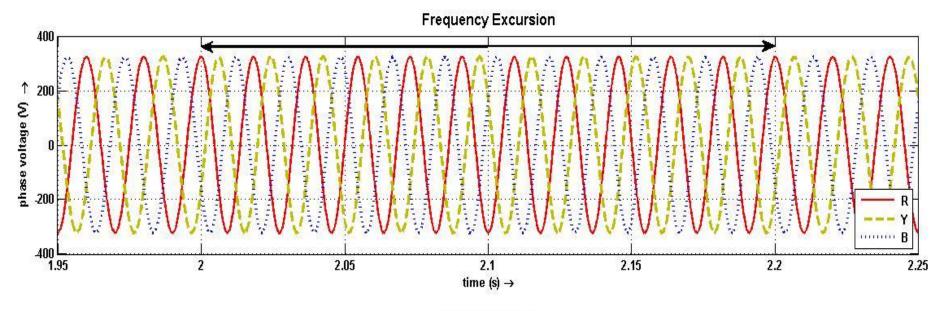
time (s) \rightarrow

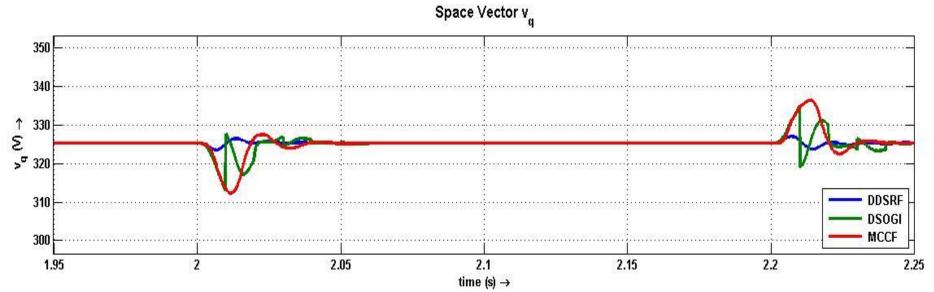
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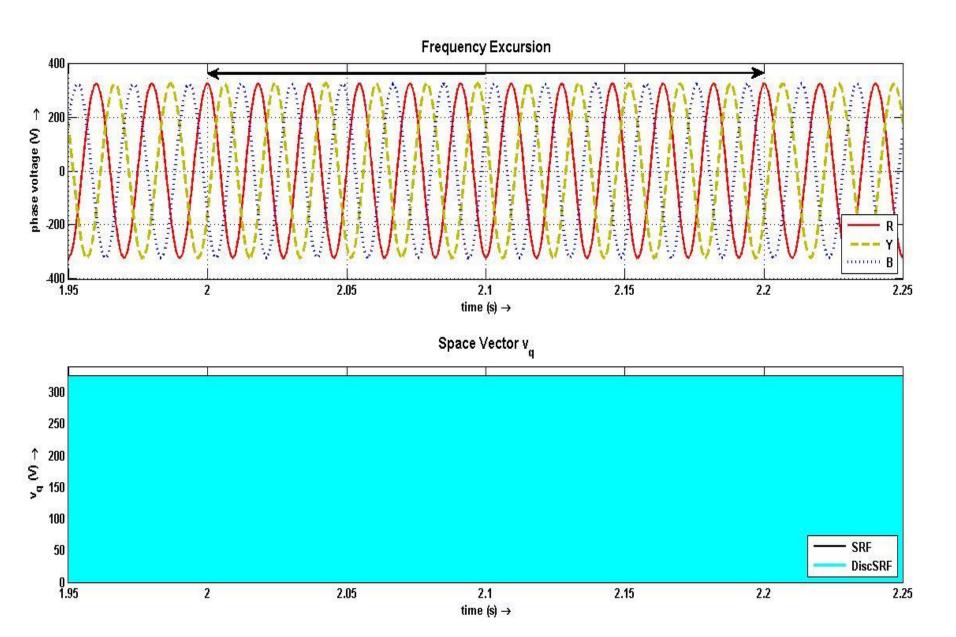
1.4

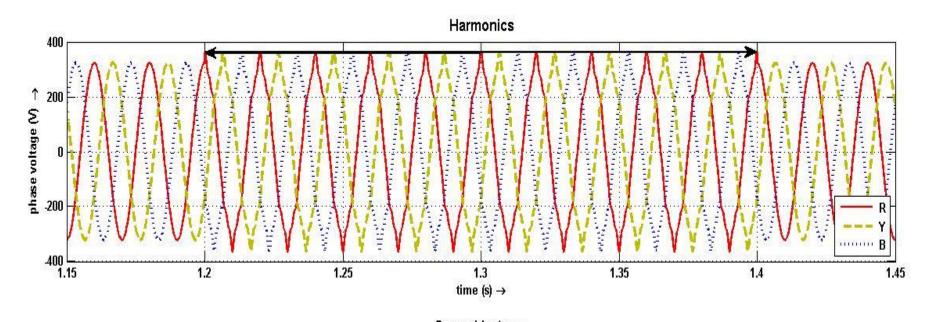


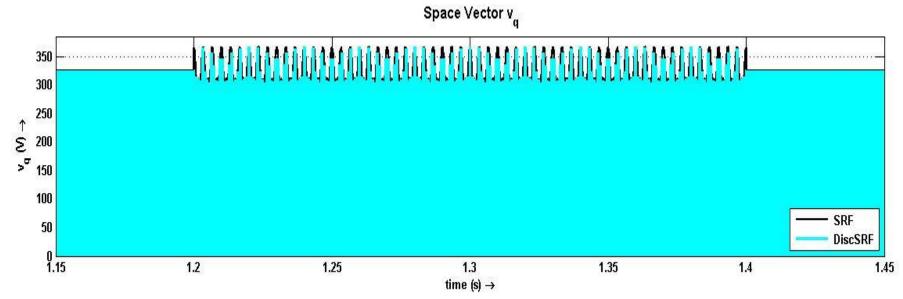


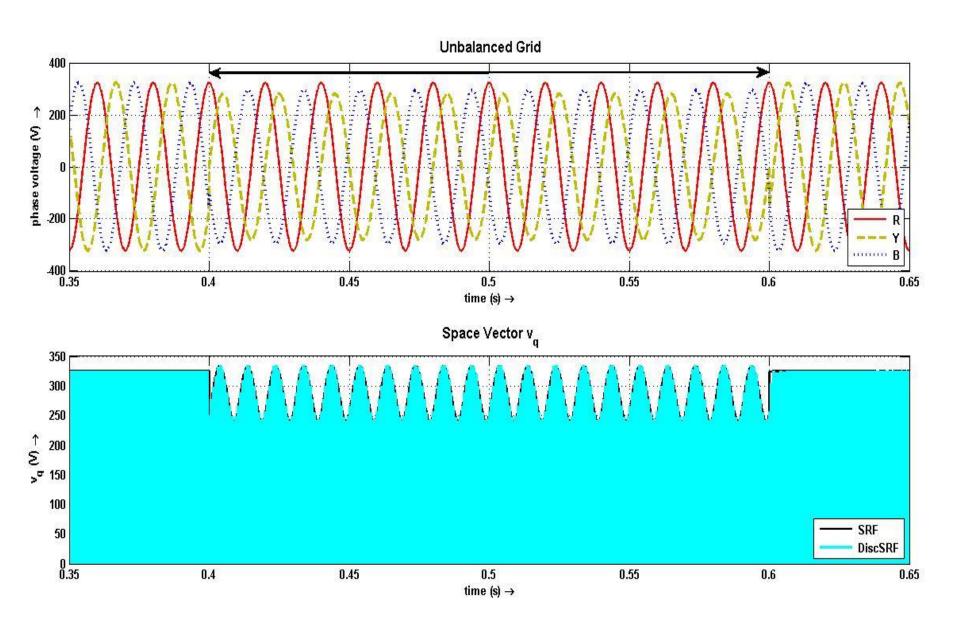


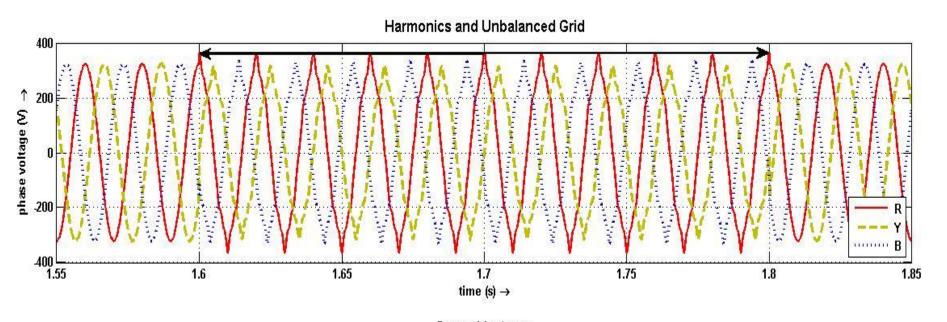


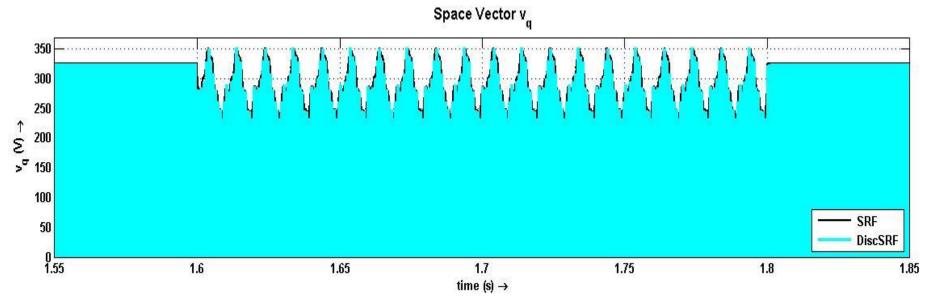


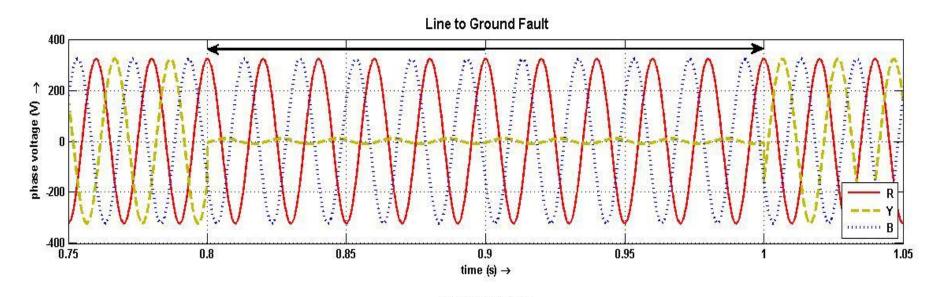


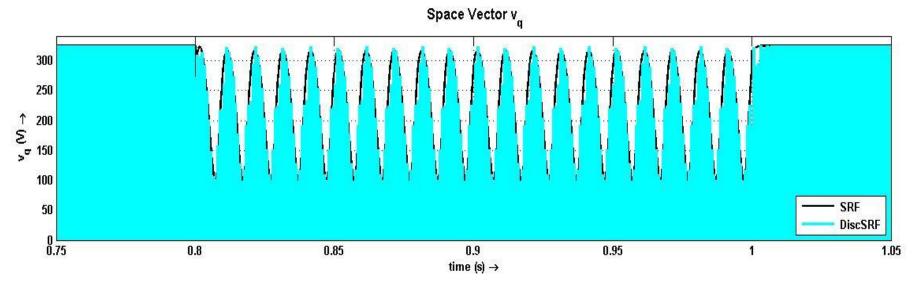


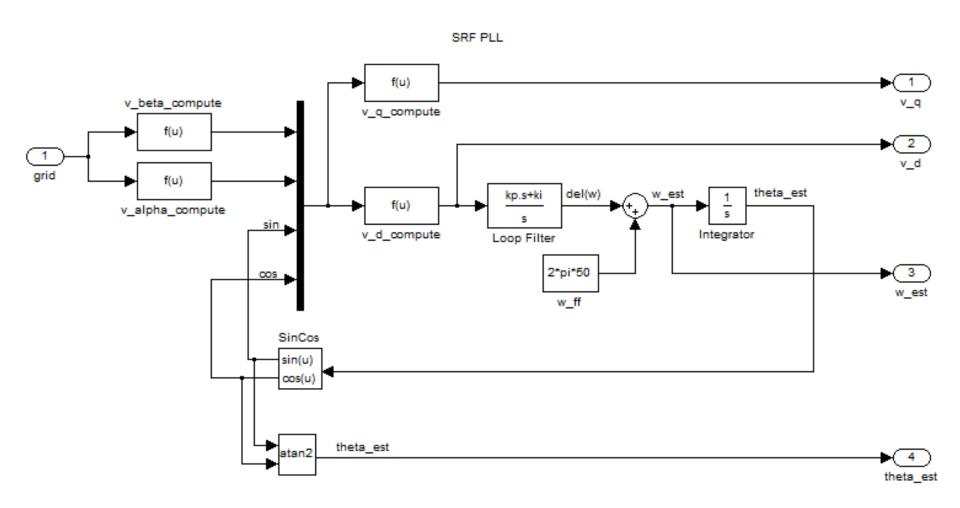


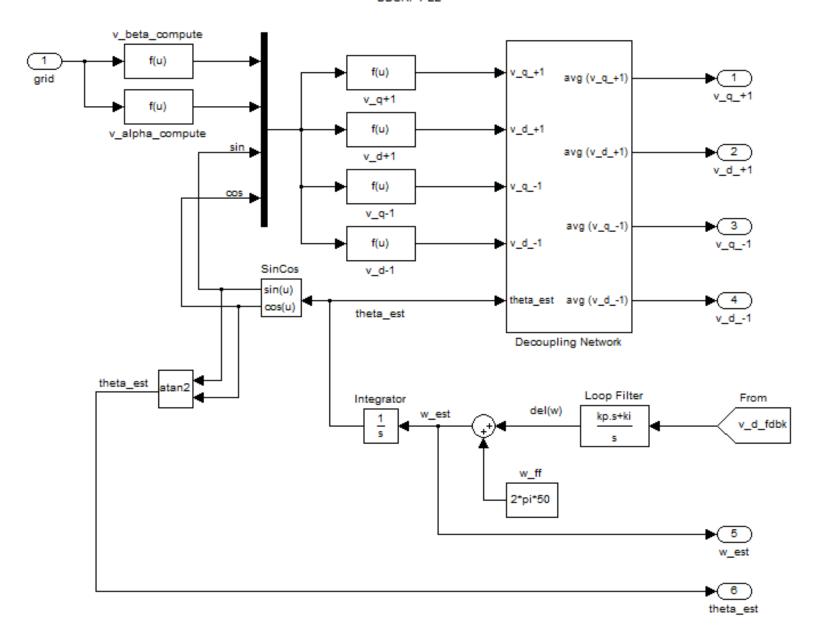






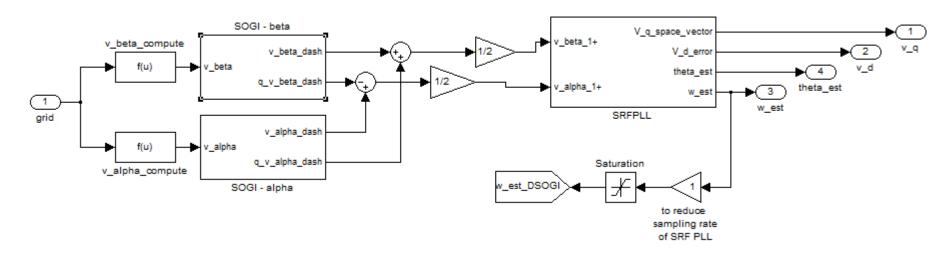


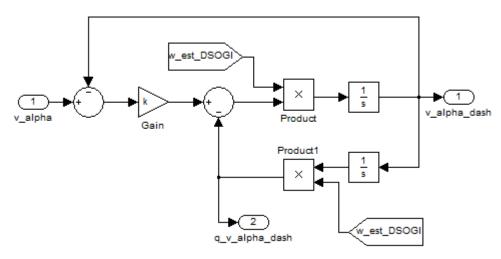




DSOGI PLL Back

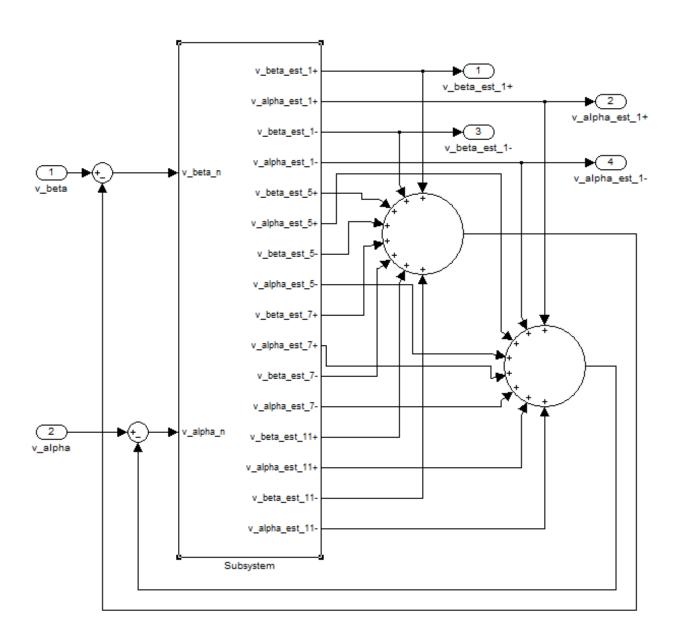
DSOGI PLL



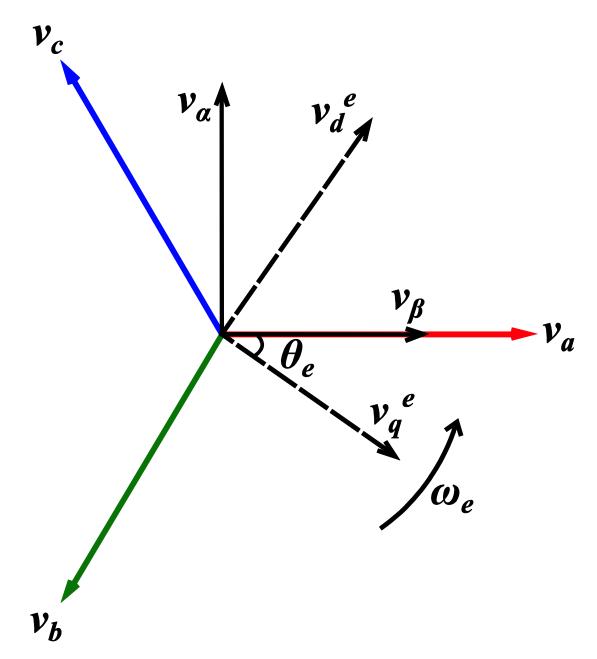


MCCF PLL

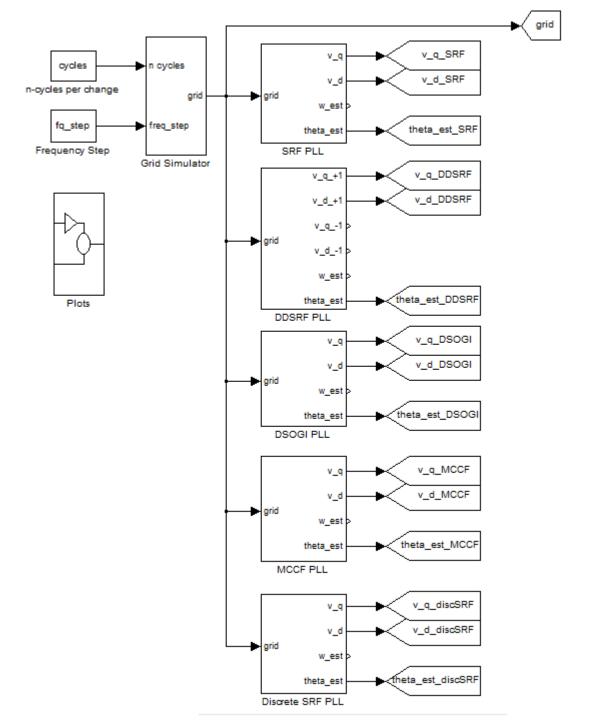
MCCF PLL V_q_space_vector v_beta_compute v_beta_est_1+ v_beta_1+ V_d_error f(u) v_beta theta_est v_alpha_est_1+ v_alpha_1+ theta_est w_est w_est SRFPLL v_beta_est_1v_alpha f(u) v_alpha_est_1v_alpha_compute Saturation MCCF module w_est_MCCF to reduce sampling rate of SRF PLL



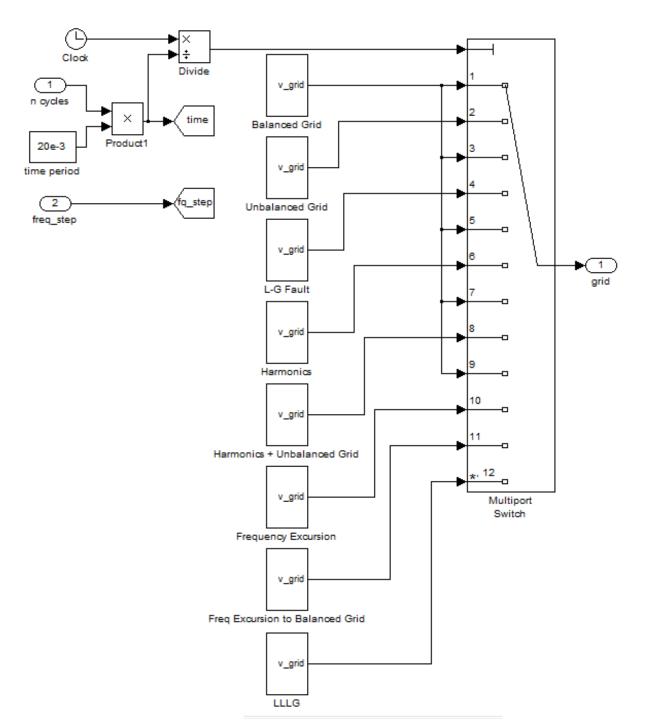
Discrete SRF PLL f(u) v_beta_compute v_q_compute f(u) grid f(u) Product del(w) theta_est kp.z+(ki*Ts-kp) Ts f(u) v_alpha_compute z-1 z-1 sin v_d_compute Gc(z) Integrator Pulse Generator 2*pi*50 cos . w_ff SinCos sin(u) cos(u) theta_est



Self-consistent model



Grid simulator



Back