Analytical Modeling of Semiconductor Losses in Matrix Converters

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***Abstract*— Analytical models for estimating semiconductor losses are commonly used for heatsink selection in the design process of power converters. While such models are established and widely known for different dc-dc converters, rectifiers and inverters, they have not been developed for matrix converters. Therefore, one has to resort to the use of numerical simulation for this purpose. Although numerical simulation is a straightforward approach as long as the power switching devices are properly modeled, it is typically time consuming and requires accurate physical models for the device. In this paper, an analytical approach to characterizing the semiconductor losses of the conventional matrix converter (CMC) and the indirect matrix converter (IMC) is presented. The analytical results are verified against the simulation results from a detailed numerical model under a wide variety of operating conditions.**

Keywords- conduction loss; conventional matrix converter (CMC); indirect matrix converter (IMC); simulation; switching loss;

I. INTRODUCTION

Since the introduction of high frequency synthesis approach for ac-ac power conversion proposed by Venturini in 1980 [1-3], significant research effort has been dedicated to the matrix converter due to its attractive features, such as high quality input and output waveforms and high power density [4-12]. The focus of much of the work has been mainly on topology, modulation, and commutation aspects, while definitive models for loss characterization have not been fully developed. Since the converter topology eliminates internal energy storage elements, the converter footprint is predominantly determined by the heat sink for the semiconductors. And in order to properly size the heat sink, estimation of the power loss/dissipation with acceptable accuracy is a key step.

Common practice of power loss estimation has been through the use of numerical time series simulation. Although the numerical simulation is a very straightforward procedure as long as the power switching devices are properly modeled, it is typically time consuming and this is particularly true if various different operating conditions need to consider. Furthermore, the loss predictions are a strong function of the accuracy of the physical models available for simulation, while most widely available semiconductor loss models are behavioral. It is known that the fidelity of loss simulations may vary by quite a wide factor in repeating actual thermal performance [13]. In contrast, the analytical approach to predicting power losses is a much more favored alternative due to its ability of fast profiling, based on readily available behavioral models for semiconductors.

Estimation of conduction loss and switching loss for voltage source and current source converters have been established [14-18]. In this paper, an analytical approach to power loss calculation for conventional matrix converter (CMC) and the indirect matrix converter (IMC) are explored. This paper is organized as follows. In Section II, the simplified loss model of the power devices, namely insulated gate bipolar transistors (IGBTs) and diodes, are reviewed. In Section III, the conduction loss and switching loss are derived for the CMC topology. The conduction loss and switching loss are derived for the IMC topology in Section IV. In Section V, analytical results are verified against the simulation results for CMC and IMC topology followed by a comparison. The contributions of the paper are summarized in the concluding Section VI.

II. SEMICONDUCTOR LOSS MODEL

Typically, three operating modes can be categorized for the semiconductor power devices in a power converter: 'on', 'off' and 'transition' modes. The power loss when the *device* is off is usually negligible compared to the 'on' mode and 'transition' modes, in which the associated losses are commonly denoted as conduction and switching losses, respectively. The conduction loss can be modeled by power dissipation caused by the voltage drop across the device and the current through the device. The voltage drop is approximated by the linear dependence on the current.

$$v_{CE}(i_C) = V_{CE0} + r_{CE} i_C$$
$$v_F(i_F) = V_{F0} + r_F i_F \quad (1)$$

where v_{CE} and v_F are the voltage drop across the IGBT and the diode for current i_C and i_F, respectively. r_{CE} and r_F are the incremental resistance of the IGBT and the diode. V_{CE0} and V_{F0} are the forward voltages when the current is zero (or quite small) [18].

The switching loss is characterized by the switching loss energy associated with each switching event. The switching energy is generally assumed proportional to the blocking voltage and the conducting current at the instant of switching event [18].

$$E_{sw} = E_{swR} \frac{v}{V_R} \frac{i}{I_R} \quad (2)$$

where E_{swR} is the switching energy at the reference voltage V_R and reference current I_R, which are typically the test conditions of in device datasheets; and *v* and *i* are the actual operating voltage and current in the particular application.

For IGBT, there are switching losses, E_{on} and E_{off}, associated with both turn-on and turn-off processes. While for diodes, the switching loss is typically cause by the reverse recovery (E_{rr}) mechanism, which only occurs during turn-off of a diode.

III. CMC Loss Calculation

As shown in Fig. 1, the topology of the CMC is represented by three single-pole-triple-throw (SPTT) switches. Each bidirectional throw S_{mn} (m, n = 1,2,3) is realized by two IGBTs and two diodes.

The input voltages and output currents are given by

$$v_{ik}(t) = V_i \cos\left(\alpha_i(t) - (k-1)\frac{2\pi}{3}\right)$$
$$i_{ok}(t) = I_o \cos\left(\beta_o(t) - (k-1)\frac{2\pi}{3}\right) \quad (3)$$

where k = 1, 2, 3; The phase angle of the input voltage and output currents can be expressed as $\alpha_i(t) = \omega_i t + \alpha_{i0}$ and $\beta_o(t) = \omega_o t + \beta_{o0}$, with ω_i and ω_o being the fundamental frequency of the input voltage and output current, respectively.

A. Conduction Losses

At any instant, the output currents flow through one IGBT and one diode. Based on the balanced three phase output currents given in (3), only one SPTT is considered and the total conduction loss is calculated by multiplying three times. Only a quarter of the period is needed to integrate due to the output current waveform symmetry.

$$P_{c\_CMC} = 3\frac{2}{\pi}\int_0^{\pi/2}\left[v_{CE}(i_{o1}) + v_F(i_{o1})\right] i_{o1} d\beta_o \quad (4)$$

Substituting the current i_{o1} in (3) and the diode/IGBT characteristics in (1) into (4) results in the closed-form expression for the conduction loss of the CMC

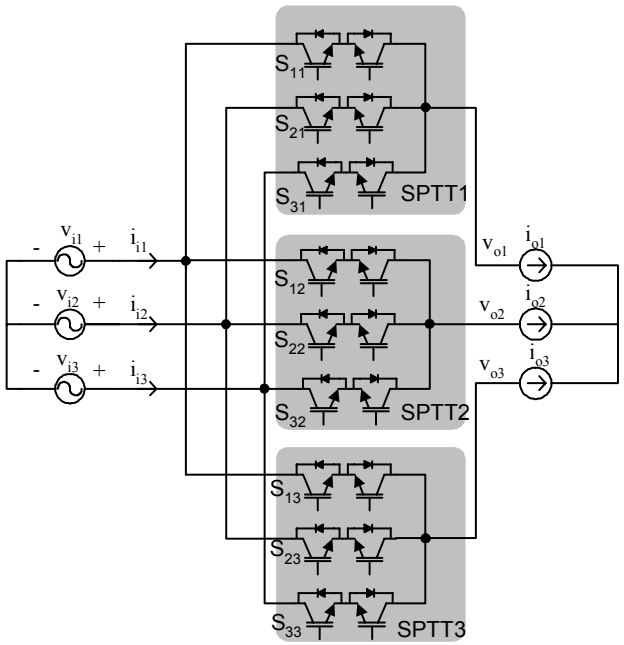

Fig. 1 Simplified schematic of the conventional matrix converter topology represented by three SPTT switches

$$P_{c\_CMC} = \frac{6}{\pi}(V_{CE0} + V_{F0}) I_o + \frac{3}{2} I_o^2 (r_{CE} + r_F) \quad (5)$$

It can be observed that the conduction loss is only determined by the peak value of the output current and is not affected by the operating conditions such as modulation index or power factor.

B. Switching Losses

Since the switching loss depends on the alternating blocking voltage of each throw, the commutation sequence will affect the switching loss. In this analytical development, a typical double-sided switching pattern is assumed [19]. Due to the symmetry of the balanced three-phase systems at input and output terminals, only one SPTT switch is considered. In Fig. 2, the switching functions h_{11}, h_{21} and h_{31} for throws S_{11}, S_{21} and S_{31} of switch SPTT1 are illustrated. There are four commutation events in one switching cycle T_s, which is assumed constant. The commutation voltage associated with each commutation event is labeled in Fig. 2.

For the topology shown in Fig. 1, during the commutation between throws, neither overlap nor dead-time is allowed since overlap means short circuit to the input voltages and dead-time means open circuit to the output currents. One way to work around this is to make the commutation happen in several steps [20]. The current-based four-step commutation scheme is assume in deriving the analytical expression for the switching losses although the methodology adopted here can be extended to other schemes, such as voltage-based commutation. The current-based four-step commutation scheme is explained here for completeness.

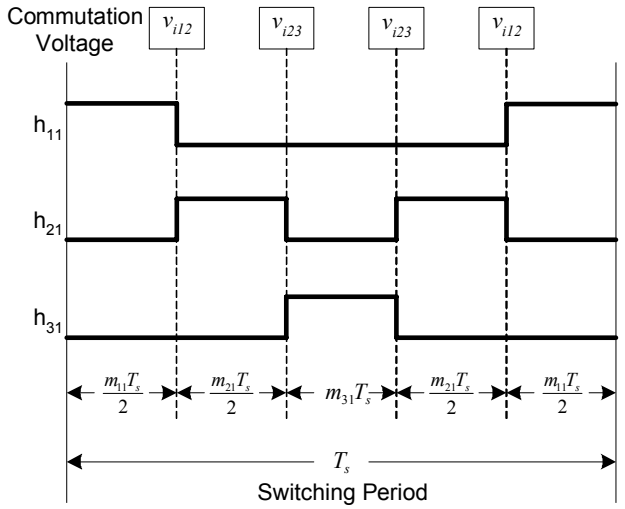

Fig. 2 Illustration of switching functions for throws S_{11}, S_{21}, and S_{31} with double-sided switching pattern.

The explanation proceeds with the example of commutating current i_{o1} from throw S_{11} to S_{21}. As illustrated in Fig. 3, if the current i_{o1} is positive, the current initially flows through the IGBT T_{11_1} and Diode D_{11_2}. The IGBT T_{11_1} is first turned off and no energy loss is involved since T_{11_1} is previously not carrying any current. Then T_{21_1} is turned on. If the commutation voltage v_{12} is negative, there will be turn-on loss with T_{21_1} and reverse recovery loss with D_{11_2}. Otherwise, nothing will happen until the next instant when T_{11_1} is turned off. When T_{11_1} is turned off, there will be turn-off energy loss with T_{11_1}. The final step is to turn on T_{21_2}. Thus, the exact instant when actual commutation happens depends on the polarity of the commutation voltage. As indicated in Fig. 3, for positive v_{12} the commutation occurs when T_{21_1} is switched on. For native v_{12}, the commutation occurs when T_{11_1} is switched off.

Similar analysis can be carried out for the case of negative i_{o1}. Furthermore, the commutation process from S_{21} to S_{11} has been carried out to complete one commutation cycle between S_{11} and S_{21}. The switching energy losses for the commutation between S_{11} and S_{21} for different pole current and throw voltage polarities are summarized in TABLE I.

TABLE I. SWITCHING ENERGY LOSSES FOR THE COMMUTATION BETWEEN S_{11} AND S_{21}

	$I_{o1}>0$		$I_{o1}<0$	
	$S_{11}\rightarrow S_{21}$	$S_{21}\rightarrow S_{11}$	$S_{11}\rightarrow S_{21}$	$S_{21}\rightarrow S_{11}$
$v_{12}>0$	$E_{off\_T11\_1}$	$E_{on\_T11\_1}$ $E_{rr\_D21\_2}$	$E_{on\_T21\_2}$ $E_{rr\_D11\_1}$	$E_{off\_T21\_2}$
$v_{12}<0$	$E_{on\_T21\_1}$ $E_{rr\_D11\_2}$	$E_{off\_T21\_1}$	$E_{off\_T11\_2}$	$E_{on\_T11\_2}$ $E_{rr\_D21\_1}$

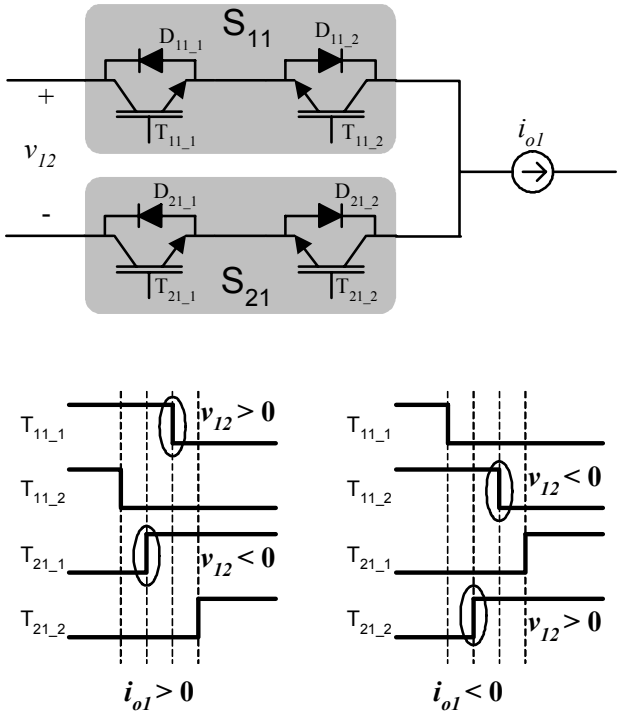

Fig. 3 Circuit schematic and actual switching function waveforms illustrating four step commutation from S_{11} to S_{21}

The observations from the table can be generalized that, for the two commutation events comprising a complete switching cycle, there are (i) one turn-on loss transient, and (ii) one turn-off loss transient for the IGBT; and (iii) one recovery energy loss for the diode. A similar table is possible for the commutation of between S_{21} and S_{31}, difference being the commutation voltage v_{23} instead of v_{12}. Thus, the total switching energy loss of one SPTT in one switching cycle can be calculated by

$$E_{sw/Ts} = \left(E_{on\_T} + E_{off\_T} + E_{rr\_D}\right)\frac{\left(|v_{12}|+|v_{23}|\right)|i_{o1}|}{V_R I_R} \qquad (6)$$

where E_{on_T}, E_{off_T}, E_{rr_D} are the turn-on and turn off energy of the IGBT and the reverse recovery energy of the diode per switching event, respectively, with the loss reference conditions being V_R and I_R.

If the switching frequency is much higher than the fundamental frequency of input voltage and output current, the average switching power loss over time interval T can be estimated using the integral

$$P_{sw/T} = f_s\left(\frac{E_{on\_T} + E_{off\_T} + E_{rr\_D}}{V_R I_R}\right)\frac{1}{T}\int_0^T\left[\left(|v_{i12}|+|v_{i23}|\right)|i_{o1}|\right]dt \qquad (7)$$

The fundamental frequency of the input is typically different from the output frequency. It follows that the integration interval must be sufficiently long to overcome possible low "beating" frequency of the integrand in (7). So, any attempt to characterize the loss of the matrix converter via simulation will be challenging unless particular input-output frequency ratio has been chosen, which does not result in extreme low "beating" frequency. Notice that $|v_{12}|$, $|v_{23}|$ and $|i_{o1}|$ can be expanded to Fourier

series and the average loss coming from harmonics can be neglected if the input and output frequency ratio is not integer, which is generally true for variable frequency drive applications. Using this process the total switching loss of the converter can be determined to be

$$P_{sw\_CMC} = \frac{24\sqrt{3}}{\pi^2} f_s \left(E_{on\_T} + E_{off\_T} + E_{rr\_D}\right) \frac{V_i I_o}{V_R I_R} \tag{8}$$

IV. IMC Loss Calculation

As shown in Fig. 4, the IMC (also called the dual bridge matrix converter) is composed of two bridges, which are treated as the current source bridge (CSB) at the input terminals and the voltage source bridge (VSB) at the output terminals. One important advantage with this topology is the simple commutation of the bidirectional switches as identified in [21]. By utilizing the zero link current created by the VSB, the CSB can commutate without overlap-time or dead-time. In this discussion, the CSB is modulated in such way that one of the three input phases a, b or c with maximum reference current amplitude is connected to the dc link for the entire switching period and the return dc link current is split between the other two phases [22]. The VSB modulation is very similar to the ordinary VSI modulation except that the amplitude of the modulation functions of its throws appropriately modified to result in sinusoidal input currents and output voltages [22]. The input voltages and output currents still follow the definitions described in (3).

A. Conduction Losses

It is relatively easy to estimate the conduction loss of the CSB since the link current always flows through two IGBTs and two diodes in the CSB. Noticing that the link current i_p is discontinuous due to the VSB switching as illustrated in Fig. 5, we may first calculate the average conduction loss of the CSB over one switching period as

$$\begin{aligned} P_{c\_avg/Ts} &= 2\frac{1}{T_s}\left[\int_{Ts}\left(V_{CE0}+V_{F0}\right) i_p dt + \int_{Ts}\left(r_{CE}+r_F\right) i_p^2 dt\right] \\ &= 2\left(V_{CE0}+V_{F0}\right) i_{p\_avg/Ts} + 2\left(r_{CE}+r_F\right) i_{p\_rms/Ts}^2 \end{aligned} \tag{9}$$

in terms of average and rms dc link currents over one switching period, which can be derived for $0 < \alpha_o(t) < \pi/3$

$$\begin{aligned} i_{p\_avg/Ts} &= \frac{3}{4} M(t) I_o \cos(\phi_o); \\ i_{p\_rms/Ts}^2 &= \frac{3M(t)I_o^2}{4}\left[\cos\left(\alpha_o(t)+\frac{\pi}{3}\right)+\frac{1}{2}\sin\left(3\alpha_o(t)+2\phi_o\right)\right] \end{aligned} \tag{10}$$

where M(t) is the the amplitude of the modulating functions of the VSB expressed as m_1, m_2, and m_3 which defined by

$$m_k = \frac{1+M(t)\cos\left(\alpha_o(t)-(k-1)2\pi/3\right)}{2} \tag{11}$$

where $\alpha_o(t) = \omega_o t + \alpha_{o0}$, $k \in \{1,2,3\}$. M(t) is the modulation function amplitude, which is time varying at frequency of $6\omega_i$ to synthesize the sinusoidal input current. The detailed derivation of (10) is found in Appendix A.

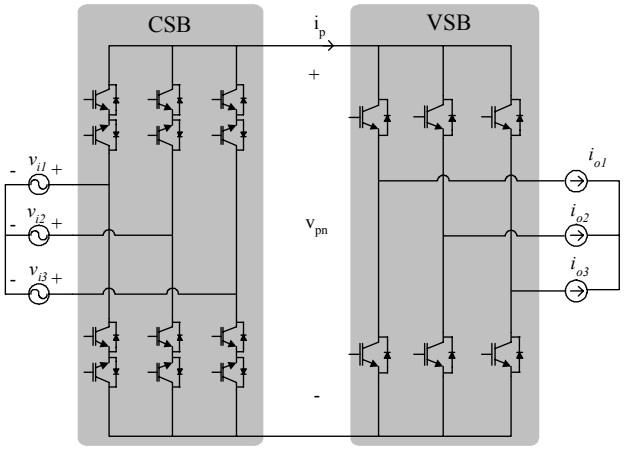

Fig. 4 Simplified schematic of the IMC topology using IGBTs and diodes.

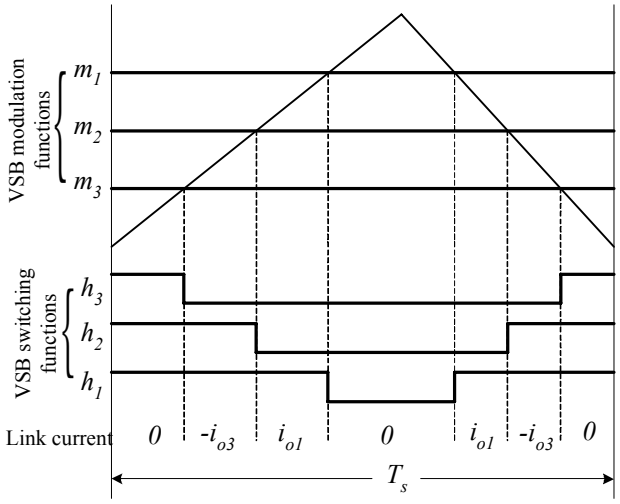

Fig. 5 Carrier based modulation for the VSB. $m_{1,2,3}$ are modulation functions of the upper throws in the VSB.

Combining (9), (10) and (11), the average conduction loss of the CSB may be determined as

$$P_{c\_CSB} = \frac{9}{2\pi}\left(V_{CE0}+V_{F0}\right) M_o I_o \cos\phi_o + \frac{3\sqrt{3}}{2\pi^2}\left(r_{CE}+r_F\right) M_o I_o^2 \left(1+4\cos^2\phi_o\right) \tag{12}$$

To calculate the conduction loss of the VSB, the top IGBT and diode in VSB phase-leg "1" is considered. The conduction loss of the top IGBT can be written as

$$P_{c\_Tp} = \frac{1}{T}\int_0^T i_{o1} v_{CE}\left(i_{o1}\right) \frac{\left[sign\left(i_{o1}\right)+1\right]}{2}\frac{\left[m_{o1}(t)+1\right]}{2} dt \tag{13}$$

The conduction loss of the top diode in the same phase-leg is

$$P_{c\_Dp} = \frac{1}{T}\int_0^T -i_{o1} v_F\left(-i_{o1}\right) \frac{\left[sign\left(-i_{o1}\right)+1\right]}{2}\frac{\left[m_{o1}(t)+1\right]}{2} dt \tag{14}$$

The conduction loss of the VSB can be calculated by

$$P_{c\_VSB} = 6\left[\begin{aligned} &\frac{\left(V_{CE0}+V_{F0}\right) I_o}{2\pi} + \frac{\left(r_{CE}+r_F\right) I_o^2}{8} + \\ &\frac{3}{8\pi}\left(V_{CE0}-V_{F0}\right) I_o M_o \cos\phi_o + \frac{\left(r_{CE}-r_F\right) I_o^2}{\pi^2} M_o \cos\phi_o \end{aligned}\right] \tag{15}$$

The expression (15) says the conduction loss of the VSB is affected by the modulation index and the output power factor angle due to the different characteristics of the IGBT and the diode, which is reasonable because the modulation index and the power factor angle will affect the relative duty ratios of the IGBTs and the diodes.

B. Switching Losses

Since the CSB only commutates only when the link current i_p is zero, there is no switching loss in the CSB. As shown in Fig. 5, there are six commutation events associated with the VSB in each switching cycle T_s. Due to the three phase symmetry of the output current, the loss in one phase leg alone needs to be determined and the total switching loss is estimated to be three times as much. During each switching period, the VSB commutation voltage (link voltage) will take one of the values of the two different input line-line voltages shown in bold in Fig. 6.

Using this formulation, the switching loss of the VSB can be expressed as

$$P_{sw\_VSB} = 3f_s \frac{1}{\theta}\int_0^{\theta}\left(E_{on}+E_{off}+E_{rr}\right)\frac{\left(v_{pn1}+v_{pn2}\right)i_{o1}}{V_R I_R}\frac{1+sign\left(i_{o1}\right)}{2}d\omega_o t \quad (16)$$

Evaluating the integral, (16) can be simplified to

$$P_{sw\_VSB} = \frac{27}{\pi^2} f_s\left(E_{on}+E_{off}+E_{rr}\right)\frac{V_i}{V_R}\frac{I_o}{I_R}\cos\left(\phi_i\right) \quad (17)$$

It can be seen the IMC switching loss varies with the input power factor. The switching losses peak at unity input power factor.

V. Simulation Verification and Discussion

To verify the analytical solutions derived in proceeding sections, the detail numerical model has been built using Matlab SimuLink™. The key parameters used in simulation are listed in TABLE II. The device parameters are based on the datasheet of SEMIKRON IGBT module SKM 75GB123D.

Selected quantities of the current and voltage waveforms for CMC and IMC obtained from the simulations are illustrated in Fig. 7 and Fig. 8 respectively.

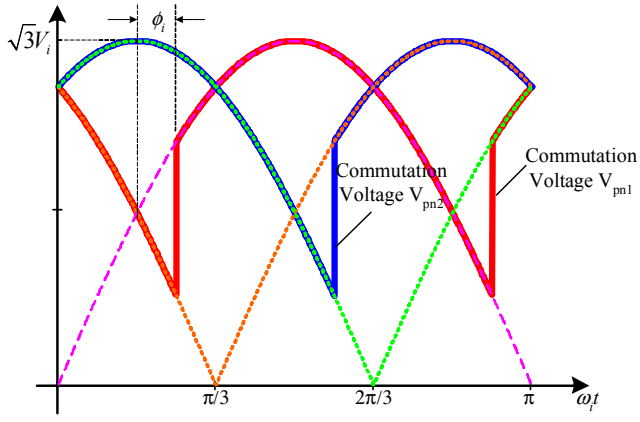

Fig. 6 Commutation voltage of the VSB with input power factor of ϕ_i

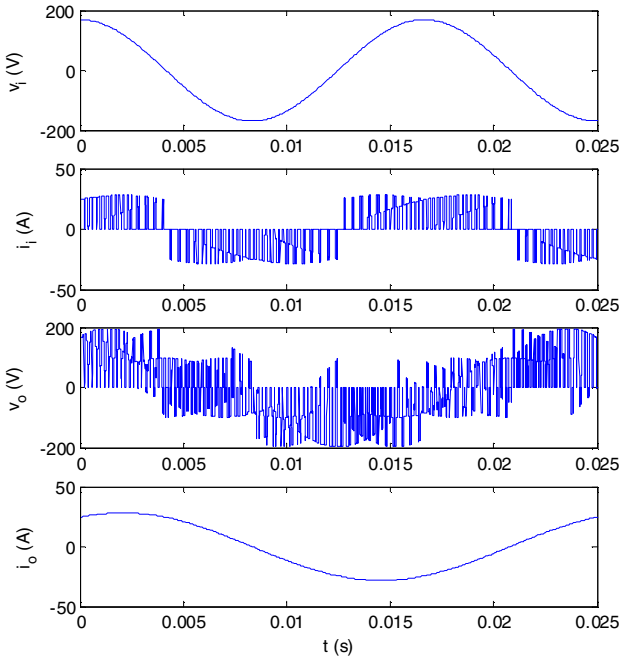

Fig. 7 Simulation waveforms of CMC: from top to bottom are input voltage v_i, input current i_i, output voltage (phase-to-load-neutral) v_o and output current i_o. Switching frequency of 3 kHz is chosen to show the waveforms with legible resolution.

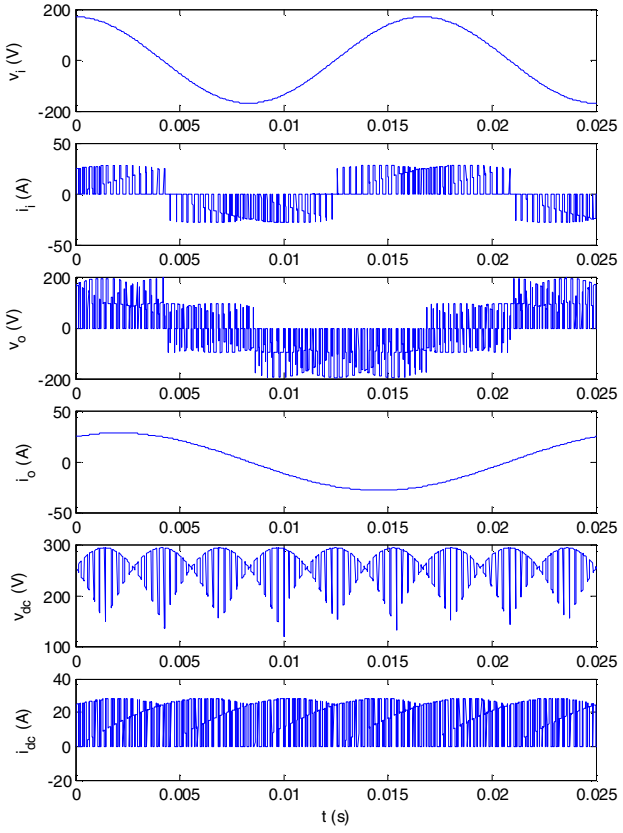

Fig. 8 Simulation waveforms of IMC: from top to bottom are input voltage v_i, input current i_i, output voltage (phase-to-load-neutral) v_o, output current i_o, link voltage v_{dc}, and link current i_{dc}. Switching frequency of 3 kHz is chosen to show the waveforms with legible resolution.

TABLE II. SWITCHING ENERGY LOSSES FOR THE COMMUTATION BETWEEN S_{11} AND S_{21}

Reference conditions	V_R (V)	600	I_R (A)	50
IGBT	V_{CE0} (V)	1.6	E_{on_T} (mJ)	8
	r_{CE} (mΩ)	30	E_{off_T} (mJ)	5
Diode	V_{F0} (V)	1.2	E_{rr_D} (mJ)	2.5
	r_F (mΩ)	18		
Input (l-n)	V_i (V_{rms})	120	ω_i (rad/s)	$2\pi\times60$
Output	I_o (A_{rms})	20	ω_o(rad/s)	$2\pi\times40$
Switching frequency	f_s (kHz)	10		

The semiconductor losses of IMC and CMC are plotted in Fig. 9 as functions of the modulation index. The per-unitized quantities are used to provide the common basis for comparison between the two different topologies. In the figure, the thin solid line, dashed line, dotted line and dash-dotted line are plots of analytical solution of the IMC losses with different input/output power factor angles. The markers on those lines are plots of the simulation results under the corresponding operation condition. The thick solid line and the markers are analytical and simulated results of the CMC losses, which are not affected by any of the operating conditions. The tight match between the analytical solution and simulation results validates the effectiveness of analytical approach developed in Section III and IV.

It can be observed from Fig. 9 at low modulation indices, the IMC has lower losses than CMC. Of course the break point relates to the different operating conditions of the IMC as indicated in the figure. For IMC, among the four different operating conditions, the losses with the ϕ_i = 0 and ϕ_o = 0 are maximum.

To better illustrate the relation, a separate 3-D plot of the IMC losses as function of the input/output power factor angle is presented in Fig. 10 using the analytical solution. It can be clearly seen the IMC losses peak at the operating point of ϕ_i, ϕ_o = 0.

In Fig. 9, all the plots are computed at the same switching frequency of 10 kHz. For different switching frequencies, the power losses of IMC and CMC are plotted in Fig. 11 to show the differences in dependency to switching frequency variations. In this comparison, the IMC power losses are plotted for different modulation indices with ϕ_i, ϕ_o = 0. It is observed that for high modulation indices, the IMC has higher losses than CMC. For case of modulation index = 0.75 as plotted in the figure, there is break point where the IMC losses become lower than CMC as the frequency goes higher since the CMC losses are more 'sensitive' to the switching frequency.

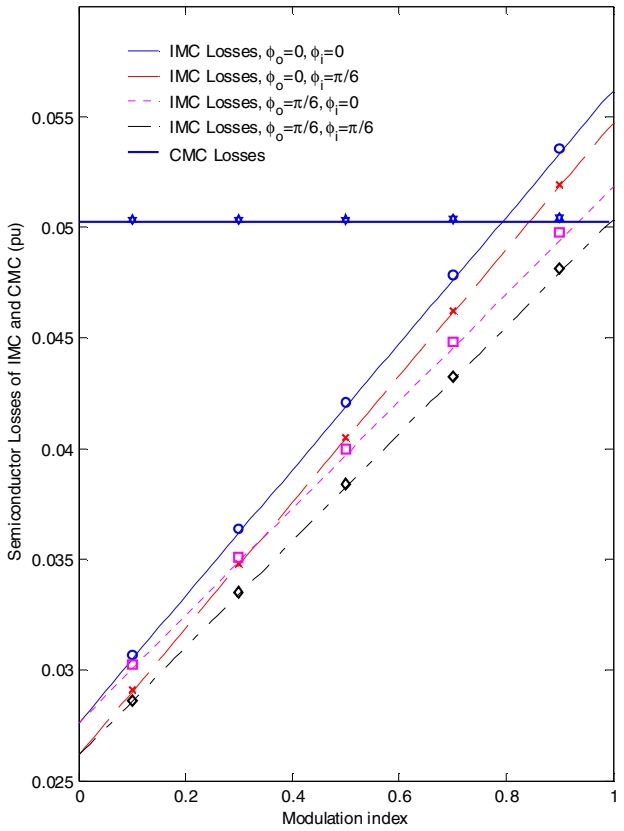

Fig. 9 Simulated and analytical power losses for CMC and IMC for different operating conditions. The lines are plots of analytical solutions and the markers on lines are the simulation results for the corresponding operating conditions.

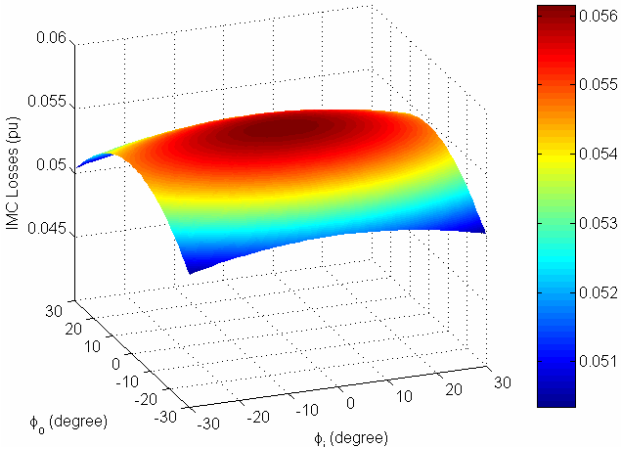

Fig. 10 Variation of the IMC losses vs input and output power factor angle ϕ_i and ϕ_o at modulation index = 1

VI. CONCLUSIONS

In this paper, an analytical approach to characterizing the semiconductor losses for two classes of matrix converters, namely CMC and IMC, has been developed. The analytical solutions are verified against numerical results from detailed simulation built on the SimuLink model. A close match between the analytical and simulated results under various operating conditions validates the effectiveness of the proposed approach.

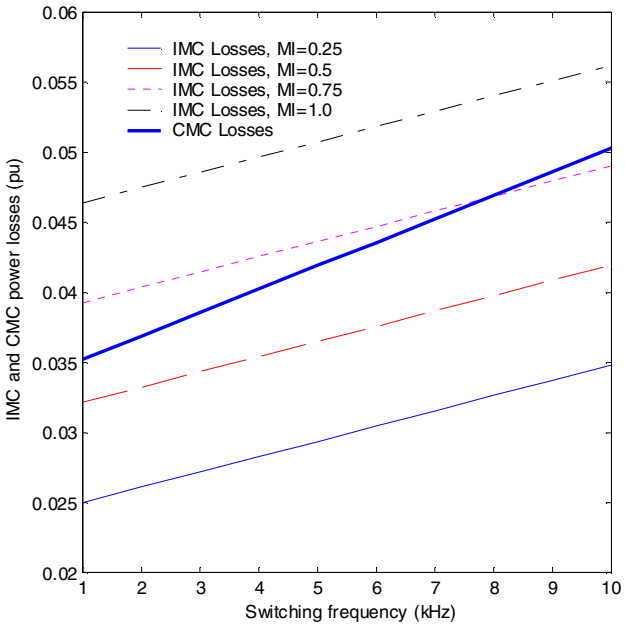

Fig. 11 Variation of power losses IMC and CMC at different switching frequencies.

It has been found power losses of the CMC and IMC respond quite differently to different operating conditions. The power losses of CMC increase as switching frequency increases while they remain invariant regardless the input and output power factors and voltage transfer ratio (or modulation index) variation. The power losses of IMC increase as the switching frequency increases, but at a smaller slope compared to the CMC. Furthermore, the IMC power losses depend on the modulation index, and input/output power factor angle and peak when modulation index is 1.0 and the input and output power factor angles are zeros. In summary the IMC tends to perform better at higher switching frequency and lower modulation index than CMC in terms of the power losses.

The analytical model presented in the paper can be readily used in computer mathematical calculation programs like a spreadsheet to estimate loss calculations in matrix converter as a rapid computer aided design tool. They may also be used in system level optimization for evaluating the effect of variations in operating conditions during thermal cycling, startup conditions, load transients, etc. in sinusoidal input/output conditions. The systematic methodology of loss estimation can be further extended to study system performance under alternate modulation algorithms, input and output waveforms and non-sinusoidal input/output conditions.

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APPENDIX A

With reference to Fig. 5, the averaged link current over one switching cycle is

$$\begin{aligned} i_{p\_avg} &= -(m_2 - m_3) i_{o3} + (m_1 - m_2) i_{o1} \\ &= \frac{\sqrt{3} M I_o}{2} \begin{bmatrix} \cos(\alpha_o(t) + \pi/2)\cos(\beta_o(t) + 2\pi/3) + \\ \cos(\alpha_o(t) + \pi/6)\cos(\beta_o(t)) \end{bmatrix} \\ &= \frac{\sqrt{3} M I_o}{2} \cos(\phi)\cos(\pi/6) \\ &= \frac{3}{4} M I_o \cos(\phi) \end{aligned} \quad (18)$$

The rms value current of the link current over one switching cycle is

$$\begin{aligned} i_{dc\_rms}^2 &= (m_2 - m_3) i_{o3}^{\ 2} + (m_1 - m_2) i_{o1}^{\ 2} \\ &= \frac{\sqrt{3} M(t) I_o^{\ 2}}{2} \begin{bmatrix} \cos(\alpha_o(t) + \pi/2)\cos^2(\beta_o(t) + 2\pi/3) + \\ \cos(\alpha_o(t) + \pi/6)\cos^2(\beta_o(t)) \end{bmatrix} \\ &= \frac{\sqrt{3} M(t) I_o^{\ 2}}{4} \begin{bmatrix} \sqrt{3}\cos\left(\alpha_o(t) + \frac{\pi}{3}\right) + \\ \frac{1}{2}\left[\cos\left(3\alpha_o(t) + 2\phi_o - \frac{\pi}{6}\right) + \cos\left(\alpha_o(t) + 2\phi_o + \frac{5\pi}{6}\right)\right] + \\ \frac{1}{2}\left[\cos\left(3\alpha_o(t) + 2\phi_o + \frac{\pi}{6}\right) + \cos\left(\alpha_o(t) + 2\phi_o - \frac{\pi}{6}\right)\right] \end{bmatrix} \\ &= \frac{\sqrt{3} M(t) I_o^{\ 2}}{4} \begin{bmatrix} \sqrt{3}\cos\left(\alpha_o(t) + \frac{\pi}{3}\right) \\ \frac{1}{2}\left[\cos\left(3\alpha_o(t) + 2\phi_o - \frac{\pi}{6}\right)\right] + \frac{1}{2}\left[\cos\left(3\alpha_o(t) + 2\phi_o + \frac{\pi}{6}\right)\right] \end{bmatrix} \\ &= \frac{3 M(t) I_o^{\ 2}}{4} \left[\cos\left(\alpha_o(t) + \frac{\pi}{3}\right) + \frac{1}{2}\sin(3\alpha_o(t) + 2\phi_o)\right] \end{aligned} \quad (19)$$

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