Evaluation of 1200V-Si-IGBTs and 1300V-SiC-JFETs for Application in Three-Phase Very Sparse Matrix AC-AC Converter Systems

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Abstract. In this paper based on experimental investigations of the power semiconductor switching behavior and on analytical calculations the conduction and switching losses of a three-phase *Very Sparse AC-AC Matrix Converter* (VSMC) supplying a permanent magnet synchronous motor are discussed in detail. There, 1200V-Si-IGBTs/1200V-Si-ultra-fast-recovery diodes and 1300V-SiC-JFET/Si-MOSFET cascodes are employed for realizing the converter power circuit. The worst case operating conditions are identified and the efficiencies resulting in dependency of the switching frequency and load current amplitude are shown in graphical form. Furthermore, the operating range of the VSMC with respect to the maximum admissible junction temperature of the power semiconductors is determined. Finally, topics to be treated in the continuation of the research are discussed briefly.

I Introduction

In [1] novel three-phase AC-AC PWM converter systems, i.e. *Sparse Matrix Converter* (SMC) topologies have been proposed, which do show a reduced count of power transistors and a significantly lower control complexity as compared to a conventional matrix converter (CMC).

As **Fig.1** shows, the system topology of a *Very Sparse Matrix Converter* (VSMC, [1]) is formed by the DC side coupling of a current DC link rectifier and a voltage DC link inverter. There, the impression of the DC link voltage is by the AC side filtering capacitors via the rectifier stage, the DC link current is formed by segments of the inductive load current and impressed via the inverter stage. Accordingly, no energy storage components have to be provided in the DC link. As for the CMC the switching frequency harmonics of the VSMC input current and output voltage are suppressed by an input filter and by the inductive characteristic of the load. Therefore, for proper control mains and load current do show a sinusoidal shape. Via the DC link only active power is transferred, therefore the input current phase displacement can be defined independent of the load current phase displacement.

However, the formation of reactive power at the input is possible only in case a sufficiently large DC link current and/or active power flow to the output is present [1].

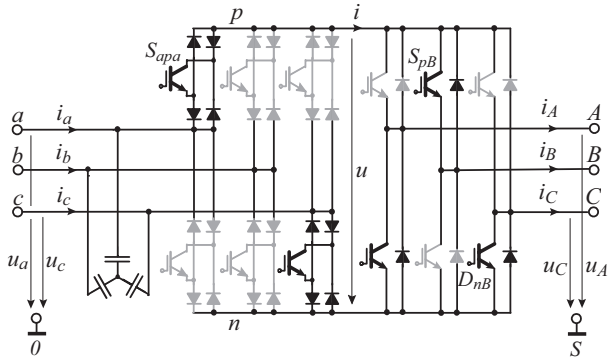


Fig.1:. Basic structure of the power circuit of the *Very Sparse Matrix Converter* (VSMC).

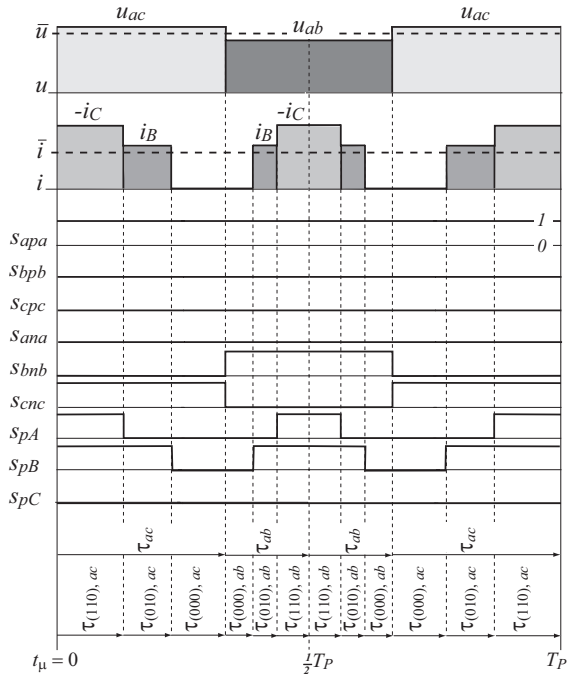


Fig.2: Formation of the DC link voltage u and DC link current i within a pulse period and corresponding switching functions of the rectifier and inverter stage being characteristic for $\varphi_1 \in (-\pi/6 ... \pi/6)$ and $\varphi_2 \in (\pi/3 ... 2\pi/3)$. Switching state changes of the rectifier stage do occur at zero DC link current. The DC link current does show equal average values (denoted by $\bar{i}$) within τ_{ac} and τ_{ab}. The switching frequency ripple of the input line-to-line voltages u_{ac} and u_{ab} and of the output phase currents i_B and i_C is neglected for the sake of clarity.

A maximum output voltage range of the VSMC is given for ohmic input characteristic, i.e. for Φ_1=0 [1]. Accordingly, all further considerations will be limited to this case.

An essential advantage of the VSMC topology does consist in the possibility of changing the switching state of the rectifier stage at zero DC link current. If the inverter output stage is switched into the free-wheeling state in advance to commutating the rectifier stage the DC link current is reduced to zero and no continuous connection of the DC link to the mains has to be considered for changing the rectifier switching state [1]. Therefore, the complex multi-step commutation in dependency on the sign of the DC link current or in dependency on the phase voltage difference of the commutating phases being characteristic for the CMC can be omitted resulting in a higher system reliability.

According to **Fig.2** and **Fig.3,** within a π/3−wide interval of the mains period always two line-to-line voltages are switched into the DC link subsequently and no free-wheeling interval of the rectifier stage is introduced. (cf. Fig.2). Accordingly, the local average value of the DC link voltage does show a variation with six times the mains frequency f_1 (cf. Fig.3). In order to achieve sinusoidally varying local average values of the inverter output phase voltages

this variation has to be compensated by an inverse adaption of the local inverter modulation index.

The aforementioned advantages do motivate a closer analysis of the novel circuit topology. There, in view of an industrial application the stresses on the power components and/or an evaluation of Si and SiC technology concerning conduction and switching losses of the power semiconductors and the relation between switching frequency and/or input filter size and efficiency of the energy conversion are of special interest.

In this paper based on experimental investigations of the switching behavior of the power semiconductors (cf. **Sections II-IV**) and on analytical calculations the conduction and switching losses (cf. **Section V**) of a VSMC supplying a permanent magnet synchronous machine are discussed in detail. There, 1200V-Si-IGBTs/1200V-Si-ultra-fast-recovery diodes and 1300V-SiC-JFET/Si-MOSFET cascodes are employed. The worst case operating conditions are identified and the efficiencies resulting in dependency of the switching frequency and load current amplitude are shown in graphical form. There, also the operating range of the VSMC with respect to the maximum admissible junction temperature of the power semiconductors is determined (cf. **Section VI**). Finally, topics to be treated in the continuation of the research are discussed briefly.

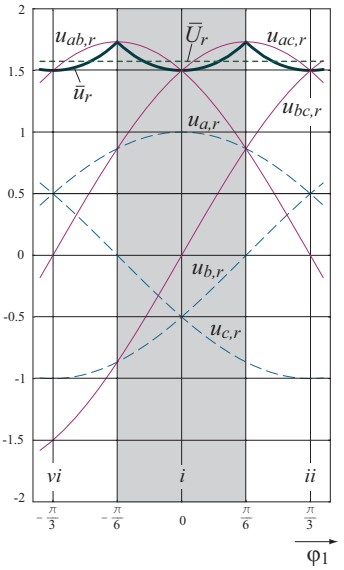


Fig.3: Time behavior of the mains phase voltages u_a, u_b, u_c, and of the local average value $\bar{u}$ of the DC link voltage u; voltages are normalized (index r) to the mains phase voltage amplitude $\hat{U}_1$. The following considerations are limited to the angle interval $\varphi_1 \in (-\pi/6 ... \pi/6)$ (input sector i), which is pointed out by a dotted area.

II Experimental Analysis of the VSMC Switching Behavior

A. Analysis of the Output Stage

The switching behavior of VSMC output stage realized in Si- and SiC-technology has been analyzed experimentally on a test setup as illustrated in **Fig.4**. The setup comprises of a foil capacitor C_S, an inverter phase leg and an inductor L_L for impressing the load current. The phase leg semiconductors are mounted on a heat sink equipped with a heating resistor, allowing to operate the setup at elevated temperatures. A control circuit (not shown in Fig.4) generates a pulse sequence where first S_{pA} is turned on until the load inductor current i_A reaches an adjustable threshold where S_{pA} is turn-off for a fixed time interval and subsequently turned on again for another fixed time interval and then finally turned off. As the repetition of this pulse sequence is with low frequency, the junction temperature is with good approximation equal to the heatsink temperature determined by the pre-heating. This allows to investigate the turn-on and turn-off behavior of S_{pA} in combination with the free-wheeling diode D_{nA}, where for employing SiC-JFETs no explicit diode is provided but the reverse conducting property of S_{nA} is utilized.

For current measurement a R10/N30 toroidal ferrite core AC current transformer with a turns ratio of 1:50, a burden resistor of 5Ω and an adaptation network to a 50Ω coaxial cable is employed. The voltage measurement is by a LeCroy DXC100A differential probe and a DA1855A differential amplifier showing a CMRR of 100dB up to 100 kHz. In order to calculate the switching losses accurately, the time lag introduced by the differential amplifier is compensated before performing the multiplication of the current and voltage signals.

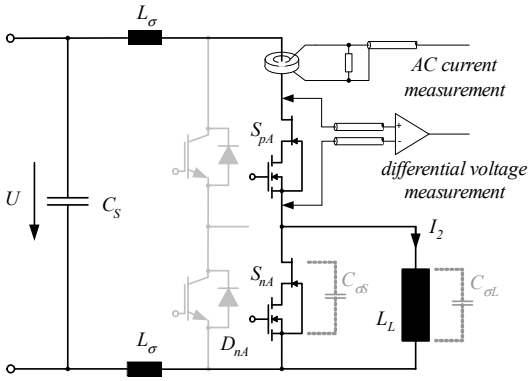


Fig.4: Test setup for switching loss measurement; for the SiC-JFET/Si-MOSFET cascode we have e.g. $C_{\sigma L}+C_{\sigma S}\approx$200pF.

Several parasitic effects do take influence on the switching losses. Of special importance are the wiring stray inductances L_σ, the semiconductor stray capacitances $C_{\sigma S}$, the current impressing inductor stray capacitance $C_{\sigma L}$ and the reverse recovery behavior of the free-wheeling diode (and/or of the power transistor operating in free-wheeling mode for SiC-JFET investigation). The bi-planar construction of the test power circuit is chosen such that the wiring inductance ($L_\sigma \approx$40 nH) is close to the properties of a full three-phase VSMC realization [1]. For an input current phase displacement of Φ_1=0 the DC link voltage of a VSMC varies from 50 to 100% of the input line-to-line voltage amplitude [1]. Accordingly, for examining the VSMC output stage the test circuit input voltage is varied between U =280…570V as a connection of the VSMC to the European low voltage mains is assumed.

In the following the switching losses of a NPT-Si-IGBT in combination with an ultra-fast recovery free-wheeling diode and a SiC-JFET/Si-MOSFET cascode circuit will be investigated.

A.1 IGBT Switching Losses

The switching losses are determined for an isolated power module of type IXYS FII50-12E (NPT IGBT) comprising a full output stage bridge leg and specified for I_{C25}=50A and V_{CES}=1200V.

The IGBT turn-off behavior is shown in **Fig.6** where the current tail considerably contributing to the total turn-off losses can be clearly identified ($R_{G,off}$=20Ω). At turn-on (cf. **Fig.7**), the relatively high reverse recovery current of the freewheeling diode is defining the peak turn-on power loss ($R_{G,on}$=20Ω).

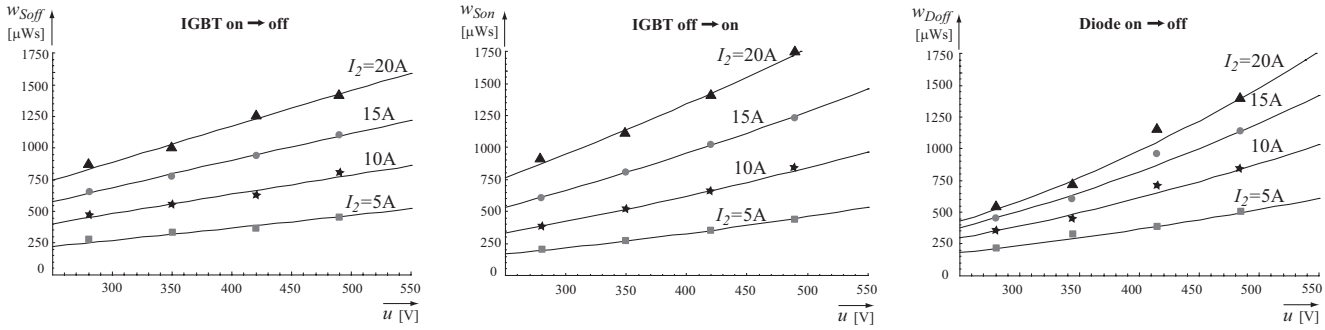


Fig.5: Measured IGBT switching losses and least-square approximations. Left: IGBT turn-off energy loss w_{Soff}; center: IGBT turn-on energy loss w_{Son}; right: free-wheeling diode turn-off energy loss w_{Doff}; Tj= 120°C.

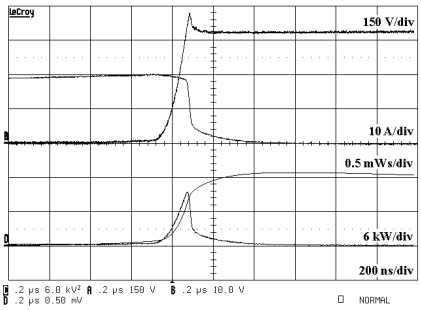


Fig.6: IGBT turn- off at 20A/490V; top: IGBT voltage and current; bottom: calculated switching power and energy loss. T_j = 25°C.

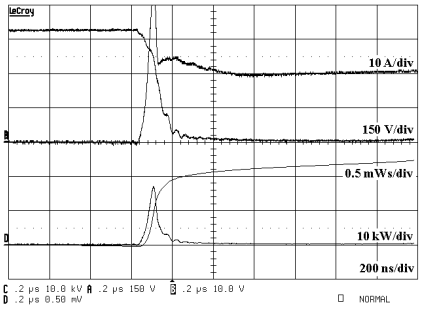


Fig.7: IGBT turn-on at 20A/490V; top: transistor voltage and current; bottom: calculated switching power and energy loss. T_j = 25°C.

The measured switching losses of IGBT and free-wheeling diode are depicted in **Fig.5** for a junction temperature of T_j=120°C. For a quadratic least-square approximation of the measured data in voltage and current we use

$$w_{Soff}(u,i) = K_{Soff1}\cdot u\cdot i_2 + K_{Soff2}\cdot u\cdot i_2^2 + K_{Soff3}\cdot u^2 + K_{Soff4}\cdot u^2\cdot i_2 + K_{Soff5}\cdot u^2\cdot i_2^2$$
$$w_{Son}(u,i) = K_{Son1}\cdot u\cdot i_2 + K_{Son2}\cdot u\cdot i_2^2 + K_{Son3}\cdot u^2 + K_{Son4}\cdot u^2\cdot i_2 + K_{Son5}\cdot u^2\cdot i_2^2$$
$$w_{Doff}(u,i) = K_{Doff1}\cdot u\cdot i_2 + K_{Doff2}\cdot u\cdot i_2^2 + K_{Doff3}\cdot u^2 + K_{Doff4}\cdot u^2\cdot i_2 + K_{Doff5}\cdot u^2\cdot i_2^2, \quad (1)$$

where only physically sensible terms are considered. E.g., the term depending solely on u^2, represents the energy loss due to parasitic capacitances.

The coefficients K_1 ... K_5 derived are compiled in **Tab.1** for T_j=25°C and 120°C, where the symbols *S* and *D* indicate the coefficients being valid for the IGBT or the freewheeling diode, and *off* and *on* indicates transistor and/or diode turn-on or turn-off switching actions.

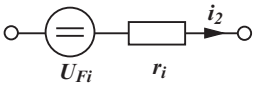


Fig.8: IGBT and free-wheeling diode equivalent circuit for calculating the conduction losses.

IGBT- Switching Loss Parameter						
T_j		K_1	K_2	K_3	K_4	K_5
25°C	S_{off}	129	-947 10^{-3}	471 10^{-3}	-84.1 10^{-3}	2.52 10^{-3}
	S_{on}	41.6	1.75	308 10^{-3}	60.7 10^{-3}	-923 10^{-6}
	D_{off}	66.6	-2.54	332 10^{-3}	95.4 10^{-3}	2.90 10^{-3}
120°C	S_{off}	179	-1.31	650 10^{-3}	-116 10^{-3}	3.48 10^{-3}
	S_{on}	70.0	2.94	518 10^{-3}	102 10^{-3}	-1.55 10^{-3}
	D_{off}	97.9	-3.73	488 10^{-3}	140 10^{-3}	4.27 10^{-3}
Units		nWs(VA)$^{-1}$	nWs(VA^2)$^{-1}$	nWs(V^2)$^{-1}$	nWs(V^{2}A)$^{-1}$	nWs(V^{2}A^2)$^{-1}$

Tab.1: Coefficients K_1 ... K_5 of the least-square approximation of the measured IGBT/free-wheeling diode switching losses.

The mathematical representation of the IGBT (and/or diode) *conduction* losses in the following sections is based on a model comprising a series voltage source $U_{F,i}$ and a differential resistor r_i (cf. **Fig.8**). Accordingly, the local average value of the conduction power loss can be expressed as

$$\overline{p}_{C,S/D} = U_{F,S/D}\cdot \bar{i}_2 + r_{S/D}\cdot i_{2,rms}^{\ 2}. \quad (2)$$

There, the indices *S*, *D* again denote whether the transistor or the diode is considered. The parameters employed in subsequent calculations are complied in **Tab.2** for T_j=25°C and 120°C.

IGBT- On-State Parameter			
T_j		U_F	r
25°C	**S**	940	52.4
	D	1250	8.04
120°C	**S**	768	78.7
	D	732	38.0
Units		mV	mVA^{-1}

Tab.2: IGBT and free-wheeling diode on-state parameters.

A.2 SiC-JFET/Si-MOSFET Cascode Switching Losses

The switching losses are determined for a cascode connection of a SiC-JFET and a low voltage Si-power-MOSFET being available from Infineon/SiCED/IXYS [7],[8] in a single package specified for I_D=4.5A (no junction temperature specified) and V_{CES}=1300 V.
In **Fig.10** the turn-off behavior of the cascode is depicted where the current shows a fall time of ≈25ns. The maximum admissible rate of change of the cascode voltage at turn-on has to be limited to 6kV/µs due to the rating of the parasitic diode of the low voltage MOSFET comprised in the free-wheeling element which in the case at hand is also implemented by a cascode (cf. Fig.2) where the gate of the low-voltage MOSFET has been short-circuited to the source. For details concerning the reverse conducting property of the cascode we would like to refer to [7] and [8] for the sake of brevity. In order not to exceed the maximum admissible du/dt-value, a relatively large gate resistor has been used for the turn-on of S_{pA} ($R_{G,on}$ = 360Ω, $R_{G,off}$ = 20Ω). Consequently, the turn-on (cf. **Fig.11**) takes significantly longer than the turn-off and thus the turn-on losses are significantly higher than the turn-off losses.

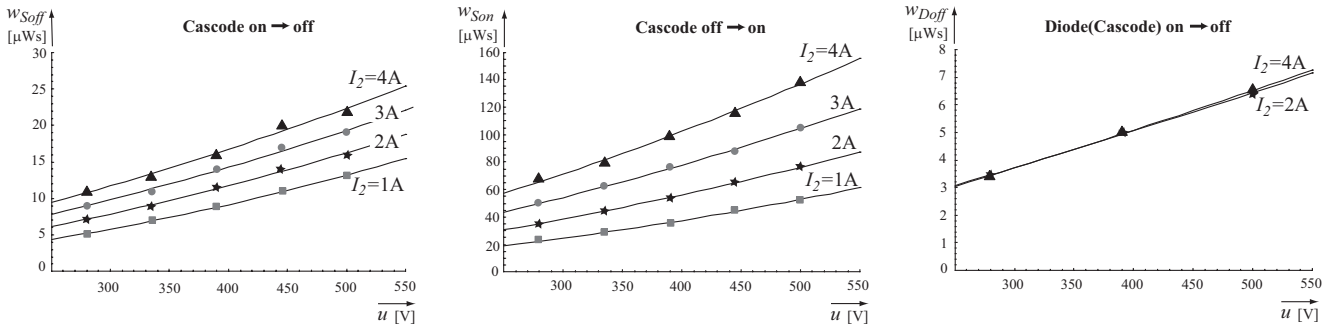


Fig.9: Measured cascode switching losses and least-square approximations. Left: cascode (transistor action) turn-off energy loss w_{Soff}; center: cascode (transistor action) turn-on energy loss w_{Son}; right: turn-off energy loss w_{Doff} for cascode acting as free-wheeling diode; Tj= 120°C.

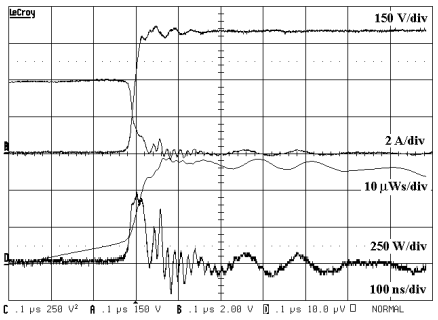


Fig.10: Cascode turn-off at 4A/500V; top: cascode voltage and current; bottom: calculated switching power and energy loss. T_j= 25°C.

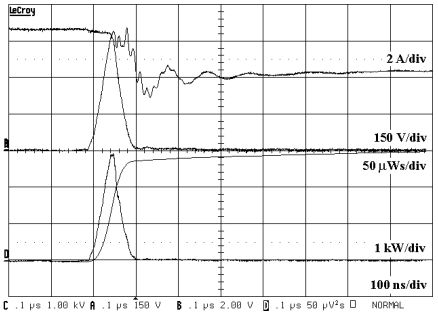


Fig.11: Cascode turn-on at 4A/500V; top: cascode voltage and current; bottom: calculated switching power and energy loss. T_j = 25°C.

The measured switching losses for transistor and free-wheeling diode action of the cascode are shown in **Fig.9** for a junction temperature of T_j=120°C. The coefficients K_1 ... K_5 of the least-square approximation of the measured data according to (1) are compiled in **Tab.3**.

SiC-Switching Loss Parameter						
T_j		K_1	K_2	K_3	K_4	K_5
25°C	S_{off}	9.16	-386 10^{-3}	40.5 10^{-3}	-6.02 10^{-3}	760 10^{-6}
	S_{on}	46.6	-135 10^{-3}	134 10^{-3}	-25.6 10^{-3}	9.15 10^{-3}
	D_{off}	8.86	-1.51	2.22 10^{-9}	1.48 10^{-3}	-156 10^{-6}
120°C	S_{off}	9.16	-386 10^{-3}	40.5 10^{-3}	-6.02 10^{-3}	760 10^{-6}
	S_{on}	58.3	-169 10^{-3}	168 10^{-3}	-32.0 10^{-3}	11.4 10^{-3}
	D_{off}	8.86	-1.51	2.22 10^{-9}	1.48 10^{-3}	-156 10^{-6}
Units		nWs(VA)$^{-1}$	nWs(VA^2)$^{-1}$	nWs(V^2)$^{-1}$	nWs(V^{2}A)$^{-1}$	nWs(V^{2}A^2)$^{-1}$

Tab.3: Coefficients K_1...K_5 of the least-square approximations of the measured cascode switching loss data (the transistor action of the cascode is indicated by *S*, the free-wheeling action by *D*).

SiC- On-State Parameter			
T_j		U_F	r
25°C	S	0	535
	D	688	492
120°C	S	0	1150
	D	568	888
Units		mV	mVA^{-1}

Tab.4: Cascode on-state parameters.

The parameters employed for the calculation of the cascode *conduction* losses in the following sections are compiled in **Tab.4** with reference to Fig.8.

B. Analysis of the Input Stage

Employing the zero DC link current commutation strategy described in [1] (cf. also Fig.2) the input stage power semiconductors are switched only in free-wheeling intervals of the output stage and/or at zero DC link current. Therefore, ideally no switching losses do occur. Switching losses remaining in practice do then originate for the reasons described in the following.

Fig.12 depicts the time-behavior of characteristic voltages and currents of the VSMC input stage realized in IGBT technology for a turn-off of S_{apa} and a subsequent turn-on of S_{bpb}. At time t_1 the VSMC output stage is switching into the free-wheeling state and as a result the current i_{Sapa} through the input stage switch S_{apa} does decrease to zero. After a predefined dead-time t_{d1} the switch S_{apa} is turned off in t_2 what however does not take any influence on the voltages or currents as we already have i_{Sapa}=0. After another predefined delay-time t_{d2}, the input stage switch S_{bpb} is turned on in t_3 and consequently a forward voltage step is applied to S_{apa} which does result is a current spike as the recombination of the charge stored in the drift region of S_{apa} has not been completed. Accordingly, switching losses do occur in the input stage power transistors also if the turn-off is in zero-current intervals. As verified experimentally the parasitic losses can be reduced by increasing the dead-time t_{d2}. However, increasing t_{d2} also does reduce the maximum inverter output voltage.

The described effect is negligible when employing SiC cascodes in the input stage.

A further switching loss component of the input stage is due to the charging and/or discharging of the parasitic DC link and power semiconductor capacitances occurring at the turn-on of S_{bpb}.

Furthermore, when the output stage returns into an active switching state the input stage has to immediately take over the resulting DC link current what does cause diode forward recovery and/or diode turn-on losses.

Based on an experimental analysis, in a first approximation a delay-time of t_{d2} = 1µs results in a ratio of the input and output stage switching losses of roughly 6% if we assume that the losses due to parasitic capacitances and due to the diode forward recovery are negligible in comparison to the input stage conduction losses. Therefore, the switching losses of the input stage will be neglected for the subsequent calculation.

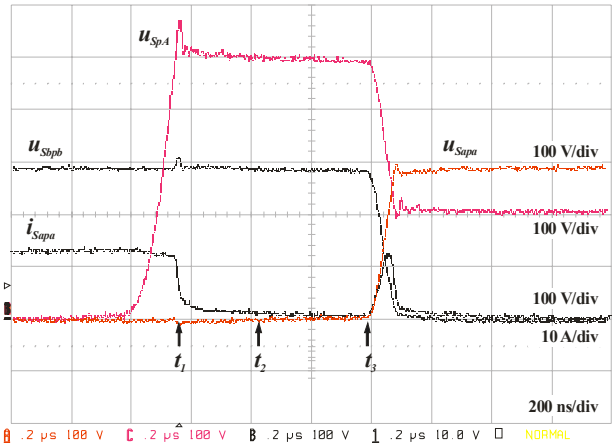


Fig.12: Commutation sequence $S_{apa} \rightarrow S_{bpb}$ of the VSMC input stage.

This assumption still has to be verified in detail for the different semiconductor technologies and for the different matrix converter input stage topologies [1] in the course of future research.

III Input Stage Considerations

A. Input Stage/Output Stage Switching Loss Balancing

As described in Section II-B , the switching losses of the input stage of an indirect matrix converter are considerably lower than the switching losses of the output stage when the input stage is commutating at zero DC link current. In this Section a method is presented which allows to transfer part of the output stage switching losses to the input stage in order to balance the switching losses of both stages.

For a converter switching state as illustrated in Fig.1 and a positive DC link current $i > 0$ opening S_{pB} will force the load current i_B into the freewheeling diode D_{nB}. Switching losses are occurring in S_{pB} and the inverter finally does output a zero vector.

Instead of opening S_{pB} one could alternatively open S_{apa}. Again the load current i_B will be forced into D_{nB} and the inverter output voltage vector will be zero. However, now the switching losses are generated in S_{apa}.

Therefore, each output stage commutation leading to zero output voltage and occurring for positive DC link current can be performed in a way which shifts the switching losses to the input stage. This is due to the fact that diodes in the opposite bridge half of the bridge legs where transistors are conducting current can act as freewheeling diodes for a positive DC link current. For a negative DC link current $i < 0$ this freewheeling path does not exist. Trying to turn off a conducting semiconductor of the input stage while the DC link current is negative (and/or a free-wheeling diode is conducting in the upper bridge half) will lead to an excessive switching overvoltage due to the missing free-wheeling path and damage the converter.

The amount of output stage commutations which do allow a switching loss balancing depends on the modulation strategy and on the phase displacement Φ_2 of the output voltage fundamental and output current space vector. As long as power is transferred in the average from the input stage to the output stage, i.e. for $\Phi_2 < \pi/2$, the DC link current must be positive for at least one inverter switching state within a pulse period. This state can be chosen to occur right before the zero vector. As shown in Fig.2 every fourth output stage switching action leads to a zero voltage vector and consequently 25% of all output stage switching actions could be initiated by the input stage resulting in a corresponding transfer of the switching losses.

B. Input stage current waveforms

The switching actions of the output stage do result in steps of the DC link current and consequently of the current in the on-state power semiconductors of the input stage. As described in Section II-B these current steps could cause diode forward recovery losses. Therefore, we will briefly analyze the DC link current shape in dependency of the output current phase displacement in order to provide a basis for a further experimental analysis.

As shown in **Fig.13**, the DC link current can be interpreted as the projection of the inverter output current space vector $\underline{i}_2$ onto the instantaneous inverter output voltage vector $\underline{u}_{(100)}$ and $\underline{u}_{(110)}$ respectively [1].

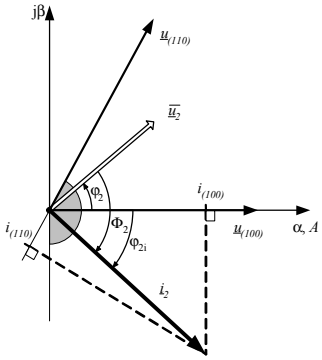


Fig.13: Inverter output voltage space vectors $\underline{u}_{(100)}$ and $\underline{u}_{(110)}$, inverter output current space vector $\underline{i}_2$ and corresponding DC link currents $i_{(100)}$ and $i_{(110)}$.

There, we assume that the phase of the fundamental inverter output voltage space vector is $\varphi_2 \in (0...\pi/3)$ and thus the instantaneous inverter output voltage vector is formed by $\underline{u}_{(100)}$, $\underline{u}_{(110)}$ and $\underline{u}_{(000)}$ (or $\underline{u}_{(111)}$) within one pulse period. Furthermore, we assume that the current space vector is lagging the voltage space vector by $\Phi_2 \in (0\ldots\pi/2)$. Therefore, the phase angle of the inverter output current space vector will be in the range of $\varphi_{2i} = \varphi_2 - \Phi_2 = -\pi/2 \ldots \pi/3$, pointed out in Fig.13. One has to note that φ_{2i} is the phase angle of the inverter output current space vector with respect to the real axis α. The DC link current assumes the value $i_{(100)}$, $i_{(110)}$ or 0, depending on the respective inverter output voltage space vector.

Fig.14 illustrates the values of the DC link currents $i_{(100)}$ and $i_{(110)}$ normalized to the output current amplitude $\hat{I}_2$ as a function of φ_{2i} for inverter output voltage vectors $\underline{u}_{(100)}$ and $\underline{u}_{(110)}$ and/or $\varphi_2 \in (0\ldots\pi/3)$. Exemplarly, the DC link current resulting for $\varphi_{2i} = -\pi/4 = \varphi_{2i,ex}$ is shown in **Fig.15** for one pulse period and the modulation strategy described in [1].

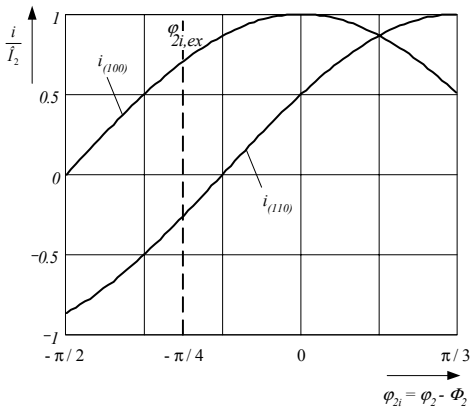


Fig.14: Normalized DC link current i as a function of $\varphi_{2i} = \varphi_2 - \Phi_2$ for inverter output voltage vectors $\underline{u}_{(100)}$, and $\underline{u}_{(110)}$ ($\varphi_2 = 0\ldots\pi/3$).

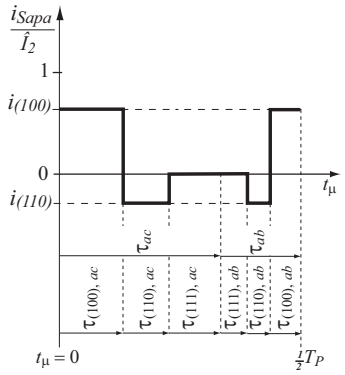


Fig.15: Typical time behavior of the current in a VSMC input stage bidirectional switch for $\varphi_{2i} = \varphi_{2i,ex} = -\pi/4$ in a pulse half period.

A detailed description of a hardware setup to be employed for an experimental analysis of the input stage switching losses will be described in the following.

IV Experimental Setup for an Exact Determination of Switching Losses Within a Pulse Period

As mentioned in section III and also in [2] the input- and output stage do affect each other concerning the occurring switching losses:

- The discontinuous behavior of the DC link current shown in Fig.15 and originating from the output stage switching actions causes losses in the diodes of the bidirectional switches of the VSMC input stage. Especially, in case the DC link current changes its direction (as shown in Fig.15) and therefore is commutated from two diodes of a four quadrant input stage switch to the other two diodes, forward recovery losses are likely to occur.
- Considering parasitic capacitances of the output stage power semiconductors, due to the changing potential of the positive or negative DC link bus resulting for an input stage switching action those capacitances (and the parasitic capacitances of the DC link and the input stage switches remaining in the off-state) are partly charged or discharged what does cause switching losses in the input stage power semiconductors conducting the charging or discharging current.

Motivated by these considerations a measuring setup employing a *three-phase* VSMC prototype is currently under development. The basic concept which will be employed for analyzing the switching loss components is shown in **Fig.16**.

An adjustable output current vector $\underline{I}_2$ will be formed in order to vary current magnitude and phase angle φ_2. Applying the output voltage vectors $\underline{u}_{(101)}$ and $\underline{u}_{(110)}$ $\underline{I}_2$ can be adjusted in the range of $\varphi_2 \in (-\pi/3 \ldots \pi/3)$. Once the specified current vector is generated an arbitrary PWM switching sequence forming a local average voltage vector within the hatched sector $\varphi_2 \in (0 \ldots \pi/3)$ of the voltage vector hexagon is generated by a programmable logic device. The practical realization of this principle is shown in **Fig.17**. There, one has to note, that the current vector formation could be controlled by measuring only a single phase current.

Fig.18 shows the switching state sequence generated by the programmable logic device (CPLD, cf. Fig.17) and the resulting behavior of the DC link quantities. For the sake of clarity the duration of the actual PWM switching sequence ($t_\mu = 0 \ldots T_P$) is drawn in enlarged time scale. The actual duration of the PWM sequence is selected such that the current vector $\underline{I}_2$ remains about constant and/or is not influenced by the generated voltage vector $\underline{\bar{u}}_2$.

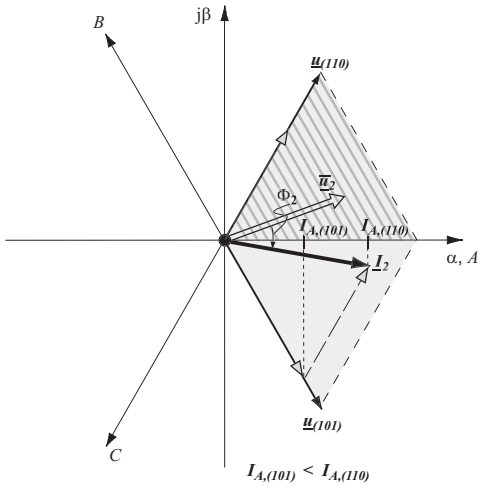


Fig.16: Formation of an output current space vector $\underline{I}_2$ by applying the output voltage vectors $\underline{u}_{(101)}$ and $\underline{u}_{(110)}$. The phase angle of $\underline{I}_2$ can be adjusted in the range of $\varphi_{2\,I} \in (-\pi/3 \ldots \pi/3)$ (entire area shown in grey). The local average output voltage vector $\underline{\bar{u}}_2$ being formed subsequently by a proper PWM switching sequence is located in the interval $\varphi_2 \in (0 \ldots \pi/3)$ (hatched area). Accordingly, the switching behavior could be investigated for $\Phi_2 \in (-\pi/3 \ldots 2\pi/3)$.

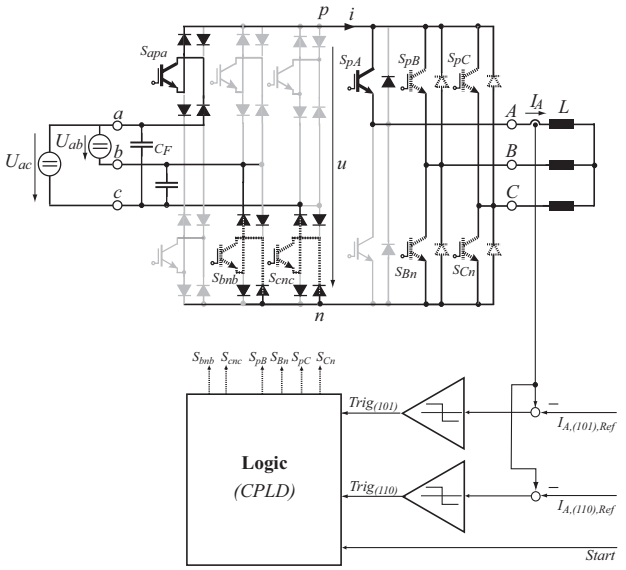


Fig.17: Concept for measuring the switching losses of a VSMC employing a three-phase VSMC power circuit prototype and an inductive load. Two adjustable DC voltage sources are connected to the VSMC input terminals in order to simulate an arbitrary phase φ_1 of the mains voltage. A CPLD (*ispMACH4A-192/96*) generates the appropriate switching functions. For controlling the output current vector formation only a single phase current has to be measured and compared to two specified reference values using analog comparators.

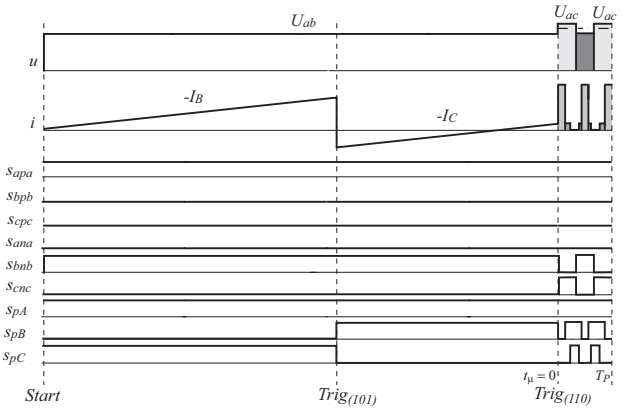


Fig.18: Switching state sequence and resulting formation of DC link voltage u and DC link current i for generating a current vector $\underline{i}_2$ (cf. Figs.16 and 17). For the sake of clarity the width of the PWM switching sequence (pulse interval $t_\mu = 0 \ldots T_P$) is shown in enlarged time scale.

V Evaluation of Measured Switching- and Conduction Losses

In the following based on the least-square approximations of the switching losses and the power semiconductor on-state behavior derived in Section II the *VSMC* conduction and switching losses will be calculated. There, analytical expressions are derived which do provide an excellent foundation for the dimensioning of the converter.

A. Basic Considerations

Since a standard application for comparable conventional converter systems (comprising a DC voltage link PWM inverter and a DC voltage link PWM rectifier) is in the field of electric drives, the *VSMC* should be investigated for feeding an electric machine. There, it is near at hand to select a permanent magnet synchronous motor (PMSM), like commonly used in servo drive applications as an exemplary load. The following analysis is based on a 3.5kW PMSM (*LUST PSM-23-20R83-0*).

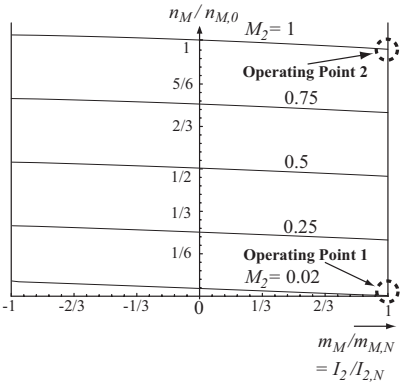


Fig.19: Torque-speed characteristic of a permanent magnet synchronous motor (PMSM) at steady state. M_2 represents the voltage transfer ratio of the converter and therefore is proportional to the amplitude of the stator voltage. The two extreme operating points marked are investigated in the paper.

The steady state torque-speed characteristic of the PMSM (having three pole pairs) is shown in **Fig.19** where, the q-component of the stator current is assumed to be impressed by field orientated control. The parameter of the family of curves, M_2, represents the voltage transfer ratio of the VSMC and therefore is proportional to the stator voltage amplitude.

Considering Fig.19 one can define two extreme operating points:

- **Operating Point1**

Nominal load torque $m_M = m_{M,N}$, speed near zero $n_M \approx 0$
$I_2 = I_{2,N} = 10\text{A}$
$f_2 \approx 0\text{Hz}$,
$M_2 = 0.02$
$\Phi_2 = 0$

Due to the very low output frequency in this operating point a certain combination of output stage semiconductors (only 5 out of 12 in total, cf. Fig.20) has to carry the load current within a wide time interval and therefore experiences maximum thermal stress (cf. Fig.24).

- **Operating Point2**

Nominal load torque $m_M = m_{M,N}$, nominal speed $n_M = n_{M,0}$
$I_2 = I_{2,N} = 10\text{A}$
$f_2 = 150\text{Hz}$,
$M_2 = 1$
$\Phi_2 = 5°$

Due to the high output frequency at this operating point the width of the time interval where a single power semiconductor experiences maximum thermal stress is significantly lower than the thermal time constant which is assumed to be in the range of 5…10ms. Furthermore, each output stage power transistor and/or power diode shows equal average losses (cf. Fig.24).

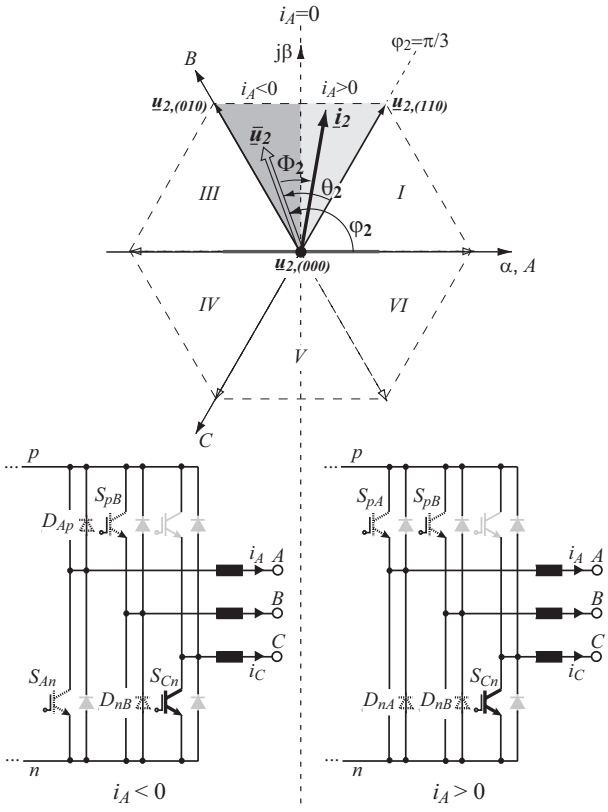


Fig.20: The angular positions of the output space vectors $\underline{\bar{u}}_2$ and $\underline{i}_2$ do determine the semiconductors being subject to power losses. In the following the output angle interval $\varphi_2 \in (\pi/3 \ldots 2\pi/3)$ and/or output sector II is considered. Switching and current carrying semiconductors are indicated by dashed lines, valves shown in grey are not subject to any losses in the considered interval. Transistor S_{Cn} is only conducting but not switching within the considered interval and thus drawn using a solid line. At $\varphi_2 = \pi/2$ phase current i_A changes its direction and in consequence, the complementary semiconductors of bridge leg A are taking over the current.

The following considerations shall initially be limited to the output angle interval $\varphi_2 \in (\pi/3 \ldots 2\pi/3)$, the corresponding sector of the output stage space vector hexagon is marked in grey in **Fig.20**. As can be seen immediately, the angular positions of the output space vectors $\underline{u}_2$ and $\underline{i}_2$ do determine the semiconductors being subject to power losses.

The output voltage space vector $\underline{\bar{u}}_2$ is formed by the active voltage vectors $\underline{u}_{(110)}$ and $\underline{u}_{(010)}$ in combination with the free-wheeling state. The transistors being switched are determined directly by the active voltage vectors. In each of the six intervals of an output period, i.e.

in each π/3-wide sector of the space vector hexagon, one output is clamped to a DC link via a power transistor (in the case at hand S_{Cn}). Accordingly, in this power transistor being shown by solid lines in Fig.20 only conduction but no switching losses do occur. Moreover, the signs of the phase currents are determining the current carrying transistor/diode pairs of a phase leg which accordingly do show power losses. E.g., for the case considered crossing the bisector $\varphi_2=\pi/2$ of the angle interval $\varphi_2\in(\pi/3...2\pi/3)$ phase current i_A, which can be derived by projecting $\underline{i}_2$ onto the phase axis A does change its sign and in consequence, the complementary semiconductors of the bridge leg A, transistor S_{An} (instead of S_{pA}) and diode D_{Ap} (instead of D_{nA}) start to conduct current. Those semiconductors which are switching and carrying current in the considered angle interval are shown with dashed lines; valves shown in light grey are not carrying any current and/or are not subject to any power loss (cf. Fig.20).

Fig.21 visualizes for the first representative fraction of a pulse period (cf. Fig.2) the time behavior of currents through the involved transistors (S_{pA}, S_{An}, S_{pB}, S_{Cn}) and the corresponding switching functions. Again it is obvious that S_{Cn} is not switching but only conducting current, S_{pB} is switching and conducting; furthermore, depending on the phase of $\underline{i}_2$ within the sector considered, either S_{pA} or S_{An} is switching and conducting current.

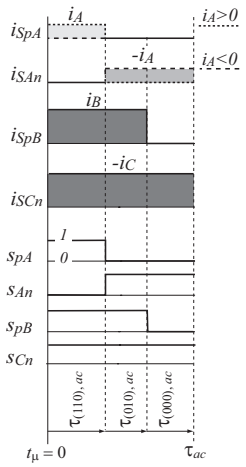


Fig.21 First segment of a pulse period being representative for the output stage switching state duty cycles (cf.Fig.2) in the considered angle interval $\varphi_2\in(\pi/3...2\pi/3)$ (cf. Fig.20). Shown are the time behavior of the inverter stage transistor currents and of the corresponding switching functions.

B. Analytic Model and Graphical Representation

Based on Subsection *A* in the following analytical expressions for the switching and conduction power losses of the single semiconductors will be derived.

At first with respect to operating point 1 the *local losses*, i.e. losses of the single semiconductors within the treated angle interval $\varphi_2\in(\pi/3...2\pi/3)$ are calculated. Next, considering the symmetries of the output stage circuit topology the results are extended to a whole output period and visualized in three-dimensional form. Finally the local losses are averaged over a whole output period in order to obtain the power losses of each valve occurring for operating point 2.

In order to limit the considerations to the essentials we will neglect the fundamental voltage drop across the filtering inductors connected in series on the input side and assume a mains voltage space vector

$$\underline{u}_1 = \hat{U}_1 \cdot e^{j\cdot\omega_1 t} \tag{3}$$

and/or corresponding phase voltages

$$\begin{aligned} u_a &= \hat{U}_1 \cos(\varphi_1) \\ u_b &= \hat{U}_1 \cos(\varphi_1 - \tfrac{2\pi}{3}) \\ u_c &= \hat{U}_1 \cos(\varphi_1 + \tfrac{2\pi}{3}) \end{aligned} \tag{4}$$

as being impressed at the system input side. There $\varphi_1=\omega_1 t$ denotes the phase and/or the position within a mains period. The system output current which is assumed to show a purely sinusoidal shape (neglecting the switching ripple) is considered to be impressed by the inductive behavior of the load and is represented by a current space vector

$$\underline{i}_2 = \hat{I}_2 \cdot e^{j\cdot(\omega_2 t - \Phi_2)} \tag{5}$$

and/or by the corresponding phase currents

$$\begin{aligned} i_A &= \hat{I}_2 \cos(\varphi_2 - \Phi_2) \\ i_B &= \hat{I}_2 \cos(\varphi_2 - \tfrac{2\pi}{3} - \Phi_2) \\ i_C &= \hat{I}_2 \cos(\varphi_2 + \tfrac{2\pi}{3} - \Phi_2). \end{aligned} \tag{6}$$

According to [1], Fig.3 and (4) we have within the considered π/3–wide interval of the mains period $\varphi_1\in(-\pi/6 ...\pi/6)$ for the local average value $\bar{u}$ of the DC link voltage

$$\bar{u} = \tfrac{3}{2}\hat{U}_1 \frac{1}{\cos(\varphi_1)}. \tag{7}$$

Based on the definition of the time-varying inverter stage modulation index

$$m_2 = \frac{\hat{U}_2}{\frac{1}{2}\bar{u}} = \tfrac{4}{3}\frac{\hat{U}_2}{\hat{U}_1}\cdot\cos(\varphi_1), \tag{8}$$

a global constant modulation index [2]

$$M_2 = \frac{3}{\pi}\int_{-\pi/6}^{\pi/6} m_2 d\varphi_1 = \frac{4}{\pi}\cdot\frac{\hat{U}_2}{\hat{U}_1}. \tag{9}$$

can be calculated by averaging over the considered mains interval (Fig.3). In the following M_2 will be used to describe the VSMC voltage transfer ratio.

With reference to [1] the duty cycles $\delta_{(110)}$ and $\delta_{(010)}$ now can be expressed as

$$\delta_{(110)} = \frac{\tau_{(110),ac}}{\tau_{ac}} = \frac{\pi}{2\sqrt{3}} M_2 \cdot \cos(\varphi_1)\cdot\cos(\theta_2 + \pi/6) \tag{10}$$

$$\delta_{(010)} = \frac{\tau_{(010),ac}}{\tau_{ac}} = \frac{\pi}{2\sqrt{3}} M_2 \cdot \cos(\varphi_1)\cdot\sin(\theta_2) \tag{11}$$

where θ_2 represents the relative phase of $\underline{\bar{u}}_2$ within the active sector of the hexagon. With reference to Fig.20 we have in the case at hand

$$\theta_2 = \varphi_2 - \pi/3. \tag{12}$$

B.1 Local Losses

B.1.1 Losses of the Single Power Semiconductors within one π/3-wide Sector of the Output Period

In the following the losses of the semiconductors being active within the considered sector II (cf. **Fig.20**) are calculated analytically. In **Fig.22** a graphical representation of the absolute values of the local losses is given for operating point 1 (f_p=15kHz, $\hat{I}_2$=10A) where the different loss components can be compared and the location of the loss maxima can be clearly identified.

B.1.1.1 **Bridge Leg B**

Transistor S_{pB}

Referring to Fig.2 the local ***switching losses*** of transistor S_{pB} occurring for the combination of input and output sector $\varphi_1\in$ (-π/6...π/6) and $\varphi_2\in(\pi/3...2\pi/3)$ are obtained by summation of the energy losses for the single switching actions within a pulse period and multiplication with the switching frequency. As a result we have

$$\begin{aligned} p_{SpB,S} &= \\ &= f_P \cdot \left[w_{S,Off}(u_{ac}, i_B) + w_{S,On}(u_{ab}, i_B) + w_{S,Off}(u_{ab}, i_B) + w_{S,On}(u_{ac}, i_B)\right] \end{aligned} \tag{13}$$

Fig.22(a) clarifies that S_{pB} shows the largest switching losses compared to all other active valves of the considered sector. The maximum is located at the end of the sector, i.e. in $\varphi_2=2\pi/3$. This is immediately clear from the space vector diagram (cf. Fig.20) as the

switched current i_B (projection of $\underline{i}_2$ onto the B-axis) assumes the highest instantaneous value in $\varphi_2=2\pi/3$.

Concerning the input sector all switching loss curves do show a maximum at $\varphi_1=0$ according to the maximum of the sum of u_{ab} and u_{ac} occurring in this point (cf. Fig.3).

Assuming a high switching frequency $f_P=1/T_P$, the phase currents (in the case at hand i_B) can be considered approximately constant within one pulse period (cf. [2]). Considering Fig.21, (2), (10) and (11) we then have for the ***conduction losses*** of S_{pB}

$$p_{SpB,C} = \left(\delta_{(110)} + \delta_{(010)}\right)\cdot i_B \cdot u_{FS,Inv} + \left(\delta_{(110)} + \delta_{(010)}\right)\cdot {i_B}^2 \cdot r_{S,Inv} \quad (14)$$

Due to the low modulation index (M_2=0.02) and since switching state (000) is employed as free-wheeling state the conduction losses of S_{pB} (which is connected to the positive DC link bus) in the considered sector are relatively low as compared to the switching losses (cf. Fig.22(a)). As a result of the dependency of (14) on the duty cycles $\delta_{(110)}$ and $\delta_{(010)}$ the maximum conduction losses do not coincide with the maximum instantaneous value of i_B occurring in $\varphi_2=2\pi/3$.

Concerning the input sector all conduction loss curves do show a maximum in $\varphi_1=0$ according to the maxima of the output duty cycles $\delta_{(110)}$ and $\delta_{(010)}$ (cf. (10), (11)) occurring in this point.

The ***total losses*** of S_{pB} now can be calculated using

$$p_{SpB} = p_{SpB,S} + p_{SpB,C} \quad (15)$$

As Fig.22(a) shows the total losses of S_{pB} (and the losses of the associated diode D_{nB}) are highest compared to other valves being active in the sector.

Diode D_{nB}

In analogy to (13)-(15) the local diode losses are

$$p_{DnB,S} = f_P \cdot \left[w_{D,Off}\left(u_{ab}, i_B\right) + w_{D,Off}\left(u_{ac}, i_B\right)\right] \quad (16)$$

Compared to all other diodes being active in sector II the ***switching losses*** of D_{nB} show the highest value (cf. Fig.22), since D_{nB} is carrying the highest current (i_B) within the whole sector.

Due to the low modulation index given for operating point 1 the relative turn-on time of diode D_{nB} is relatively high. This results in ***conduction losses***

$$p_{DnB,C} = \left(1-\left(\delta_{(110)} + \delta_{(010)}\right)\right)\cdot i_B \cdot u_{FD,Inv} + \left(1-\left(\delta_{(110)} + \delta_{(010)}\right)\right)\cdot {i_B}^2 \cdot r_{D,Inv} \quad (17)$$

which are highest as compared to all other active diodes (cf. Fig.22) as i_B is the highest phase current in the sector.

In consequence the ***total losses*** of D_{nB}

$$p_{DnB} = p_{DnB,S} + p_{DnB,C} \quad (18)$$

are determining the maximum thermal diode stress as is confirmed by Fig.22.

For operating point 1 (f_p=15kHz, $\hat{I}_2$=10A) and the employed power semiconductors the total losses of the transistor S_{pB} and the diode D_{nB} being subject to the maximum thermal stresses accidentally turn out to be about equal, i.e. $p_{SpB,max} \approx p_{DnB,max}$. As is obvious from Fig.22(a), the transistor losses are largely determined by the switching losses whereas for the diodes the ratio of the switching and conduction losses (≈4/3) is quite balanced. From this it follows that increasing the switching frequency f_p results in $p_{SpB,max} > p_{DnB,max}$, while reducing f_p would lead to $p_{SpB,max} < p_{DnB,max}$.

B.1.1.2 Bridge Leg C

Transistor S_{Cn}

Since output C is continuously clamped to the negative DC link bus via transistor S_{Cn}, in bridge leg C only conduction losses of S_{Cn} (and no diode losses) do occur

$$p_{SCn,S} = 0 \quad (19)$$

$$p_{SCn,C} = -i_C \cdot u_{FS,Inv} + {i_C}^2 \cdot r_{S,Inv} \quad (20)$$

$$p_{SCn} = p_{SCn,C} \cdot \quad (21)$$

As is immediately clear from the space vector diagram (cf. Fig.20), the conduction loss maximum is located at the beginning of the sector and/or coincides in time with the highest instantaneous value of i_C.

B.1.1.3 Bridge Leg A, $i_A>0$

Transistor S_{pA}

In analogy to Eqs.(13)-(15) we have

$$p_{SpA.,S} = = f_P \cdot \left[w_{S,Off}\left(u_{ac}, i_A\right) + w_{S,On}\left(u_{ab}, i_A\right) + w_{S,Off}\left(u_{ab}, i_A\right) + w_{S,On}\left(u_{ac}, i_A\right)\right] \quad (22)$$

$$p_{SpA,C} = \delta_{(110)} \cdot i_A \cdot u_{FS,Inv} + \delta_{(110)} \cdot {i_A}^2 \cdot r_{S,Inv} \quad (23)$$

$$p_{SpA} = p_{SpA,S} + p_{SpA,C} \quad (24)$$

Diode D_{nA}

In analogy to the relations for diode D_{nB} we have

$$p_{DnA,S} = f_P \cdot \left[w_{D,Off}\left(u_{ab}, i_A\right) + w_{D,Off}\left(u_{ac}, i_A\right)\right] \quad (25)$$

$$p_{DnA,C} = \left(1-\delta_{(110)}\right)\cdot i_A \cdot u_{FD,Inv} + \left(1-\delta_{(110)}\right)\cdot {i_A}^2 \cdot r_{D,Inv} \quad (26)$$

$$p_{DnA} = p_{DnA,S} + p_{DnA,C} \cdot \quad (27)$$

For $i_A > 0$ the maximum of switching and conduction losses of S_{pA} and D_{nA} is located at the beginning of the sector ($\varphi_2=\pi/3$). In contrary, for $i_A < 0$ the losses of S_{An}, and D_{Ap} show a maximum at the end of the sector ($\varphi_2=2\pi/3$).

Due to symmetry properties (cf. space vector diagram, Fig.20) the switching loss curves show a symmetry with respect to $\varphi_2=\pi/2$.

B.1.1.4 Bridge Leg A, $i_A<0$

Transistor S_{An}

In analogy to $i_A>0$ we have

$$p_{SAn.,S} = = f_P \cdot \left[w_{S,On}\left(u_{ac}, -i_A\right) + w_{S,Off}\left(u_{ab}, -i_A\right) + w_{S,On}\left(u_{ab}, -i_A\right) + w_{S,Off}\left(u_{ac}, -i_A\right)\right] \quad (28)$$

$$p_{SAn,C} = \left(1-\delta_{(110)}\right)\cdot\left(-i_A\right)\cdot u_{FS,Inv} + \left(1-\delta_{(110)}\right)\cdot {i_A}^2 \cdot r_{S,Inv} \quad (29)$$

$$p_{SAn} = p_{SAn,S} + p_{SAn,C} \cdot \quad (30)$$

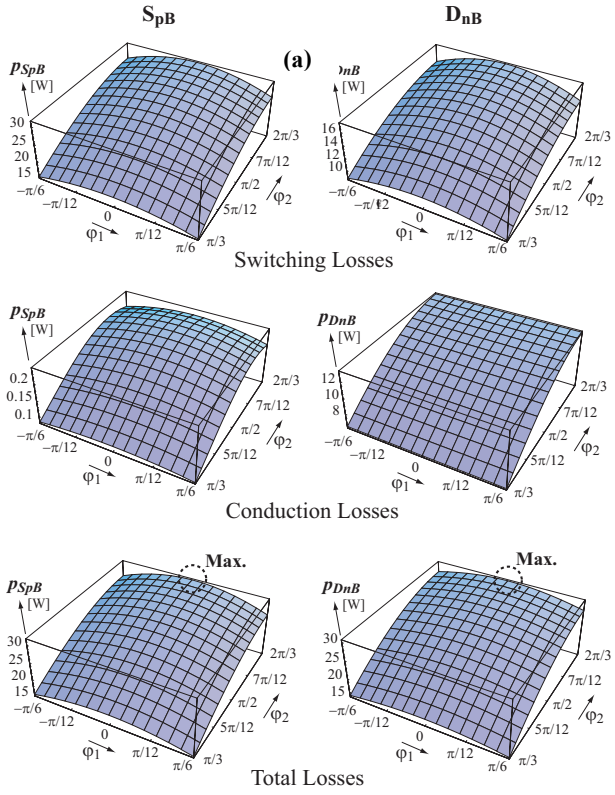
Diode D_{Ap}

In analogy to $i_A>0$ we have

$$p_{DAp,S} = f_P \cdot \left[w_{D,Off}\left(u_{ac}, -i_A\right) + w_{D,Off}\left(u_{ab}, -i_A\right)\right] \quad (31)$$

$$p_{DAp,C} = \delta_{(110)} \cdot \left(-i_A\right) \cdot u_{FD,Inv} + \delta_{(110)} \cdot {i_A}^2 \cdot r_{D,Inv} \quad (32)$$

$$p_{DAp} = p_{DAp,S} + p_{DAp,C} \cdot \quad (33)$$



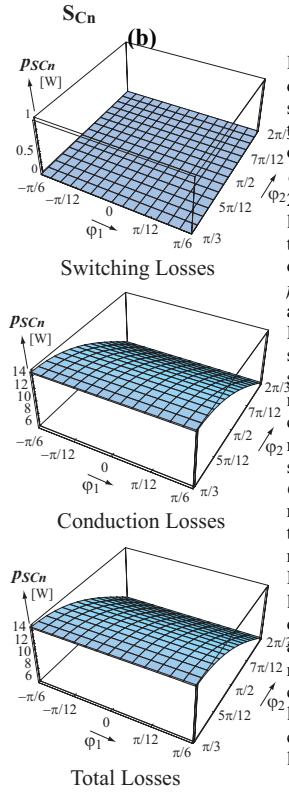
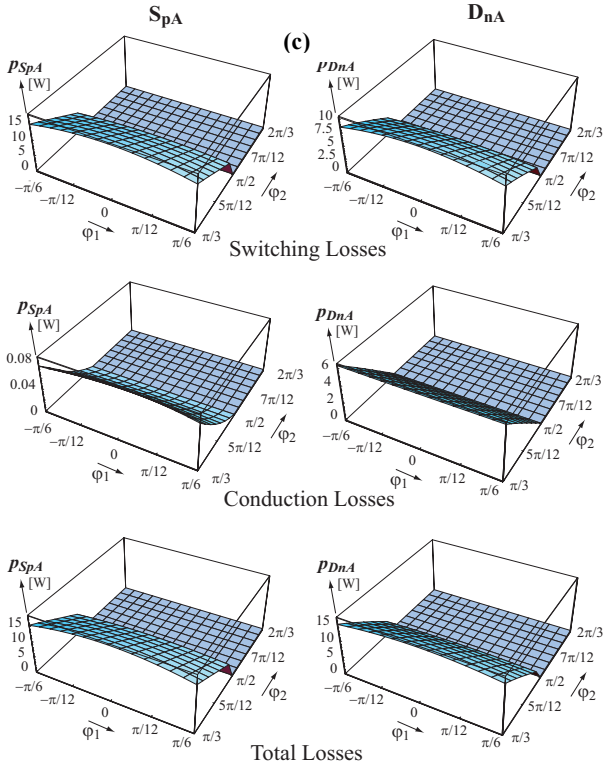
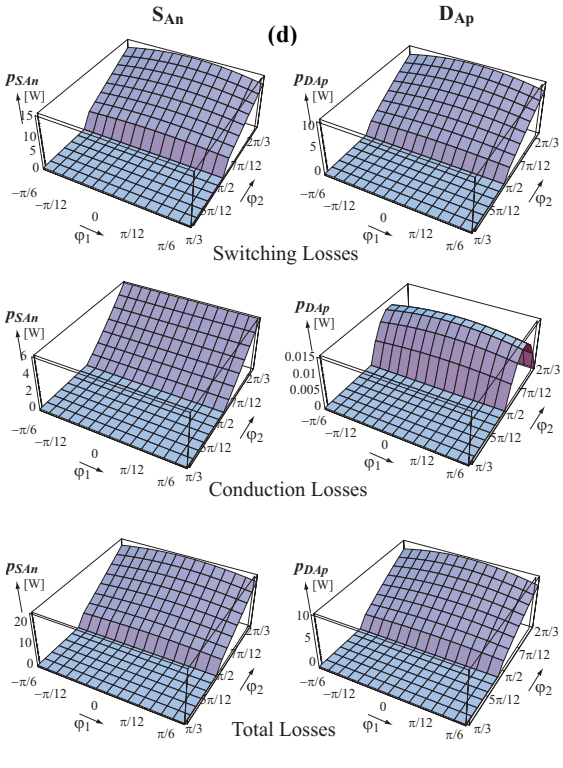


Fig.22: Local losses of the output stage power semiconductors being active for the combination of input and output sectors $\varphi_1 \in (-\pi/6 ... \pi/6)$ and $\varphi_2 \in (\pi/3 ... 2\pi/3)$. Shown are the switching losses, conduction losses and total losses for an exemplary operating point 1 (where f_p=15kHz, and $\hat{I}_2$=10A is assumed). **(a)** Characteristics for Bridge leg *B*, S_{pB} and D_{nB} are subject to the highest thermal stress. Due to the low modulation index (M_2=0.02) the conduction losses of S_{pB} are negligible as compared to the switching losses. **(b)** Bridge leg *C*, as S_{Cn} is continuously remaining in the on-state only transistor conduction losses and no diode losses do occur. **(c)** Bridge leg A, i_A>0, **(d)** Bridge leg *A*, i_A<0, the characteristics of the switching losses for i_A>0 and i_A<0 are symmetric with respect to φ_2=π/2; the conduction losses are negligibly low in the active valves connected to the positive DC link bus.





For i_A> 0 the switching and conduction losses of S_{pA}, D_{nA} show a maximum at the beginning of the sector, i.e. in φ_2=π/3. In contrary, for i_A< 0 resp. S_{An}, and D_{Ap} the highest losses do occur at the end of the sector, i.e. in φ_2=2π/3.

Due to symmetry properties (cf. space vector diagram, Fig.20) the switching loss curves show a symmetry with respect to φ_2=π/2. The main conduction losses do occur in the valves connected to the negative DC link bus. Therefore, apart from S_{pB}, and D_{nB}, S_{An} temporarily does experience a high thermal stress.

B.1.2 Losses of a Single Output Stage Power Semiconductor Within a Whole Output Period

Starting from the local loss characteristics discussed in Subsection B.1 for the different valves being active within a π/3-wide sector of the output period the entire local loss characteristic of a valve within the whole output period can be derived based on symmetry considerations. This is shown in **Fig.23** for the (normalized) total losses of transistor S_{pB}, where in sector II the loss characteristic calculated in Subsection B.1 is depicted. The conditions experienced by by S_{Cn} in sector II are valid for S_{pB} in sector III, where S_{pB} is remaining in the on-state, carrying a positive current and clamping output *B* to the positive DC link bus. In sectors IV and I i_B is changing its sign and therefore the loss characteristics of S_{pA} and S_{An} known for sector II are relevant for S_{pB} there. Within sectors V and VI i_B is negative, therefore no power losses do occur in S_{pB} as the transistor is connected to the positive DC link bus.

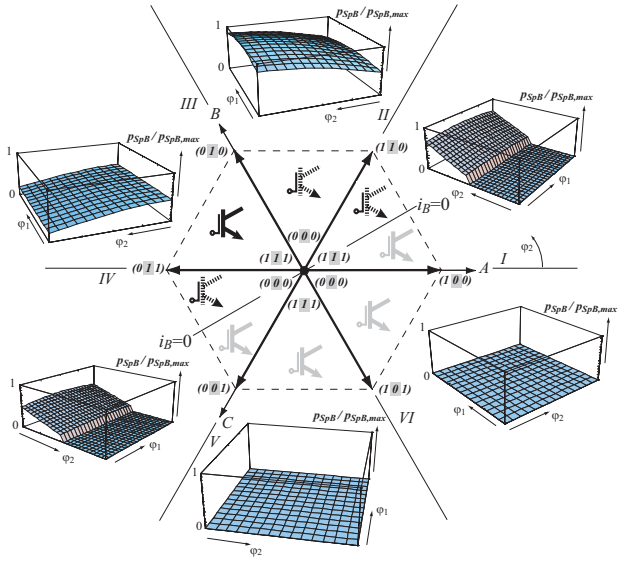


Fig.23: Calculation of the local losses of S_{pB} within a whole output voltage period based on the local losses of the output stage transistors being active within sector II. For $i_B < 0$, S_{pB} is not carrying any current, accordingly no power losses do occur within this interval. The switching sequence being applied to S_{pB} in the single sectors can be directly seen from the corresponding switching state digit highlighted in grey.

The aforementioned symmetry considerations do result in the (normalized) characteristic of the local losses of S_{pB} depicted in **Fig.24**. There, the φ_2-coordinate indicates a position within the output voltage fundamental period and/or covers the sectors I…VI. The φ_1-coordinate indicates a position within the input voltage period and/or covers the sectors i…vi. One can clearly identify the variation of the local average value of the DC link voltage with six times the input frequency (cf. Fig.3) resulting in a corresponding variation of the local losses.

Depending on the ratio of output frequency f_2 and input frequency f_1 the linear trajectory of the operating point ($\varphi_2=2\pi f_2 t$, $\varphi_1=2\pi f_1 t$) in the φ_2,φ_1-plane will show a characteristic slope and result in a corresponding variation of the local losses. E.g., for $f_2 >> f_1$ the operating point will cross the φ_2,φ_1-plane within $\varphi_1 \in (0,2\pi)$ several times about parallel to the φ_2-axis, whereas for $f_1 >> f_2$ the trajectory will be about parallel with the φ_1-axis.

For other transistors of the output stage the loss characteristic will show an incidental shape, however, the scale of the φ_2-axis will be shifted with reference to the scale valid for S_{pB} as the a transistor might conduct another phase current and/or another current half wave.

The loss characteristic resulting for the diodes shows qualitatively a shape similar to Fig.24. The main difference is that within the clamping interval of the transistor lying in antiparallel no current conduction and/or no losses do occur.

The loss characteristics of output stage transistors and diodes resulting for operating point 2 are similar to the characteristics given for operating point 1. However, due to the high modulation index

- the transistor conduction losses and in consequence the total losses do increase in sectors II and IV but decrease in sector I;
- the total diode losses are lower in sectors II and IV but do increase in sector I.

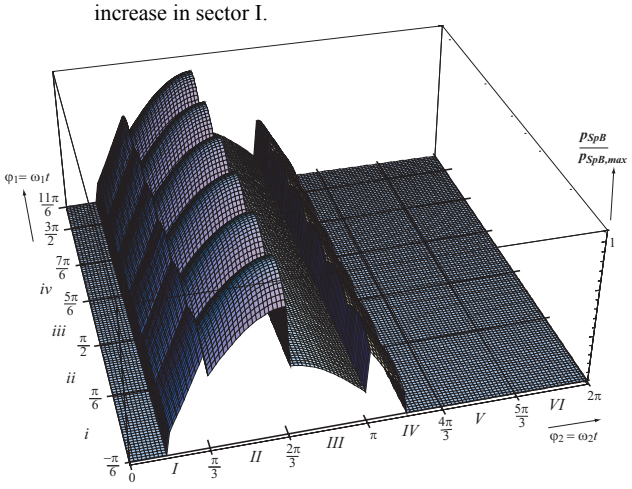


Fig.24: Characteristic of the total local losses of transistor S_{pB} within an input- and output period combination. $\varphi_2 \in (0,2\pi)$ and/or output voltage fundamental period; $\varphi_1 \in (0,2\pi)$ and/or input voltage (mains) period. The characteristic is valid for operating point 1 (f_P=15kHz, $\hat{I}_2$=10A).

B.1.3 Analytical Formulation of Local Loss Maxima

For dimensioning the converter output stage we refer to operating point 1 as there due to the very low output frequency ($f_2 \approx 0$) the maxima of the characteristic of the (local) losses have to be considered as existing continuously. According to Fig.24 and Fig.22(a) for S_{pB} the highest losses are occuring in output sector II.

Transistor

Based on the least-square approximation of the switching losses (cf. (1)) and on the on-state model (cf. Fig.8) we have for the maximum of the total local losses of an output stage transistor in general

$$p_{S,\max} = p_{SpB,\max} =$$
$$= \frac{3}{2} f_P \hat{U}_1 \cdot \left[3K_3 \cdot \hat{U}_1 + \left(2K_1 + 3K_4 \cdot \hat{U}_1\right) \cdot \hat{I}_2 + \left(2K_2 + 3K_5 \cdot \hat{U}_1\right) \cdot \hat{I}_2{}^2 \right] +$$
$$+ \frac{\pi}{4} M_2 \hat{I}_2 \cdot \left(U_{FS,Inv} + r_{S,Inv} \cdot \hat{I}_2\right) \tag{34}$$

There, in the first term represents the switching losses, the second term represents the conduction losses. The coefficients K_i are representing the turn-off and turn-on parameters,

$$K_i = K_{SOff,i} + K_{SOn,i} \tag{35}$$

Diode

As for the transistors and diodes an identical approach for approximating the switching losses has been chosen (cf. Section II-A.1II A.1) (34) is also valid for the maximum local diode losses considering the following substitutions

$$K_i \rightarrow K_{DOff,i} \tag{36}$$

$$(U_{FS,Inv}, r_{S,Inv}) \rightarrow (U_{FD,Inv}, r_{D,Inv}) \tag{37}$$

$$\frac{\pi}{4}M_2 \rightarrow (1-\frac{\pi}{4}M_2) \tag{38}$$

B.2 Global Average Losses

B.2.1 Switching Losses

For high output frequencies f_2 as given in operating point 2 (f_2=150Hz at n_M= n_{M0}) the local loss maxima are not relevant anymore for thermal dimensioning as the thermal time constant of the power semiconductors is in the range of τ_{th}=5…10ms. Therefore, the (global) average losses occurring within an output period have to be considered where the local DC link voltage is varying with six times the input frequency.

Transistor

In a first approximation we have for the global switching losses of the transistor

$$P_{Sw,Inv} = \frac{1}{4\pi^2}\int_0^{2\pi}\int_{-\pi/6}^{11\pi/6} p_{SpB}\,d\varphi_1 d\varphi_2 = \\ = \frac{3}{2\pi^2}\int_0^{2\pi}\left(\int_{-\pi/6}^{\pi/6} p_{SpB}\,d\varphi_1\right)d\varphi_2 \tag{39}$$

where the outer integral has to be solved for each sector of the output period separately and the output current phase displacement Φ_2 has to be taken into account [2].

For $\Phi_2 \in (-\pi/6 \ldots \pi/6)$ one receives for the global average switching losses of one single transistor

$$P_{Sw,Inv,S}(\Phi_2) = \\ = \frac{3 f_P \hat{U}_1}{32\pi^2}\cdot\Big[-3\hat{I}_2\cdot\Big(12\sqrt{3}\big(4K_1\cos\Phi_2 + \hat{I}_2 K_2\cos(2\Phi_2)\big)+ \\ +\big(9+4\sqrt{3}\pi\big)\cdot\hat{U}_1\big(4K_4\cos\Phi_2 + \hat{I}_2 K_5\cos(2\Phi_2)\big)\Big)+ \\ +12\hat{I}_2\cdot\Big(\big(48-12\sin\Phi_2\big)K_1 + \hat{I}_2\cdot\big(8\pi - 9\sin(2\Phi_2)\big)K_2\Big)+ \\ +\big(3\sqrt{3}+4\pi\big)\cdot\hat{U}_1\big(16\pi K_3 + 8\hat{I}_2\big(6-12\cdot\sin\Phi_2\big)K_4 + \hat{I}_2^2\big(8\pi - 9\cdot\sin(2\Phi_2)\big)K_5\big)\Big] \tag{40}$$

where K_i is defined by (35). The global average switching loss of all output stage (inverter) transistors then results from

$$P_{\sum Sw,Inv,S} = 6\cdot P_{Sw,Inv,S} \tag{41}$$

Diode

The analytical expression (40) is valid also for the global average switching losses of an output stage diode, in case (36) is considered for substituting the parameter K_i.

For directly calculating the global average switching losses of the whole inverter stage

$$P_{Inv,S} = P_{\sum Sw,Inv,S} + P_{\sum D,Inv,S} \tag{42}$$

the parameters K_i in (40) can be substituted by

$$K_i \rightarrow 6\cdot(K_{SOff,i} + K_{SOn,i} + K_{DOff,i}). \tag{43}$$

The result then basically is identical to (51) of [2]. The differences of (40) and (51) as given in [2] are originating only from the more accurate approximation of the switching losses used in this paper.

B.2.2 Conduction Losses

Transistor

For the global average conduction losses of a single transistor a less complex but not less accurate expression is gained by applying the approach proposed in [1], [2]

$$P_{Sw,Inv,C}(\Phi_2) = \\ = \frac{\hat{I}_2}{24\pi}\Big[3\big(\hat{I}_2\cdot\pi r_{S,Inv} + 4U_{FS,Inv}\big)+M_2\cdot\big(8\hat{I}_2 r_{S,Inv} + 3\pi U_{FS,Inv}\big)\cdot\cos\Phi_2\Big] \tag{44}$$

The global average conduction losses of all inverter transistors then result from

$$P_{\sum Sw,Inv,C} = 6\cdot P_{Sw,Inv,C}. \tag{45}$$

Diode

For the inverter stage diodes (44) is valid considering the substitution

$$M_2 \rightarrow -M_2. \tag{46}$$

C. Verification of the Analytical Results

In **Fig.25** the global switching losses of the total inverter stage $P_{Inv,S}$ calculated based on (40) are depicted in dependency on the output current/voltage phase displacement Φ_2. The analytically gained values (shown by a bold line) are compared to corresponding simulation data for different output frequencies f_2 (f_1=50Hz) and/or different input/output frequency ratios. In the simulation for each switching action the switching losses according to (1) are considered, and the sum of all switching loss energies is finally averaged over the time period $Max(1/f_1, 1/f_2)$.

As can be seen from Fig.25 the deviations of the analytical results from the (exact) simulation data is limited within the entire frequency range (f_1=50Hz, f_2=5…750Hz) and for all phase displacements Φ_2 to 10%. Therefore, the analytical calculation provides an excellent basis for the thermal dimensioning of the converter.

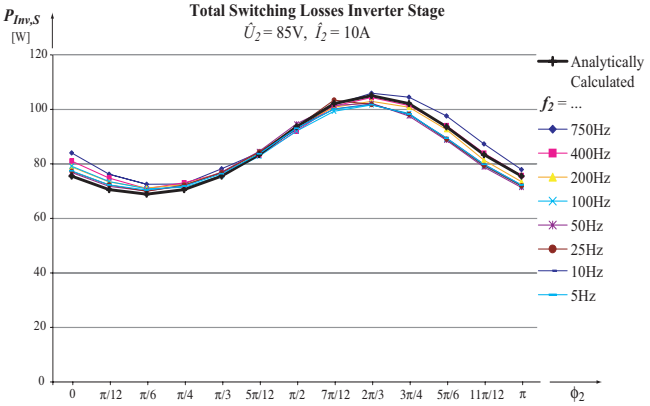


Fig.25: Total global switching losses $P_{Inv,S}$ of the inverter stage in dependency on the output current/voltage phase displacement Φ_2. Comparison of the analytically calculated losses (bold line) with exact digital simulation data for different ratios of input-/output frequency (f_1=50Hz, $\hat{U}_1$=230V, f_P=20kHz, purely sinusoidal output current).

Remark: For investigating the dependency of the accuracy of the analytical result (40) on the input/output frequency ratio the permanent magnet synchronous motor is excluded from the simulation model and a purely sinusoidal output current is impressed by current sources. Otherwise, for changing output frequency f_2 the modulation index and/or output voltage fundamental amplitude $\hat{U}_2$ would have to be adapted accordingly. The output voltage amplitude $\hat{U}_2$=85V considered in Fig.25 corresponds to a machine speed of n_M=1000min^{-1}, and $\hat{I}_2$=10A is equal to the machine nominal load current, thus only f_2=50Hz represents a real operating point of the motor.

VI RESULTS

Based on the above gained analytical expressions for the losses of the power semiconductors, in the following diagrams showing the dependency of the thermally maximum admissible output current

amplitude on the switching frequency and the resulting converter efficiency for both operating points of the PMSM are given (cf. Fig.19). There, typical values for the thermal resistance between junction and heat sink, i.e. $R_{th,S,JH}$ =1.2K/W for the transistors and $R_{th,D,JH}$=2.6K/W for the diodes [6] and a heat sink temperature of T_H =75°C are assumed and all power semiconductors are considered to operate at maximum junction temperature T_j=120°C.

For the converter efficiency we define

$$\eta(f_P,\hat{I}_2)=1-\frac{P_{Loss,VSMC}(f_P,\hat{I}_2)}{S_2(M_2=1,\hat{I}_2=\hat{I}_{2,\max}(f_P))}. \qquad (47)$$

There,

$$P_{Loss,VSMC}=P_{Inv,S}+P_{Inv,C}+P_{Rect,C}. \qquad (48)$$

considers the switching and conduction losses of the inverter stage and the conduction losses of the rectifier stage which are calculated according to [2]. The apparent output power

$$S_2=\frac{3}{2}\frac{\pi}{4}\hat{U}_1\cdot M_2\cdot\hat{I}_2, \qquad (49)$$

is set to its admissible maximum value (according to $\hat{I}_{2,max}$) for a given switching frequency f_P.

The following presentation of the results is structured in terms of the two investigated semiconductor technologies, i.e. Si-IGBTs/Si-diodes and SiC-cascodes and moreover in terms of operating point 1 and operating point 2.

A. IGBT-Technology

A.1 Operating Point 1

In **Fig.26** the limitations of the output current amplitude resulting from the individual power semiconductors by limiting the maximum admissible junction temperature to T_J=120°C are shown.

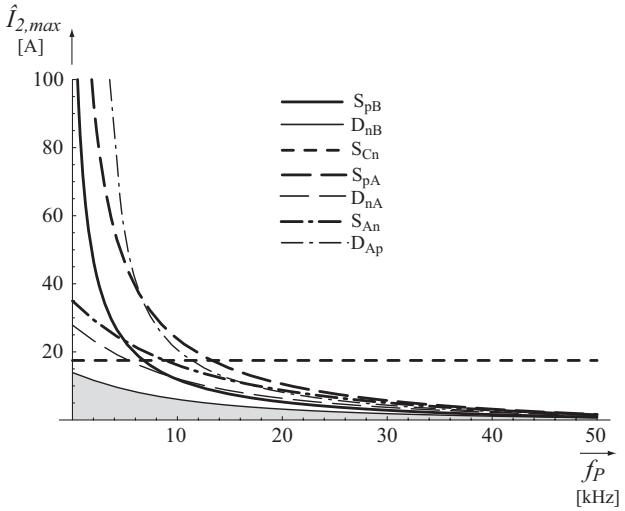


Fig.26: Limitation of the maximum admissible output current amplitude as resulting from a limitation of the power semiconductor junction temperature to T_j=120°C for operating point 1. The losses of the output stage free-wheeling diodes (in the output sector considered diode D_{nB}) do limit the output current. The area highlighted in grey marks the admissible operating area.

The main limitation is by the output stage free-wheeling diodes (cf. loss characteristic of D_{nB} in Fig.20) due to the high thermal resistance as compared to the power transistors; for a switching frequency of f_P=20kHz we have only $\hat{I}_{2,max}$≈3.5A.

In **Fig.27** the dependency of the limitation of $\hat{I}_2$ originating from the output stage free-wheeling diodes on the switching frequency and the corresponding conversion efficiencies η and the ratio ξ of switching losses and total losses are shown. The ratio ξ is depicted for the actual limiting valve (D_{nB} at the output sector considered) and for the whole VSMC.

Due to the large portion of conduction losses on the total losses of D_{nB} as caused by the low modulation index (cf. Fig.22(a)) the corresponding ratio ξ is lower than for the whole VSMC nevertheless the total converter losses also do include the rectifier stage conduction losses which are however comparably small due to the low modulation index M_2=0.02.

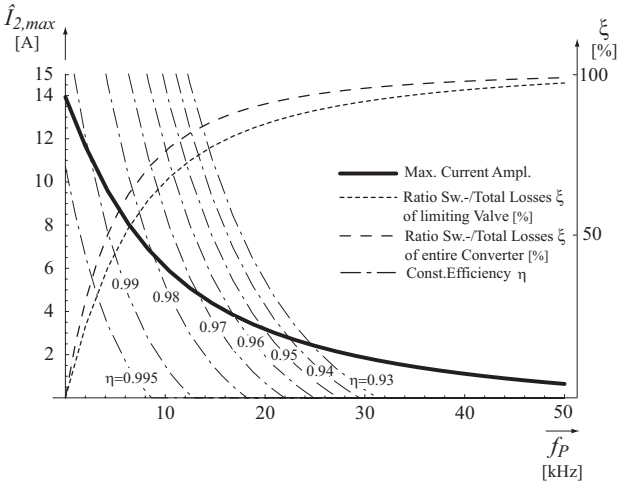


Fig.27: Thermal limitation of output current amplitude, corresponding overall VSMC efficiency η and ratio ξ of switching and total losses (scale on the right) for operating point 1 and T_j=120°C. The relation ξ is shown for the actual limiting valve and for the whole VSMC. As T_j=120°C is assumed for all power semiconductors, for low current amplitudes (and/or actual lower junction temperatures and/or lower switching losses) higher conversion efficiencies might result in practice.

For a switching frequency of f_P=20kHz there results an efficiency of η≈95%@ $\hat{I}_{2,max}$≈3.5A.

A.2 Operating Point 2

In **Fig.28** the limitations of the output current amplitude resulting from the individual power semiconductors by limiting the maximum admissible junction temperature to T_j=120°C are shown. For switching frequencies lower than ≈45kHz the output stage power transistors do limit the admissible output current amplitude; for higher switching frequencies the free-wheeling diodes are determining $\hat{I}_{2,max}$.

The global average power losses of the output stage diodes are relatively low as compared to the power transistors. Besides the lower diode conduction voltage drop (Fig.5, Tab.2) this is due to the large modulation index which does lead to high diode conduction losses in only one sector of the output period (in two sectors the conduction losses are lowered by increasing modulation index). Furthermore, in contrast to the transistors there is no clamping interval in which high losses do occur. Therefore, the limitation of the current amplitude for high switching frequencies results from the thermal resistance $R_{th,D,JH}$ being considerably higher than the thermal resistance $R_{th,S,JH}$ of the power transistor.

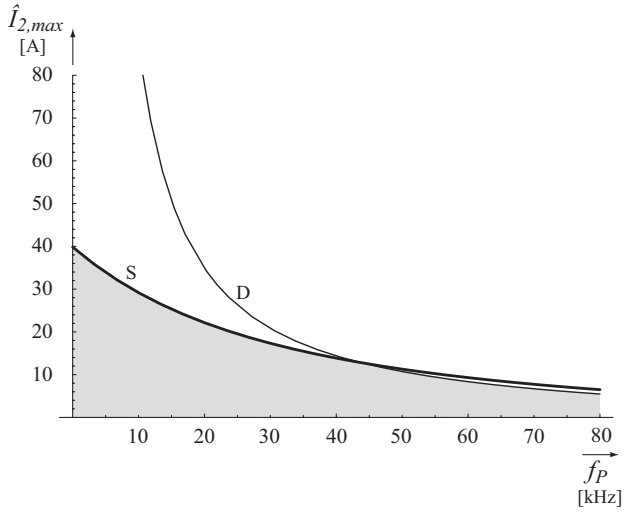


Fig.28: Limitations of the output current amplitude as given for the maximum admissible thermal stress $T_{j,max}$=120°C on the output stage transistors and diodes for operating point 2. For switching frequencies lower than ≈45kHz the power transistors are determining the thermally maximum admissible output current amplitude $\hat{I}_{2,max.}$.

In **Fig.29** the dependency of the limitation of $\hat{I}_2$ on the switching frequency and the corresponding conversion efficiencies η and the ratio ξ of switching losses and total losses are shown.
For a switching frequency of f_P=20kHz an efficiency of η≈ 95% is achieved for operation at the maximum admissible current amplitude of $\hat{I}_{2,max}$ ≈22A.

Due to the high modulation index, M_2=1, the rectifier stage shows relatively high conduction losses. This leads to a lower ratio of the switching and total losses of the whole VSMC as compared to the corresponding ratio of the limiting valve.

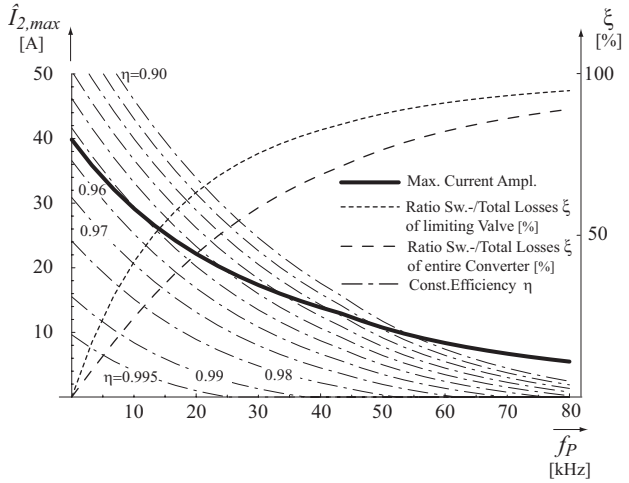


Fig.29: Limitation of output current amplitude, corresponding VSMC efficiency η and relation ξ of switching and total losses (scale on the right) for operating point 2 and T_j=120°C for all power semiconductors.

B. SiC – Technology

B.1 Operating Point 1

In **Fig.30** the limitations of the output current amplitude resulting from individual power semiconductors by limiting the maximum admissible junction temperature to T_j=120°C are depicted. For the same basic reason mentioned in connection with Fig.26 up to a switching frequency of f_P=105kHz, the cascode operating in free-wheeling diode mode (diode D_{nB}) limits the output current, for higher switching frequencies the power transistor S_{pB} is determining $\hat{I}_{2,max}$.

As the switching losses of the cascode operating as diode show only a weak dependency on the output current (cf. Fig.9) in Fig.30 the maximum current amplitude determined by D_{nB} does only slightly decrease with increasing switching frequency.

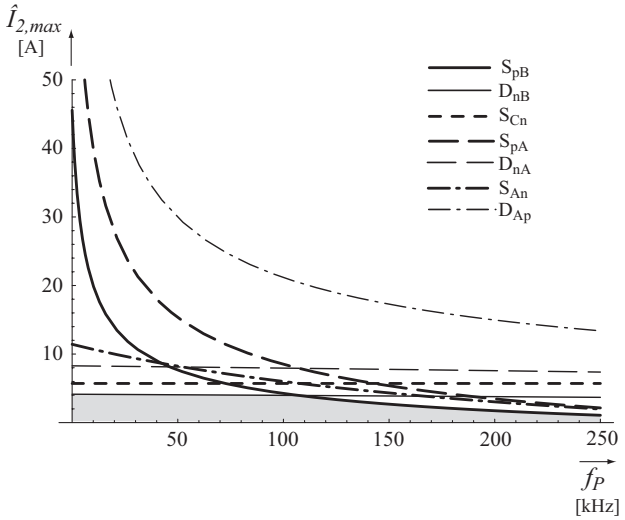


Fig.30: Limitation of the maximum admissible output current amplitude as resulting from a limitation of the junction temperature of the individual power semiconductors to T_j=120°C for operating point 1. The area highlighted in grey marks the admissible operating area

As **Fig.31** shows, e.g. for a switching frequency of f_P=150kHz, and full utilization of the thermally maximum admissible output current amplitude $\hat{I}_{2,max}$=2.6A and a total VSMC efficiency of η≈ 94% could be achieved.

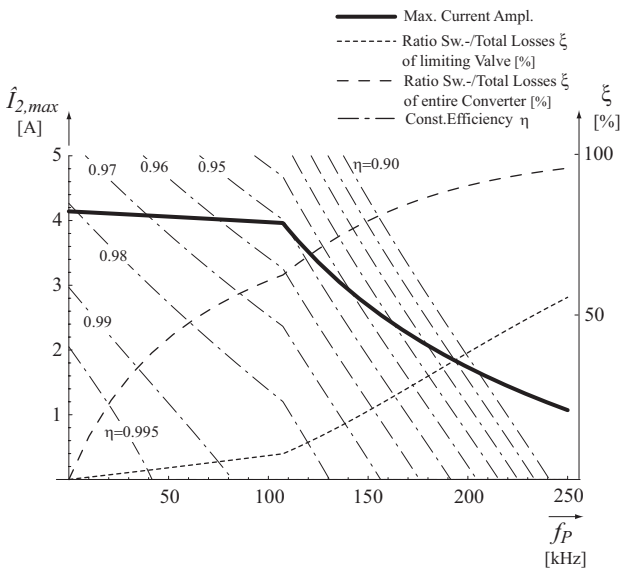


Fig.31: Thermally admissible maximum output current amplitude, corresponding efficiency η and the ratio ξ of switching and total losses (scale on the right) for the limiting valve and the whole VSMC for operating point 1 and T_j=120°C.

B.2 Operating Point 2

In this case the maximal admissible current amplitude is not determined by power losses and/or the junction temperature limitation but by the current rating of the power transistors specified in the data sheet ($I_{D,max}$ =4.5A).

According to **Fig.32** for operating the VSMC realized in SiC-technology at a switching frequency of f_P=150kHz and $\hat{I}_2$=2.6A (admissible current amplitude for operating point 1), a total conversion efficiency of η≈94.5% could be achieved.

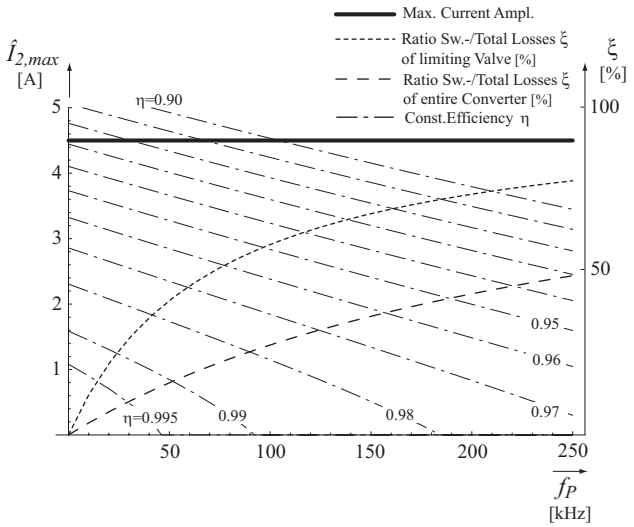


Fig.32: Admissible output current amplitude $\hat{I}_{2,max}$, corresponding efficiency η and ratio ξ of switching and total losses (scale on the right) for operating point 2 and T_j=120°C; $\hat{I}_{2,max}$ is determined by the maximum rating $I_{D,max}$=4.5A of the SiC-cascode according to the data sheet.

VII CONCLUSIONS

In this paper the stresses on the power components of a three-phase AC-AC *Very Sparse Matrix Converter* (VSMC) feeding a permanent magnet synchronous motor (PMSM) are calculated analytically for operation at zero output frequency (standstill, operating point 1) and at high output frequency (rated speed, operating point 2). As verified by simulations the analytical calculations do show a high accuracy independent of the input/output frequency ratio and therefore do provide an excellent basis for the dimensioning of the VSMC.

Two turn-off power semiconductor technologies, i.e. a Si-IGBTs/Si-ultra-fast free-wheeling diode power module and a SiC-JFET in cascode connection with a low-voltage Si-power-MOSFET are analyzed concerning the dependency of the thermally maximum admissible output current amplitude on the switching frequency for both operating points. For operation at standstill the free-wheeling diodes of the output stage are limiting the current carrying capability of the VSMC output stage and/or the torque of the PMSM to low values as known from conventional VSI drives. At high output frequencies the limitation is due to the power transistors where for the IGBTs a high utilization of the current rating given in the data sheet could be achieved in case a switching frequency of f_P≈20kHz is selected; for the SiC-cascode f_P=150kHz turns out to give a good compromise between device utilization and efficiency which in both cases is close to η≈95%. This remarkably high value does result from the fact that for the commutation strategy employed essentially no switching losses of the VSMC input stage do occur.

As proposed in Section III-A, the output stage switching losses could be partly shifted to the input stage allowing a further increase in utilization of the output stage transistors current carrying capability. A detailed analysis of this novel commutation scheme in combination with an exact switching loss measurement (cf. Section IV) considering especially the influence of parasitic capacitances which might be responsible for a considerable share of the total losses at very high switching frequencies is currently under investigation.

All results derived in this paper will in a next step be compared to a conventional matrix converter and to a cascade connection of a voltage DC link rectifier and a voltage DC link inverter employing power semiconductors of equal type. This should clearly show all advantages and drawbacks of the VSMC concept in comparison to conventional converter topologies. Furthermore, a 7.5kW VSMC will be realized in IGBT-technology for servo drive applications and a 2.5kW fully SiC *Sparse Matrix Converter* [1] employing a novel SiC-cascode switch and operating at 200kHz switching frequency will be developed for supplying a constant frequency load from a heavily frequency varying mains.

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