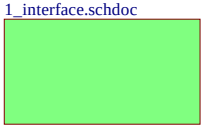
Rev	Description	Date	Author
0.1	- Initial release	01-Apr-2021	Andre M. P. Mattos

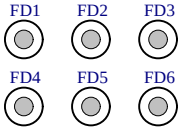
Revision History

PCB

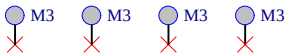
1_interface.schdoc



FIDUTIALS



MECHANICAL HOLES

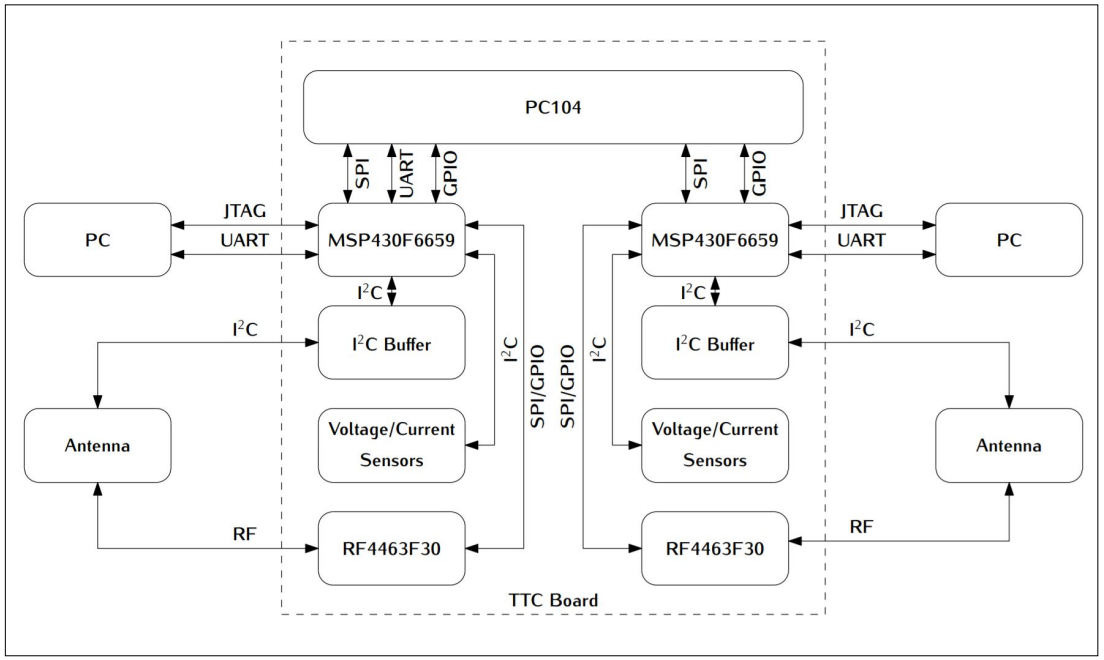


PCB Elements

OBDH2 Hardware:

- Drawn by: André M. P. Mattos
- Reviewers: Yan C. Azeredo
- Based on FloripaSat-I OBDH designed by: Sara V. Martinez
- Support: Gabriel M. Marcelino

Project Contributions

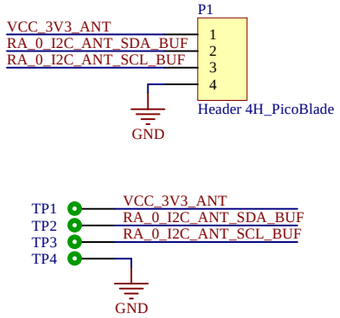


Block Diagram

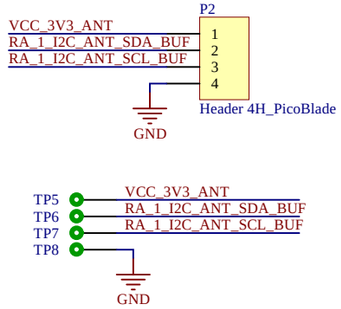
Project Information

SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Hardware Archictecture*			
Designed by: *André M. P. Mattos*			
Date: 09/04/2021	Version: *v0.1*	Sheet *0* of *6*	Size: A4

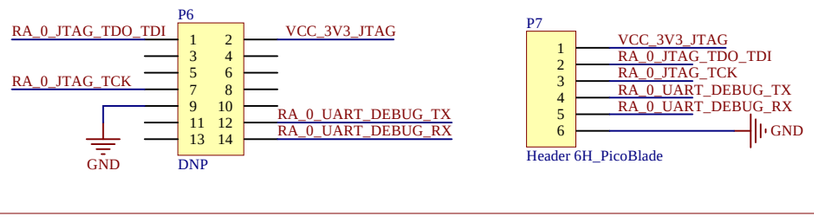
ANTENNA DEPLOYER INTERFACE (RADIO_0)



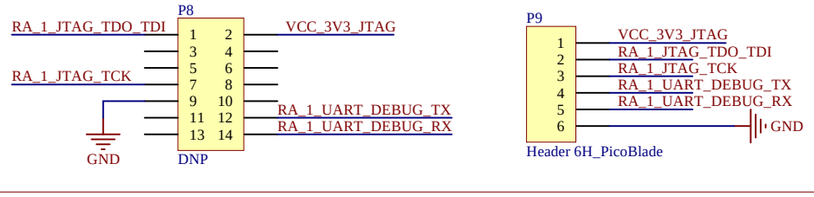
ANTENNA DEPLOYER INTERFACE (RADIO_1)



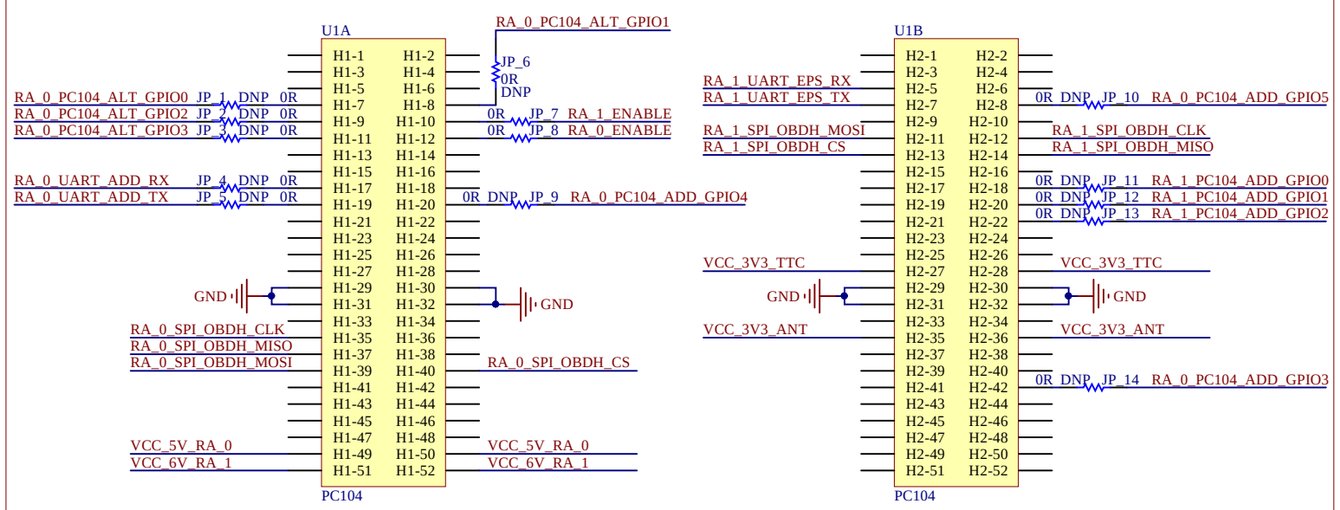
PROGRAMMING HEADERS MCU RADIO 0 (JTAG Spy Bi-Wire)



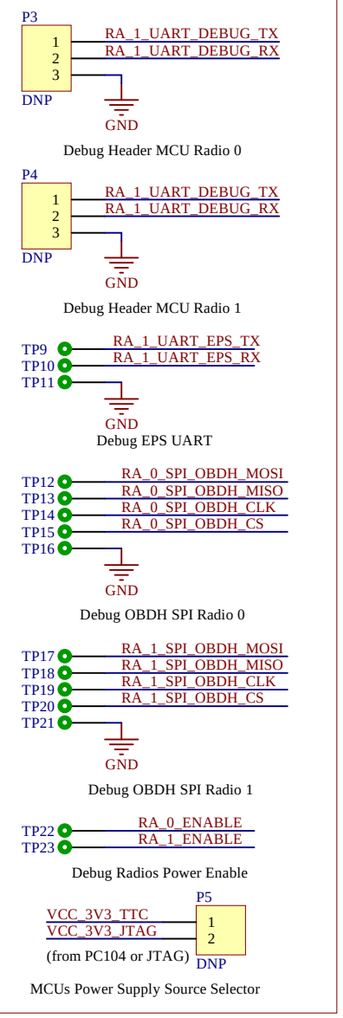
PROGRAMMING HEADERS MCU RADIO 1 (JTAG Spy Bi-Wire)

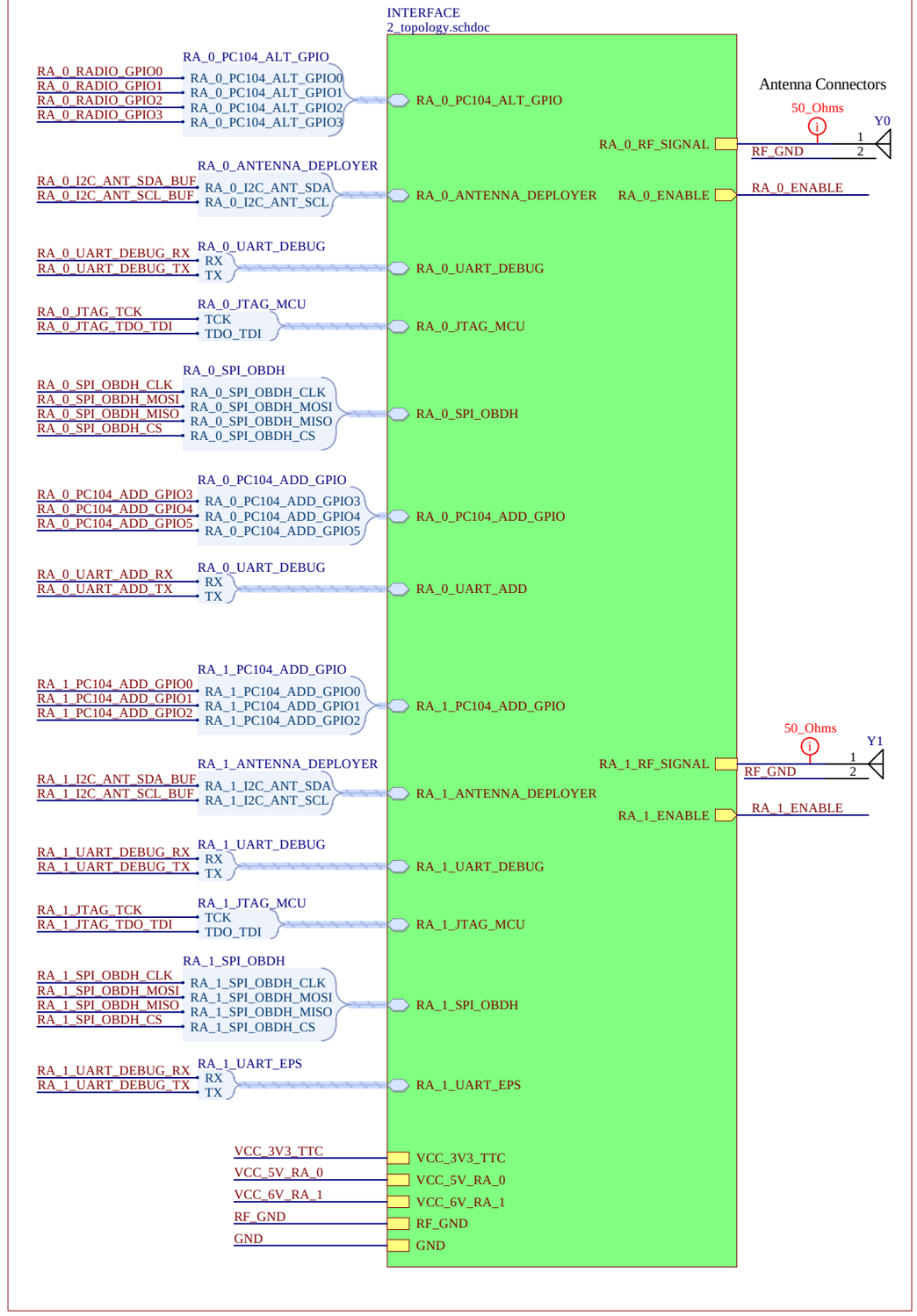


PC104 INTERFACE

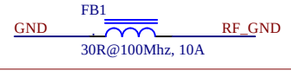


DEBUG HEADERS AND TESTPOINTS

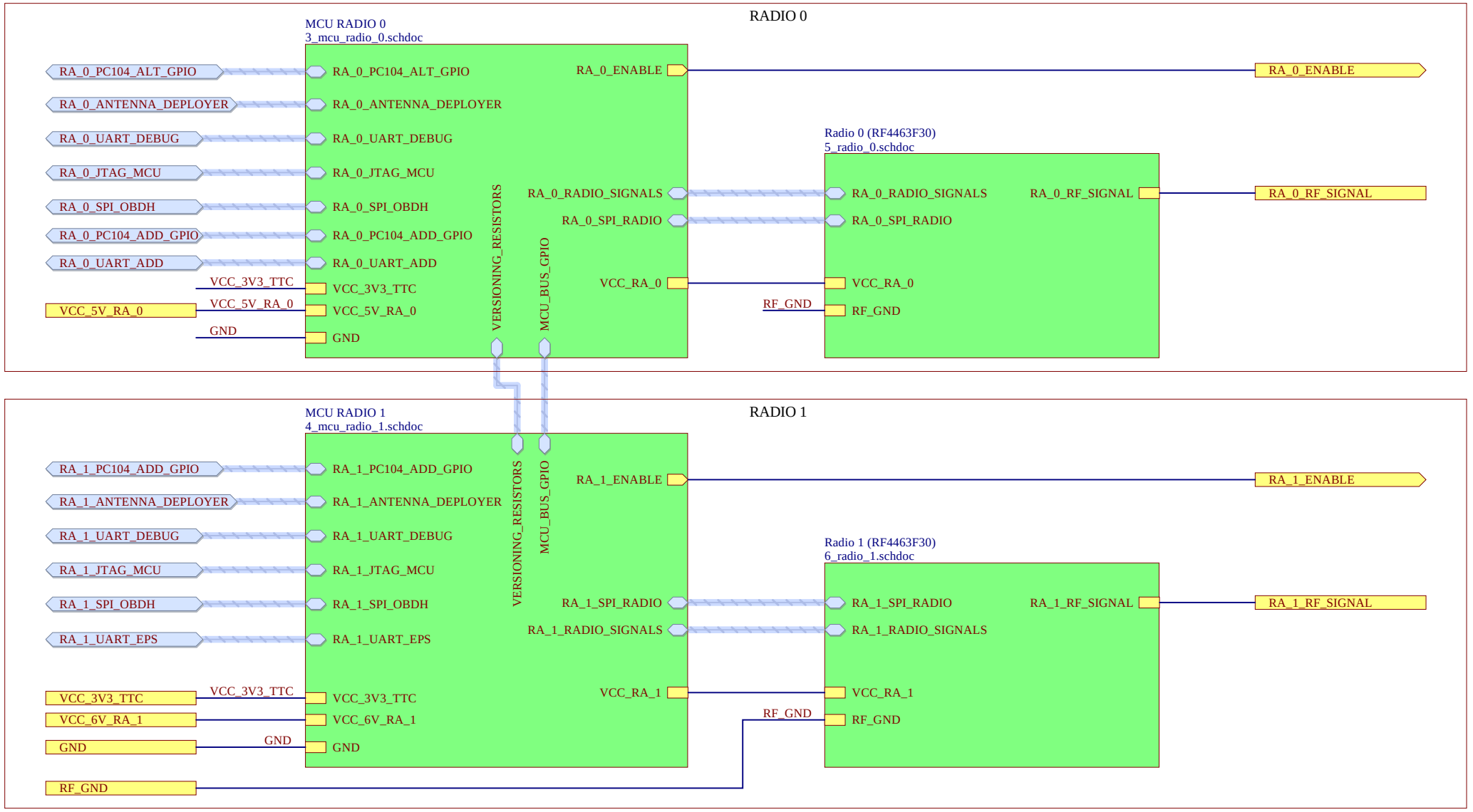




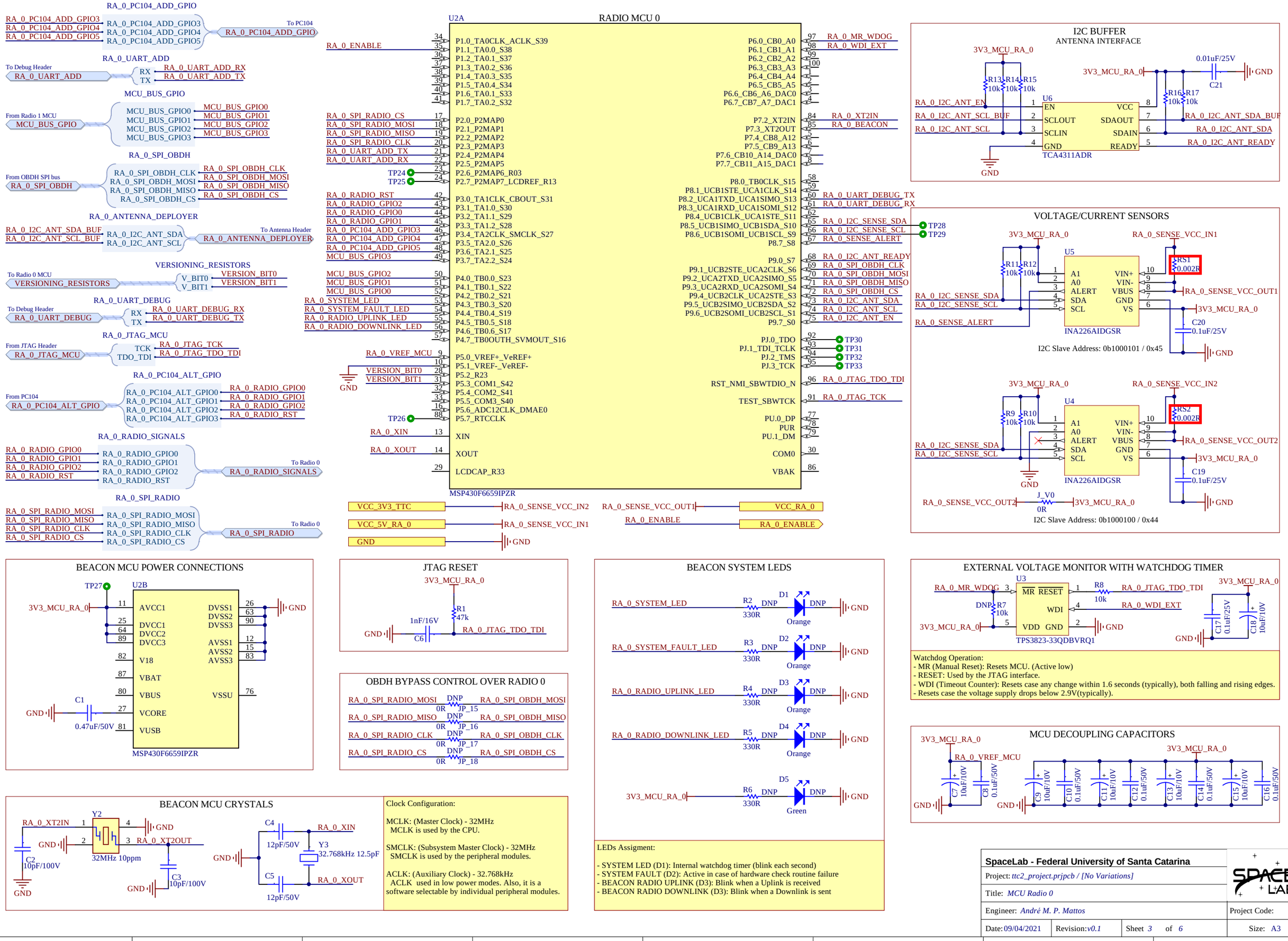
GROUNDING



SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Interface*			
Engineer: *André M. P. Mattos*			Project Code:
Date: 09/04/2021	Revision: *v0.1*	Sheet *1* of *6*	Size: A3



SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Topology*			
Designed by: *André M. P. Mattos*			Project Code:
Date: 09/04/2021	Revision: *v0.1*	Sheet *2* of *6*	Size: A4


RADIO MCU 0
U2A
MSP430F6659IPZR
RA_0_PC104_ADD_GPIO
RA_0_UART_ADD
MCU_BUS_GPIO
RA_0_SPI_OBDH
RA_0_ANTENNA_DEPLOYER
VERSIONING_RESISTORS
RA_0_UART_DEBUG
RA_0_JTAG_MCU
RA_0_PC104_ALT_GPIO
RA_0_RADIO_SIGNALS
RA_0_SPI_RADIO
I2C BUFFER
ANTENNA INTERFACE
TCA4311ADR
VOLTAGE/CURRENT SENSORS
INA226AIDGSR
I2C Slave Address: 0b1000101 / 0x45
I2C Slave Address: 0b1000100 / 0x44
BEACON MCU POWER CONNECTIONS
JTAG RESET
OBDH BYPASS CONTROL OVER RADIO 0
BEACON SYSTEM LEDS
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER
TPS3823-33QDBVRQ1
MCU DECOUPLING CAPACITORS
BEACON MCU CRYSTALS
Clock Configuration:
MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.
SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.
ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.
LEDs Assigment:
- SYSTEM LED (D1): Internal watchdog timer (blink each second)
- SYSTEM FAULT (D2): Active in case of hardware check routine failure
- BEACON RADIO UPLINK (D3): Blink when a Uplink is received
- BEACON RADIO DOWNLINK (D3): Blink when a Downlink is sent
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).
SpaceLab - Federal University of Santa Catarina
Project: ttc2_project.prjpcb / [No Variations]
Title: MCU Radio 0
Engineer: André M. P. Mattos
Project Code:
Date: 09/04/2021
Revision: v0.1
Sheet 3 of 6
Size: A3

RADIO MCU 1

U7A

MSP430F6659IPZR

RA_1_PC104_ADD_GPIO

RA_1_PC104_ADD_GPIO0
RA_1_PC104_ADD_GPIO1
RA_1_PC104_ADD_GPIO2
RA_1_PC104_ADD_GPIO0
RA_1_PC104_ADD_GPIO1
RA_1_PC104_ADD_GPIO2
To PC104
RA_1_PC104_ADD_GPIO

MCU_BUS_GPIO

From Radio 0 MCU
MCU_BUS_GPIO
MCU_BUS_GPIO0
MCU_BUS_GPIO1
MCU_BUS_GPIO2
MCU_BUS_GPIO3
MCU_BUS_GPIO0
MCU_BUS_GPIO1
MCU_BUS_GPIO2
MCU_BUS_GPIO3

RA_1_SPI_OBDH

From OBDH SPI bus
RA_1_SPI_OBDH
RA_1_SPI_OBDH_CLK
RA_1_SPI_OBDH_MOSI
RA_1_SPI_OBDH_MISO
RA_1_SPI_OBDH_CS
RA_1_SPI_OBDH_CLK
RA_1_SPI_OBDH_MOSI
RA_1_SPI_OBDH_MISO
RA_1_SPI_OBDH_CS

VERSIONING_RESISTORS

To Radio 0 MCU
VERSIONING_RESISTORS
V_BIT0
V_BIT1
VERSION_BIT0
VERSION_BIT1

RA_1_ANTENNA_DEPLOYER

RA_1_I2C_ANT_SDA_BUF
RA_1_I2C_ANT_SCL_BUF
RA_1_I2C_ANT_SDA
RA_1_I2C_ANT_SCL
To Antenna Header
RA_1_ANTENNA_DEPLOYER

RA_1_UART_EPS

To EPS (through PC104)
RA_1_UART_EPS
RX
TX
RA_1_UART_EPS_RX
RA_1_UART_EPS_TX

RA_1_UART_DEBUG

To Debug Header
RA_1_UART_DEBUG
RX
TX
RA_1_UART_DEBUG_RX
RA_1_UART_DEBUG_TX

RA_1_JTAG_MCU

From JTAG Header
RA_1_JTAG_MCU
TCK
TDO_TDI
RA_1_JTAG_TCK
RA_1_JTAG_TDO_TDI

RA_1_RADIO_SIGNALS

RA_1_RADIO_GPIO0
RA_1_RADIO_GPIO1
RA_1_RADIO_GPIO2
RA_1_RADIO_RST
RA_1_RADIO_GPIO0
RA_1_RADIO_GPIO1
RA_1_RADIO_GPIO2
RA_1_RADIO_RST
To Radio 1
RA_1_RADIO_SIGNALS

RA_1_SPI_RADIO

RA_1_SPI_RADIO_MOSI
RA_1_SPI_RADIO_MISO
RA_1_SPI_RADIO_CLK
RA_1_SPI_RADIO_CS
RA_1_SPI_RADIO_MOSI
RA_1_SPI_RADIO_MISO
RA_1_SPI_RADIO_CLK
RA_1_SPI_RADIO_CS
To Radio 1
RA_1_SPI_RADIO

RA_1_ENABLE 34
P1.0_TA0CLK_ACLK_S39
P1.1_TA0.0_S38
P1.2_TA0.1_S37
P1.3_TA0.2_S36
P1.4_TA0.3_S35
P1.5_TA0.4_S34
P1.6_TA0.1_S33
P1.7_TA0.2_S32

RA_1_SPI_RADIO_CS 17
RA_1_SPI_RADIO_MOSI 18
RA_1_SPI_RADIO_MISO 19
RA_1_SPI_RADIO_CLK 20
RA_1_UART_EPS_TX 21
RA_1_UART_EPS_RX 22
TP34 23
TP35 24
P2.0_P2MAP0
P2.1_P2MAP1
P2.2_P2MAP2
P2.3_P2MAP3
P2.4_P2MAP4
P2.5_P2MAP5
P2.6_P2MAP6_R03
P2.7_P2MAP7_LCDREF_R13

RA_1_RADIO_RST 42
RA_1_RADIO_GPIO2 43
RA_1_RADIO_GPIO0 44
RA_1_RADIO_GPIO1 45
RA_1_PC104_ADD_GPIO0 46
RA_1_PC104_ADD_GPIO1 47
RA_1_PC104_ADD_GPIO2 48
P3.0_TA1CLK_CBOUT_S31
P3.1_TA1.0_S30
P3.2_TA1.1_S29
P3.3_TA1.2_S28
P3.4_TA2CLK_SMCLK_S27
P3.5_TA2.0_S26
P3.6_TA2.1_S25
P3.7_TA2.2_S24

RA_1_SYSTEM_LED 53
RA_1_SYSTEM_FAULT_LED 54
RA_1_RADIO_UPLINK_LED 55
RA_1_RADIO_DOWNLINK_LED 56
P4.0_TB0.0_S23
P4.1_TB0.1_S22
P4.2_TB0.2_S21
P4.3_TB0.3_S20
P4.4_TB0.4_S19
P4.5_TB0.5_S18
P4.6_TB0.6_S17
P4.7_TB0OUTH_SVMOUT_S16

RA_1_VREF_MCU 9
P5.0_VREF+_VeREF+
P5.1_VREF-_VeREF-
VERSION_BIT0 28
VERSION_BIT1 31
P5.2_R23
P5.3_COM1_S42
P5.4_COM2_S41
P5.5_COM3_S40
P5.6_ADC12CLK_DMAE0
TP36 88
P5.7_RTCCLK

RA_1_XIN 13
XIN
RA_1_XOUT 14
XOUT
29
LCDCAP_R33

P6.0_CB0_A0 97
P6.1_CB1_A1 98
P6.2_CB2_A2 99
P6.3_CB3_A3 100
P6.4_CB4_A4 1
P6.5_CB5_A5 2
P6.6_CB6_A6_DAC0 3
P6.7_CB7_A7_DAC1 4

P7.2_XT2IN 84
P7.3_XT2OUT 85
P7.4_CB8_A12 5
P7.5_CB9_A13 6
P7.6_CB10_A14_DAC0 7
P7.7_CB11_A15_DAC1 8

P8.0_TB0CLK_S15 58
P8.1_UCB1STE_UCA1CLK_S14 59
P8.2_UCA1TXD_UCA1SIMO_S13 60
P8.3_UCA1RXD_UCA1SOMI_S12 61
P8.4_UCB1CLK_UCA1STE_S11 62
P8.5_UCB1SIMO_UCB1SDA_S10 65
P8.6_UCB1SOMI_UCB1SCL_S9 66
P8.7_S8 67

P9.0_S7 68
P9.1_UCB2STE_UCA2CLK_S6 69
P9.2_UCA2TXD_UCA2SIMO_S5 70
P9.3_UCA2RXD_UCA2SOMI_S4 71
P9.4_UCB2CLK_UCA2STE_S3 72
P9.5_UCB2SIMO_UCB2SDA_S2 73
P9.6_UCB2SOMI_UCB2SCL_S1 74
P9.7_S0 75

PJ.0_TDO 92
PJ.1_TDI_TCLK 93
PJ.2_TMS 94
PJ.3_TCK 95

RST_NMI_SBWTDIO_N 96
TEST_SBWTCK 91

PU.0_DP 77
PUR 78
PU.1_DM 79
COM0 30
VBAK 86

RA_1_MR_WDOG
RA_1_WDI_EXT
MCU_BUS_GPIO0
MCU_BUS_GPIO1
MCU_BUS_GPIO2
MCU_BUS_GPIO3
RA_1_XT2IN
RA_1_BEACON
RA_1_UART_DEBUG_TX
RA_1_UART_DEBUG_RX
RA_1_I2C_SENSE_SDA
RA_1_I2C_SENSE_SCL
RA_1_SENSE_ALERT
RA_1_I2C_ANT_READY
RA_1_SPI_OBDH_CLK
RA_1_SPI_OBDH_MOSI
RA_1_SPI_OBDH_MISO
RA_1_SPI_OBDH_CS
RA_1_I2C_ANT_SDA
RA_1_I2C_ANT_SCL
RA_1_I2C_ANT_EN
TP37
TP38
TP39
TP40
TP41
TP42
RA_1_JTAG_TDO_TDI
RA_1_JTAG_TCK

VCC_3V3_TTC → RA_1_SENSE_VCC_IN2
VCC_6V_RA_1 → RA_1_SENSE_VCC_IN1
GND → GND
RA_1_SENSE_VCC_OUT1 → VCC_RA_1
RA_1_ENABLE → RA_1_ENABLE

I2C BUFFER
ANTENNA INTERFACE

3V3_MCU_RA_1
R29 10k
R30 10k
R31 10k
0.01uF/25V
C42
GND
U11
EN
SCLOUT
SCLIN
GND
VCC
SDAOUT
SDAIN
READY
TCA4311ADR
R32 10k
R33 10k
RA_1_I2C_ANT_EN
RA_1_I2C_ANT_SCL_BUF
RA_1_I2C_ANT_SCL
RA_1_I2C_ANT_SDA_BUF
RA_1_I2C_ANT_SDA
RA_1_I2C_ANT_READY

VOLTAGE/CURRENT SENSORS

3V3_MCU_RA_1
R27 10k
R28 10k
U10
A1
A0
ALERT
SDA
SCL
VIN+
VIN-
VBUS
GND
VS
INA226AIDGSR
RS3 0.002R
RA_1_SENSE_VCC_IN1
RA_1_SENSE_VCC_OUT1
RA_1_I2C_SENSE_SDA
RA_1_I2C_SENSE_SCL
RA_1_SENSE_ALERT
3V3_MCU_RA_1
C41 0.1uF/25V
GND
I2C Slave Address: 0b1000101 / 0x45

3V3_MCU_RA_1
R25 10k
R26 10k
U9
INA226AIDGSR
RS4 0.002R
RA_1_SENSE_VCC_IN2
RA_1_SENSE_VCC_OUT2
RA_1_I2C_SENSE_SDA
RA_1_I2C_SENSE_SCL
3V3_MCU_RA_1
C40 0.1uF/25V
GND
J_V1
0R
RA_1_SENSE_VCC_OUT2
3V3_MCU_RA_1
I2C Slave Address: 0b1000100 / 0x44

BEACON MCU POWER CONNECTIONS

TP43
U7B
3V3_MCU_RA_1
AVCC1
DVCC1
DVCC2
DVCC3
V18
VBAT
VBUS
VCORE
VUSB
DVSS1
DVSS2
DVSS3
AVSS1
AVSS2
AVSS3
VSSU
C27
0.47uF/50V
GND
MSP430F6659IPZR

JTAG AND VERSIONING COMPONENTS

3V3_MCU_RA_1
R18 47k
C26 1nF/16V
RA_1_JTAG_TDO_TDI
V1 47k
V2 DNP 47k
V3 47k
V4 DNP 47k
VERSION_BIT0
VERSION_BIT1
GND
Configuration for version v0.1

BEACON SYSTEM LEDS

RA_1_SYSTEM_LED
RA_1_SYSTEM_FAULT_LED
RA_1_RADIO_UPLINK_LED
RA_1_RADIO_DOWNLINK_LED
3V3_MCU_RA_1
R19 DNP 330R
R20 DNP 330R
R21 DNP 330R
R22 DNP 330R
R23 DNP 330R
D6 DNP Orange
D7 DNP Orange
D8 DNP Orange
D9 DNP Orange
D10 DNP Green
GND

LEDs Assigment:

- SYSTEM LED (D1): Internal watchdog timer (blink each second)
- SYSTEM FAULT (D2): Active in case of hardware check routine failure
- BEACON RADIO UPLINK (D3): Blink when a Uplink is received
- BEACON RADIO DOWNLINK (D3): Blink when a Downlink is sent

EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER

U8
RA_1_MR_WDOG
DNP R34 10k
3V3_MCU_RA_1
MR
RESET
WDI
VDD
GND
R24 10k
RA_1_JTAG_TDO_TDI
RA_1_WDI_EXT
TPS3823-33QDBVRQ1
C38 0.1uF/25V
C39 10uF/10V

Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).

BEACON MCU CRYSTALS

Y4
RA_1_XT2IN
RA_1_XT2OUT
32MHz 10ppm
C22 10pF/100V
C23 10pF/100V
GND
C24 12pF/50V
C25 12pF/50V
RA_1_XIN
RA_1_XOUT
Y5 32.768kHz 12.5pF

Clock Configuration:

MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.

SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.

ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.

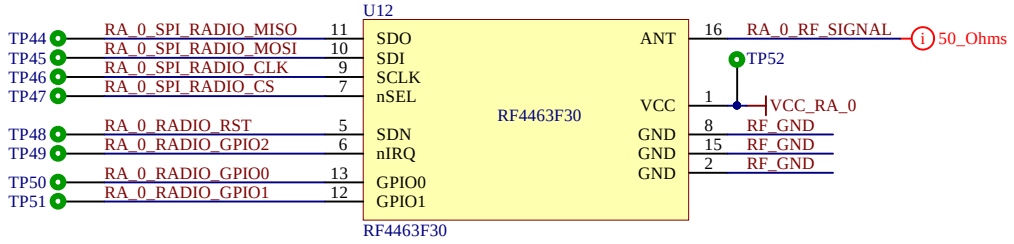
MCU DECOUPLING CAPACITORS

3V3_MCU_RA_1
RA_1_VREF_MCU
C28 10uF/10V
C29 0.1uF/50V
C30 10uF/10V
C31 0.1uF/50V
C32 10uF/10V
C33 0.1uF/50V
C34 10uF/10V
C35 0.1uF/50V
C36 10uF/10V
C37 0.1uF/50V
GND

SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *MCU Radio 1*			
Engineer: *André M. P. Mattos*			Project Code:
Date: 09/04/2021	Revision: *v0.1*	Sheet *4* of *6*	Size: A3

RADIO 0 (TRANSCEIVER)

Notes:
nIRQ - Interrupt output
GPIO0/1 - Si4463 GPIOs
SDN - Power down control
(SDN=1, power down)



NiceRF RF4463F30 transceiver module:
- Based on the Si4463/61/60-C transceiver
- Antenna matching network and two-way switch control
- 3.3-6.5 V Power supply
- Receiving current: 15mA
- Transmitting current: 500mA (at VCC=5V and TX=30dBm)
- Typical output power: +30dBm (at 433MHz and VCC=5V)
- Sensitivity up to -126 dBm (at 433MHz and Data rate=600bps)
- Operating Temperature Range:-40 + 85 °C

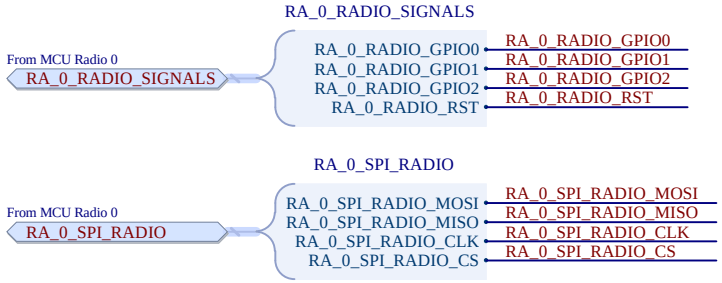
- Frequency Range: 315/433/490/868/915 (Customizable 142-1050MHz)
- Modulation: (G)FSK,4(G)FSK,(G)MSK,OOK and ASK
- Data transfer rate: 0.1-1000Kbps
- TX/RX FIFO: 64/128Byte data register

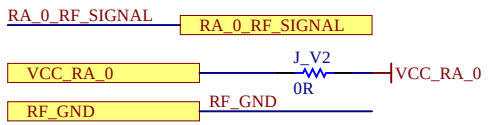
FloripaSat-1 Configuration:
Customization:
- Center Frequency: 433Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 2.4Kbps
- Input voltage: 5V
- Maximum output power: +30dBm
- Transmitting current: 500mA
- Receiving current (always on): 15mA
- Modulation: GFSK

FloripaSat-2 Configuration:
Customization:
- Center Frequency: 450Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 4.8Kbps
- Input voltage: 5V
- Maximum output power: +30dBm
- Transmitting current: 500mA
- Receiving current (always on): 15mA
- Modulation: GMSK

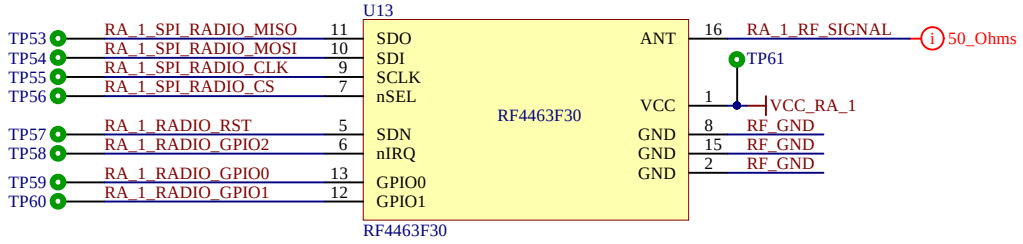




SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Radio 0*			
Designed by: *André M. P. Mattos*			Project Code:
Date: 09/04/2021	Revision: *v0.1*	Sheet *5* of *6*	Size: A4

RADIO 1 (TRANSCEIVER)

Notes:
nIRQ - Interrupt output
GPIO0/1 - Si4463 GPIOs
SDN - Power down control
(SDN=1, power down)



NiceRF RF4463F30 transceiver module:
- Based on the Si4463/61/60-C transceiver
- Antenna matching network and two-way switch control
- 3.3-6.5 V Power supply
- Receiving current: 15mA
- Transmitting current: 500mA (at VCC=5V and TX=30dBm)
- Typical output power: +30dBm (at 433MHz and VCC=5V)
- Sensitivity up to -126 dBm (at 433MHz and Data rate=600bps)
- Operating Temperature Range:-40 + 85 °C

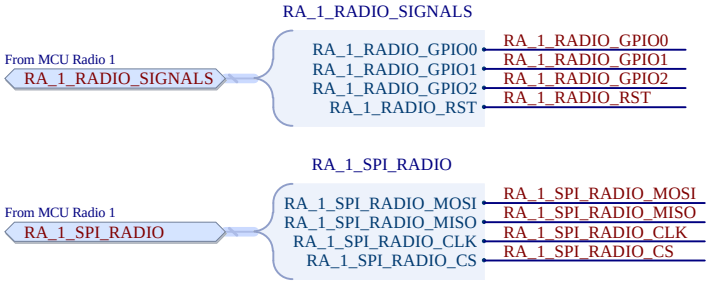
- Frequency Range: 315/433/490/868/915 (Customizable 142-1050MHz)
- Modulation: (G)FSK,4(G)FSK,(G)MSK,OOK and ASK
- Data transfer rate: 0.1-1000Kbps
- TX/RX FIFO: 64/128Byte data register

FloripaSat-1 Configuration:
Customization:
- Center Frequency: 160Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 1.2Kbps
- Input voltage: 5V
- Output power: +28.6dBm
- Transmitting current: 500mA
- Receiving current (always on): 15mA
- Modulation: GFSK

FloripaSat-2 Configuration:
Customization:
- Center Frequency: 160Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 1.2Kbps
- Input voltage: 6V
- Maximum output power: +30dBm
- Transmitting current: 550mA
- Receiving current (always on): 15mA
- Modulation: GMSK



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Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Radio 1*			
Designed by: *André M. P. Mattos*			Project Code:
Date: 09/04/2021	Revision: *v0.1*	Sheet *6* of *6*	Size: A4