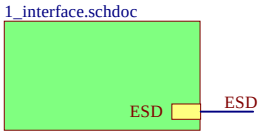
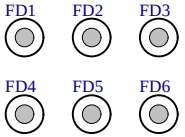
Rev	Description	Date	Author
0.1	- Initial release	01-Apr-2021	Andre M. P. Mattos

Revision History

PCB



FIDUTIALS



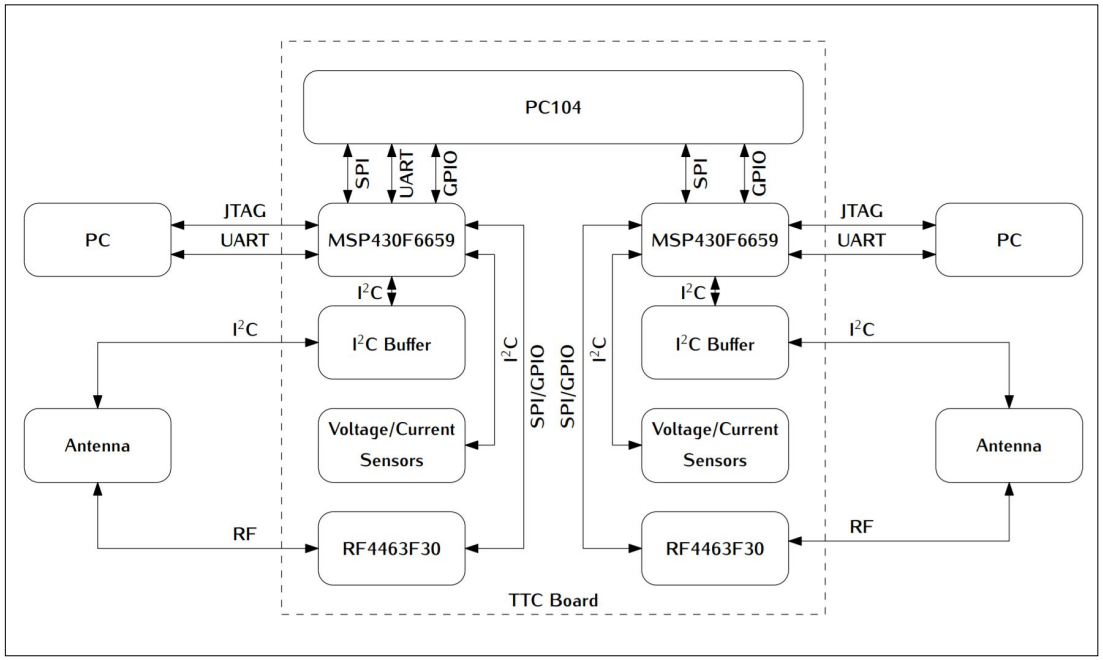
MECHANICAL HOLES

PCB Elements

TTC2 Hardware:

- Drawn by: André M. P. Mattos
- Reviewers: Yan C. Azeredo
- Based on FloripaSat-I TTC designed by: Sara V. Martinez
- Support: Gabriel M. Marcelino

Project Contributions



Block Diagram

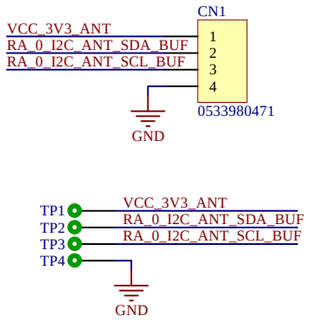
Github repository: https://github.com/spacelab-ufsc/ttc2

More info about SpaceLab: https://spacelab.ufsc.br/

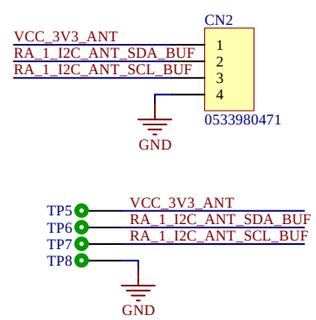
Project Information

SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Hardware Archictecture*			
Designed by: *André M. P. Mattos*			Project Code: *TTC2*
Date: 15/04/2021	Revision: *v0.1*	Sheet *0* of *6*	Size: A4

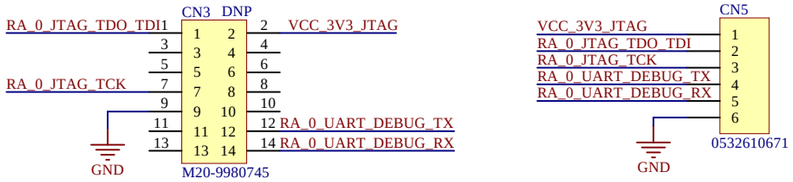
ANTENNA DEPLOYER INTERFACE (RADIO_0)
Picoblade Connector and debug testpoints



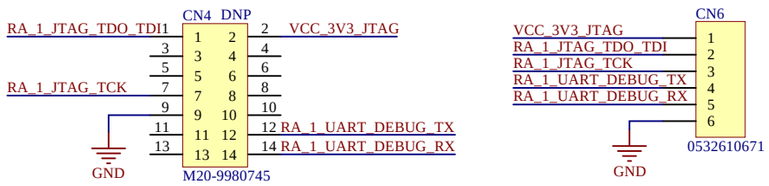
ANTENNA DEPLOYER INTERFACE (RADIO_1)



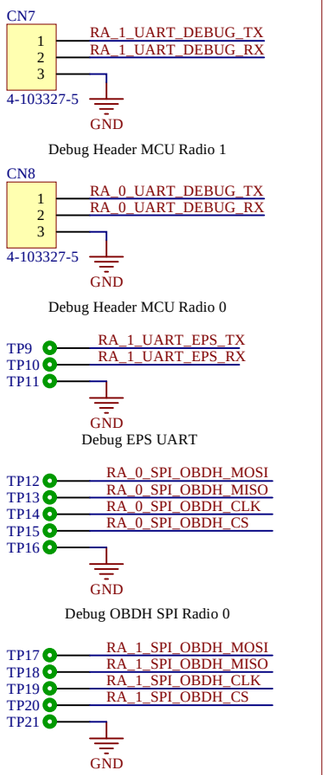
PROGRAMMING HEADERS MCU RADIO 0
(JTAG Spy Bi-Wire)



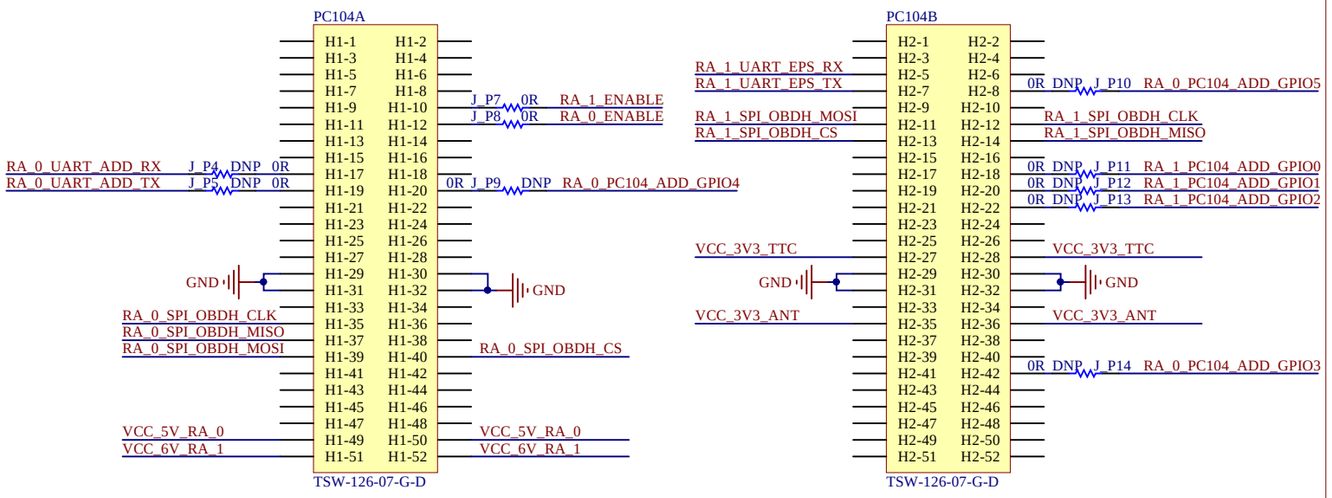
PROGRAMMING HEADERS MCU RADIO 1
(JTAG Spy Bi-Wire)



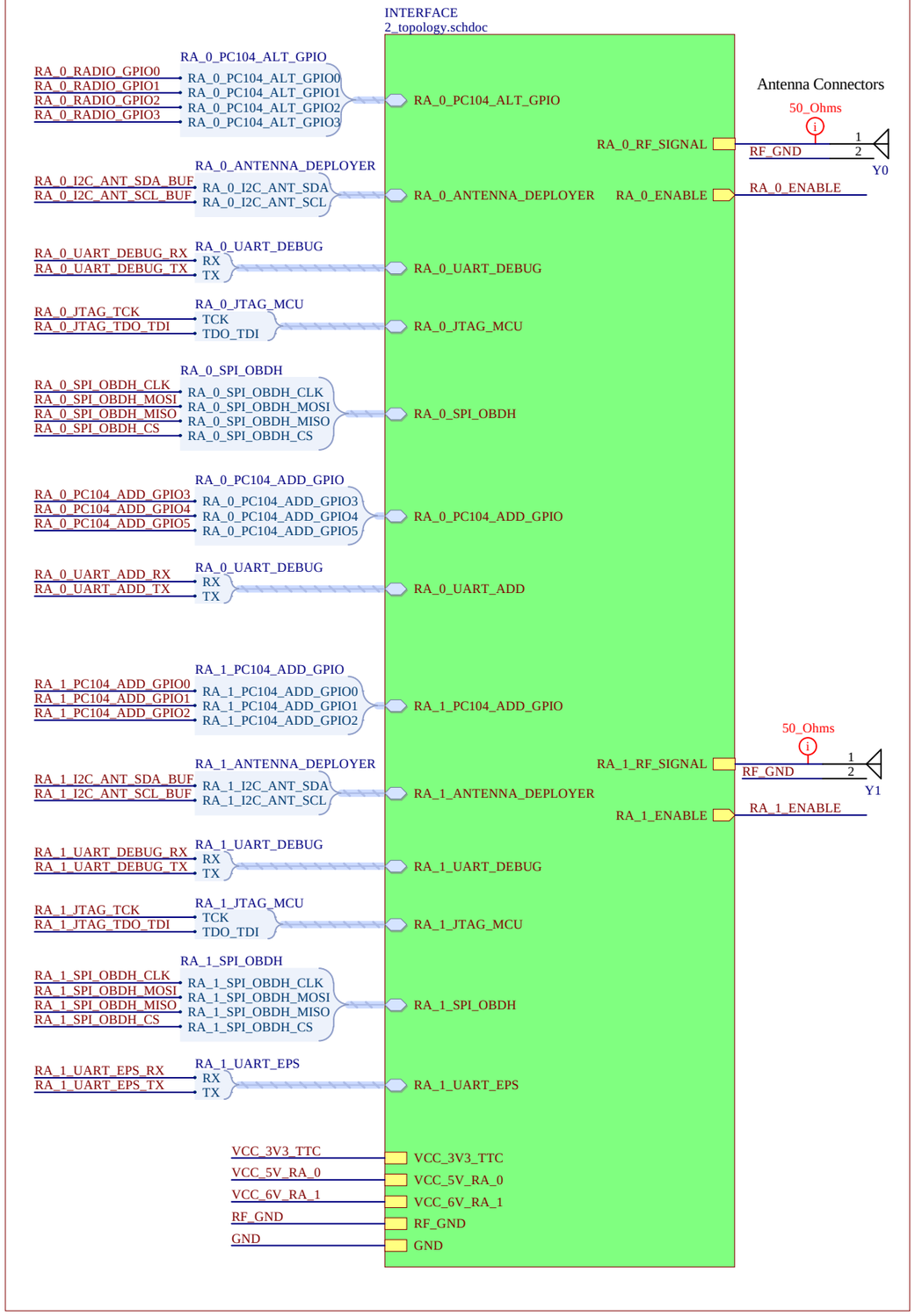
DEBUG HEADERS AND TESTPOINTS



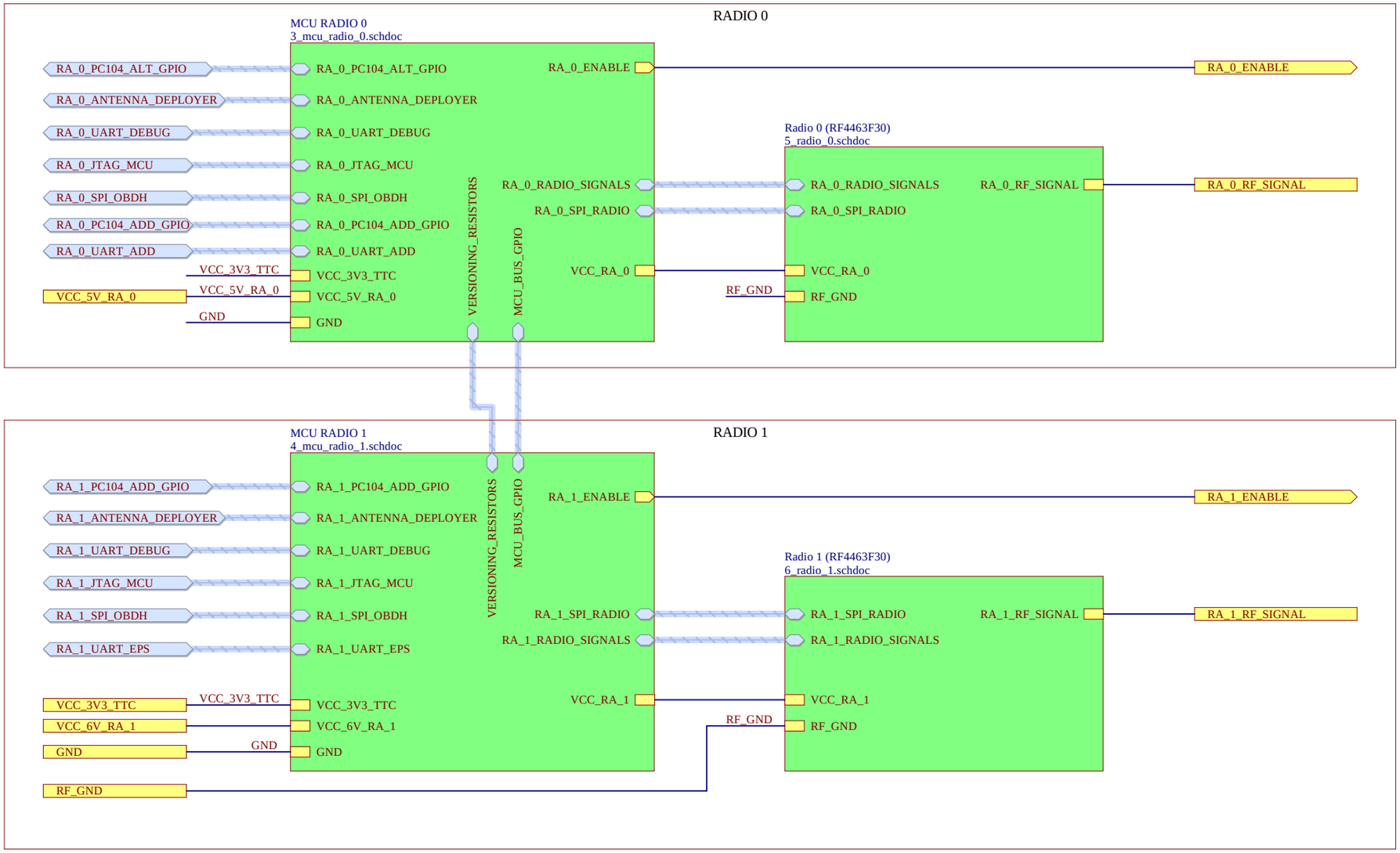
PC104 INTERFACE



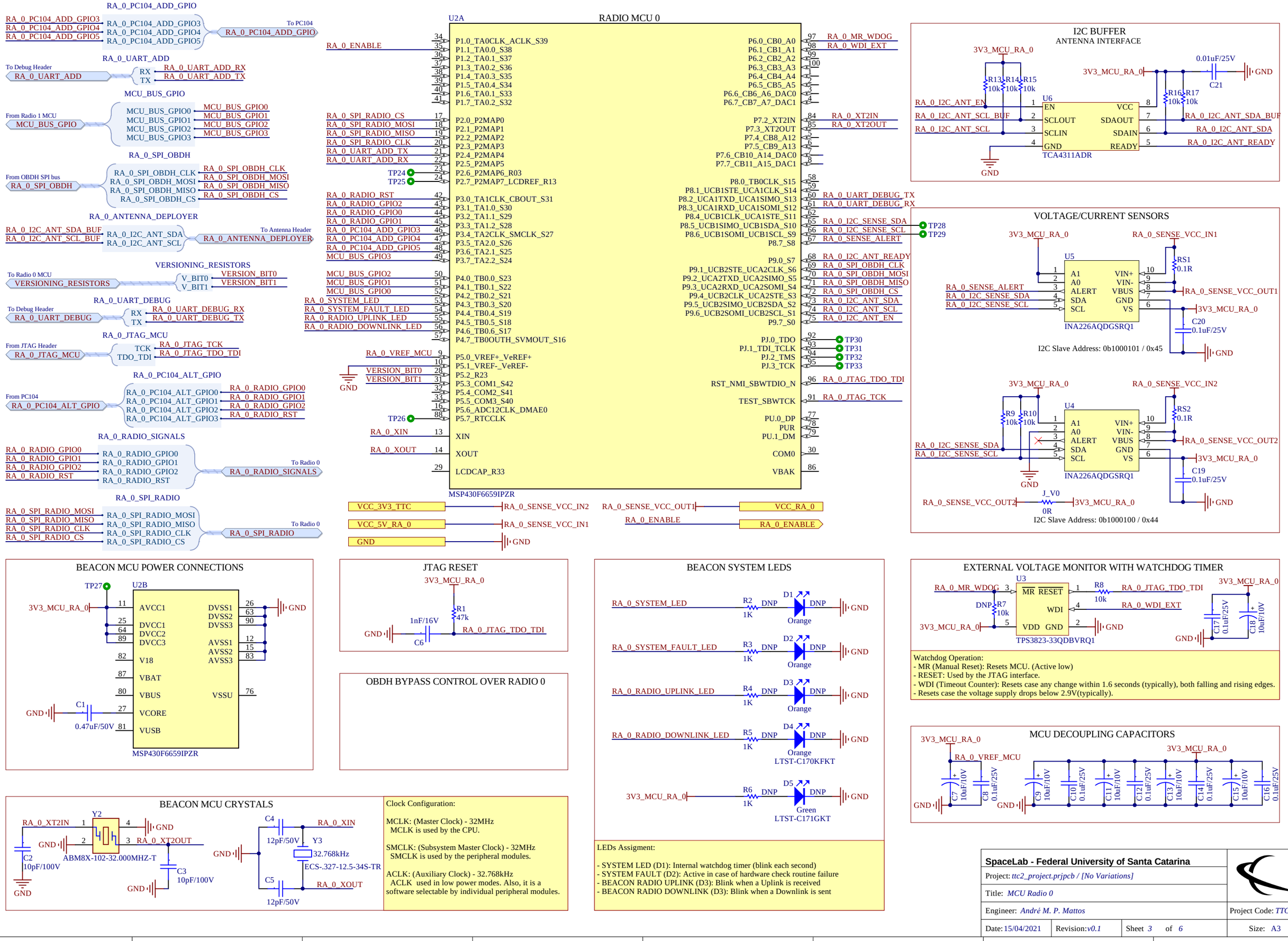
GROUNDING



SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Interface*			
Engineer: *André M. P. Mattos*			Project Code: *TTC2*
Date: 15/04/2021	Revision: *v0.1*	Sheet *1* of *6*	Size: A3



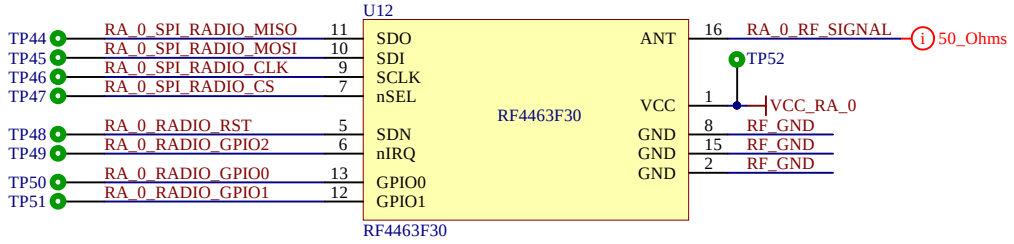
SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Topology*			
Engineer: *André M. P. Mattos*			Project Code: *TTC2*
Date: 15/04/2021	Revision: *v0.1*	Sheet *2* of *6*	Size: A3


RADIO MCU 0
U2A
MSP430F6659IPZR
RA_0_PC104_ADD_GPIO
RA_0_UART_ADD
MCU_BUS_GPIO
RA_0_SPI_OBDH
RA_0_ANTENNA_DEPLOYER
VERSIONING_RESISTORS
RA_0_UART_DEBUG
RA_0_JTAG_MCU
RA_0_PC104_ALT_GPIO
RA_0_RADIO_SIGNALS
RA_0_SPI_RADIO
To PC104
To Radio 0
To Antenna Header
From Radio 1 MCU
From OBDH SPI bus
From JTAG Header
From PC104
To Debug Header
I2C BUFFER
ANTENNA INTERFACE
VOLTAGE/CURRENT SENSORS
I2C Slave Address: 0b1000101 / 0x45
I2C Slave Address: 0b1000100 / 0x44
INA226AQDGSRQ1
TCA4311ADR
BEACON MCU POWER CONNECTIONS
JTAG RESET
OBDH BYPASS CONTROL OVER RADIO 0
BEACON SYSTEM LEDS
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER
TPS3823-33QDBVRQ1
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).
MCU DECOUPLING CAPACITORS
BEACON MCU CRYSTALS
Clock Configuration:
MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.
SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.
ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.
LEDs Assigment:
- SYSTEM LED (D1): Internal watchdog timer (blink each second)
- SYSTEM FAULT (D2): Active in case of hardware check routine failure
- BEACON RADIO UPLINK (D3): Blink when a Uplink is received
- BEACON RADIO DOWNLINK (D3): Blink when a Downlink is sent
SpaceLab - Federal University of Santa Catarina
Project: ttc2_project.prjpcb / [No Variations]
Title: MCU Radio 0
Engineer: André M. P. Mattos
Project Code: TTC2
Date: 15/04/2021
Revision: v0.1
Sheet 3 of 6
Size: A3

RADIO MCU 1
U7A
MSP430F6659IPZR
P1.0_TA0CLK_ACLK_S39
P1.1_TA0.0_S38
P1.2_TA0.1_S37
P1.3_TA0.2_S36
P1.4_TA0.3_S35
P1.5_TA0.4_S34
P1.6_TA0.1_S33
P1.7_TA0.2_S32
P2.0_P2MAP0
P2.1_P2MAP1
P2.2_P2MAP2
P2.3_P2MAP3
P2.4_P2MAP4
P2.5_P2MAP5
P2.6_P2MAP6_R03
P2.7_P2MAP7_LCDREF_R13
P3.0_TA1CLK_CBOUT_S31
P3.1_TA1.0_S30
P3.2_TA1.1_S29
P3.3_TA1.2_S28
P3.4_TA2CLK_SMCLK_S27
P3.5_TA2.0_S26
P3.6_TA2.1_S25
P3.7_TA2.2_S24
P4.0_TB0.0_S23
P4.1_TB0.1_S22
P4.2_TB0.2_S21
P4.3_TB0.3_S20
P4.4_TB0.4_S19
P4.5_TB0.5_S18
P4.6_TB0.6_S17
P4.7_TB0OUTH_SVMOUT_S16
P5.0_VREF+_VeREF+
P5.1_VREF-_VeREF-
P5.2_R23
P5.3_COM1_S42
P5.4_COM2_S41
P5.5_COM3_S40
P5.6_ADC12CLK_DMAE0
P5.7_RTCCLK
XIN
XOUT
LCDCAP_R33
P6.0_CB0_A0
P6.1_CB1_A1
P6.2_CB2_A2
P6.3_CB3_A3
P6.4_CB4_A4
P6.5_CB5_A5
P6.6_CB6_A6_DAC0
P6.7_CB7_A7_DAC1
P7.2_XT2IN
P7.3_XT2OUT
P7.4_CB8_A12
P7.5_CB9_A13
P7.6_CB10_A14_DAC0
P7.7_CB11_A15_DAC1
P8.0_TB0CLK_S15
P8.1_UCB1STE_UCA1CLK_S14
P8.2_UCA1TXD_UCA1SIMO_S13
P8.3_UCA1RXD_UCA1SOMI_S12
P8.4_UCB1CLK_UCA1STE_S11
P8.5_UCB1SIMO_UCB1SDA_S10
P8.6_UCB1SOMI_UCB1SCL_S9
P8.7_S8
P9.0_S7
P9.1_UCB2STE_UCA2CLK_S6
P9.2_UCA2TXD_UCA2SIMO_S5
P9.3_UCA2RXD_UCA2SOMI_S4
P9.4_UCB2CLK_UCA2STE_S3
P9.5_UCB2SIMO_UCB2SDA_S2
P9.6_UCB2SOMI_UCB2SCL_S1
P9.7_S0
PJ.0_TDO
PJ.1_TDI_TCLK
PJ.2_TMS
PJ.3_TCK
RST_NMI_SBWTDIO_N
TEST_SBWTCK
PU.0_DP
PUR
PU.1_DM
COM0
VBAK
RA_1_ENABLE
RA_1_SPI_RADIO_CS
RA_1_SPI_RADIO_MOSI
RA_1_SPI_RADIO_MISO
RA_1_SPI_RADIO_CLK
RA_1_UART_EPS_TX
RA_1_UART_EPS_RX
TP34
TP35
RA_1_RADIO_RST
RA_1_RADIO_GPIO2
RA_1_RADIO_GPIO0
RA_1_RADIO_GPIO1
RA_1_PC104_ADD_GPIO2
RA_1_PC104_ADD_GPIO1
RA_1_PC104_ADD_GPIO0
RA_1_SYSTEM_LED
RA_1_SYSTEM_FAULT_LED
RA_1_RADIO_UPLINK_LED
RA_1_RADIO_DOWNLINK_LED
RA_1_VREF_MCU
VERSION_BIT0
VERSION_BIT1
GND
TP36
RA_1_XIN
RA_1_XOUT
RA_1_MR_WDOG
RA_1_WDI_EXT
MCU_BUS_GPIO0
MCU_BUS_GPIO1
MCU_BUS_GPIO2
MCU_BUS_GPIO3
RA_1_XT2IN
RA_1_XT2OUT
RA_1_UART_DEBUG_TX
RA_1_UART_DEBUG_RX
RA_1_I2C_SENSE_SDA
RA_1_I2C_SENSE_SCL
RA_1_SENSE_ALERT
TP38
TP39
RA_1_I2C_ANT_READY
RA_1_SPI_OBDH_CLK
RA_1_SPI_OBDH_MOSI
RA_1_SPI_OBDH_MISO
RA_1_SPI_OBDH_CS
RA_1_I2C_ANT_SDA
RA_1_I2C_ANT_EN
RA_1_I2C_ANT_SCL
TP40
TP41
TP42
TP43
RA_1_JTAG_TDO_TDI
RA_1_JTAG_TCK
RA_1_I2C_ANT_EN
RA_1_I2C_ANT_EN
RA_1_PC104_ADD_GPIO
To PC104
RA_1_ANTENNA_DEPLOYER
To Antenna Header
RA_1_UART_EPS
To EPS (through PC104)
RA_1_UART_DEBUG
To Debug Header
RA_1_JTAG_MCU
From JTAG Header
RA_1_RADIO_SIGNALS
To Radio 1
RA_1_SPI_RADIO
To Radio 1
MCU_BUS_GPIO
From Radio 0 MCU
RA_1_SPI_OBDH
From OBDH SPI bus
VERSIONING_RESISTORS
To Radio 0 MCU
VCC_3V3_TTC
VCC_6V_RA_1
GND
RA_1_SENSE_VCC_IN2
RA_1_SENSE_VCC_IN1
RA_1_SENSE_VCC_OUT1
VCC_RA_1
RA_1_ENABLE
I2C BUFFER
ANTENNA INTERFACE
3V3_MCU_RA_1
R30 10k
R31 10k
R32 10k
R33 10k
R34 10k
0.01uF/25V
C50
U11
EN
SCLOUT
SCLIN
GND
VCC
SDAOUT
SDAIN
READY
TCA4311ADR
RA_1_I2C_ANT_SDA_BUF
RA_1_I2C_ANT_SCL_BUF
VOLTAGE/CURRENT SENSORS
U10
A1
A0
ALERT
SDA
SCL
VIN+
VIN-
VBUS
VS
INA226AQDGSRQ1
RS3 0.1R
C49 0.1uF/25V
I2C Slave Address: 0b1000101 / 0x45
U9
RS4 0.1R
C48 0.1uF/25V
J_V1
0R
I2C Slave Address: 0b1000100 / 0x44
BEACON MCU POWER CONNECTIONS
U7B
AVCC1
DVCC1
DVCC2
DVCC3
V18
VBAT
VBUS
VCORE
VUSB
DVSS1
DVSS2
DVSS3
AVSS1
AVSS2
AVSS3
VSSU
C30
0.47uF/50V
JTAG AND VERSIONING COMPONENTS
R18 47k
1nF/16V
C35
V1
V2 DNP
V3
V4 DNP
47k
Configuration for version v0.1
BEACON SYSTEM LEDS
D6
D7
D8
D9
D10
R19 DNP 1K
R20 DNP 1K
R21 DNP 1K
R22 DNP 1K
R23 DNP 1K
DNP
Orange
Green
LTST-C170KFKT
LTST-C171GKT
LEDs Assigment:
- SYSTEM LED (D1): Internal watchdog timer (blink each second)
- SYSTEM FAULT (D2): Active in case of hardware check routine failure
- BEACON RADIO UPLINK (D3): Blink when a Uplink is received
- BEACON RADIO DOWNLINK (D3): Blink when a Downlink is sent
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER
U8
MR
RESET
WDI
VDD
TPS3823-33QDBVRQ1
R24 10k
R25 10k
C46 0.1uF/25V
C47 10uF/10V
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).
MCU DECOUPLING CAPACITORS
C36 10uF/10V
C37 0.1uF/25V
C38 10uF/10V
C39 0.1uF/25V
C40 10uF/10V
C41 0.1uF/25V
C42 10uF/10V
C43 0.1uF/25V
C44 10uF/10V
C45 0.1uF/25V
BEACON MCU CRYSTALS
Y4
ABM8X-102-32.000MHZ-T
C31 10pF/100V
C32 10pF/100V
Y5
ECS-.327-12.5-34S-TR
C33 12pF/50V
C34 12pF/50V
Clock Configuration:
MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.
SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.
ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.
SpaceLab - Federal University of Santa Catarina
Project: ttc2_project.prjpcb / [No Variations]
Title: MCU Radio 1
Engineer: André M. P. Mattos
Project Code: TTC2
Date: 15/04/2021
Revision: v0.1
Sheet 4 of 6
Size: A3

RADIO 0 (TRANSCEIVER)

Notes:
nIRQ - Interrupt output
GPIO0/1 - Si4463 GPIOs
SDN - Power down control
(SDN=1, power down)



NiceRF RF4463F30 transceiver module:
- Based on the Si4463/61/60-C transceiver
- Antenna matching network and two-way switch control
- 3.3-6.5 V Power supply
- Receiving current: 15mA
- Transmitting current: 500mA (at VCC=5V and TX=30dBm)
- Typical output power: +30dBm (at 433MHz and VCC=5V)
- Sensitivity up to -126 dBm (at 433MHz and Data rate=600bps)
- Operating Temperature Range:-40 + 85 °C

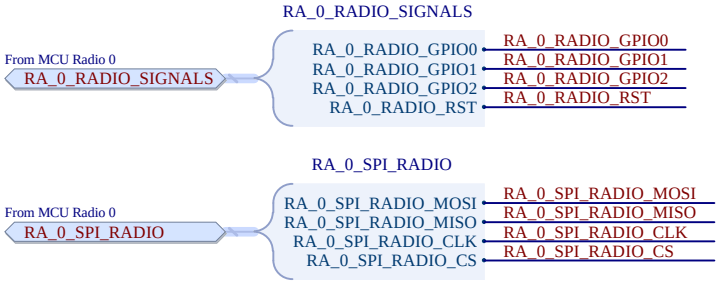
- Frequency Range: 315/433/490/868/915 (Customizable 142-1050MHz)
- Modulation: (G)FSK,4(G)FSK,(G)MSK,OOK and ASK
- Data transfer rate: 0.1-1000Kbps
- TX/RX FIFO: 64/128Byte data register

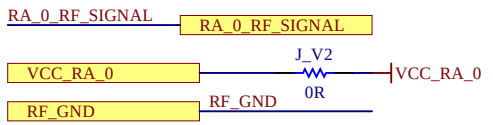
FloripaSat-1 Configuration:
Customization:
- Center Frequency: 433Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 2.4Kbps
- Input voltage: 5V
- Maximum output power: +30dBm
- Transmitting current: 500mA
- Receiving current (always on): 15mA
- Modulation: GFSK

FloripaSat-2 Configuration:
Customization:
- Center Frequency: 450Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 4.8Kbps
- Input voltage: 5V
- Maximum output power: +30dBm
- Transmitting current: 500mA
- Receiving current (always on): 15mA
- Modulation: GMSK

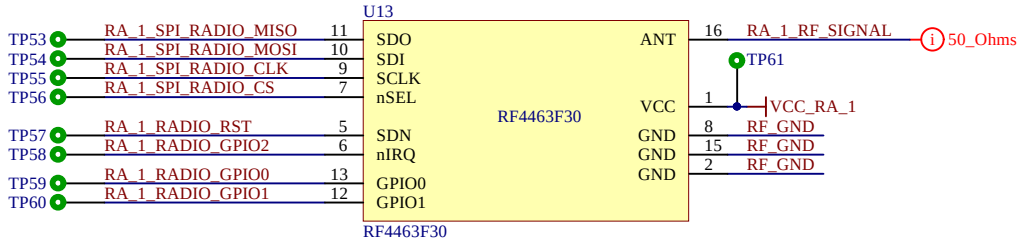




SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Radio 0*			
Designed by: *André M. P. Mattos*			Project Code: *TTC2*
Date: 15/04/2021	Revision: *v0.1*	Sheet *5* of *6*	Size: A4

RADIO 1 (TRANSCEIVER)

Notes:
nIRQ - Interrupt output
GPIO0/1 - Si4463 GPIOs
SDN - Power down control
(SDN=1, power down)



NiceRF RF4463F30 transceiver module:
- Based on the Si4463/61/60-C transceiver
- Antenna matching network and two-way switch control
- 3.3-6.5 V Power supply
- Receiving current: 15mA
- Transmitting current: 500mA (at VCC=5V and TX=30dBm)
- Typical output power: +30dBm (at 433MHz and VCC=5V)
- Sensitivity up to -126 dBm (at 433MHz and Data rate=600bps)
- Operating Temperature Range:-40 + 85 °C

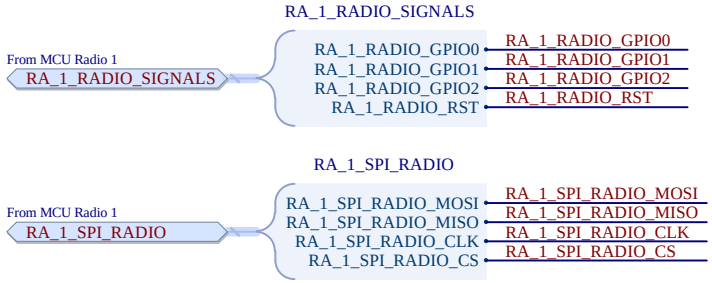
- Frequency Range: 315/433/490/868/915 (Customizable 142-1050MHz)
- Modulation: (G)FSK,4(G)FSK,(G)MSK,OOK and ASK
- Data transfer rate: 0.1-1000Kbps
- TX/RX FIFO: 64/128Byte data register

FloripaSat-1 Configuration:
Customization:
- Center Frequency: 160Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 1.2Kbps
- Input voltage: 5V
- Output power: +28.6dBm
- Transmitting current: 500mA
- Receiving current (always on): 15mA
- Modulation: GFSK

FloripaSat-2 Configuration:
Customization:
- Center Frequency: 160Mhz

Operating parameters:
- Sensitivity up to -126dBm
- Data transfer rate: 1.2Kbps
- Input voltage: 6V
- Maximum output power: +30dBm
- Transmitting current: 550mA
- Receiving current (always on): 15mA
- Modulation: GMSK



SpaceLab - Federal University of Santa Catarina			
Project: *ttc2_project.prjpcb / [No Variations]*			
Title: *Radio 1*			
Designed by: *André M. P. Mattos*			Project Code: *TTC2*
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