

V_USB

C1
2.2uF

GND

R1
100k

V_USB

U1
IN OUT
EN
GND BP
MIC5219 3.3V

PROC_PWR_EN

GND

3.3V

C2
2.2uF

GND

MIC5219-3.3V

Iout (max): 500mA

Vin (max): 12V

Vdrop (typ @ 500mA): 350mV

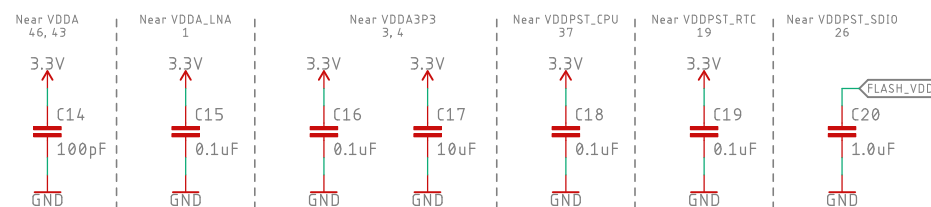
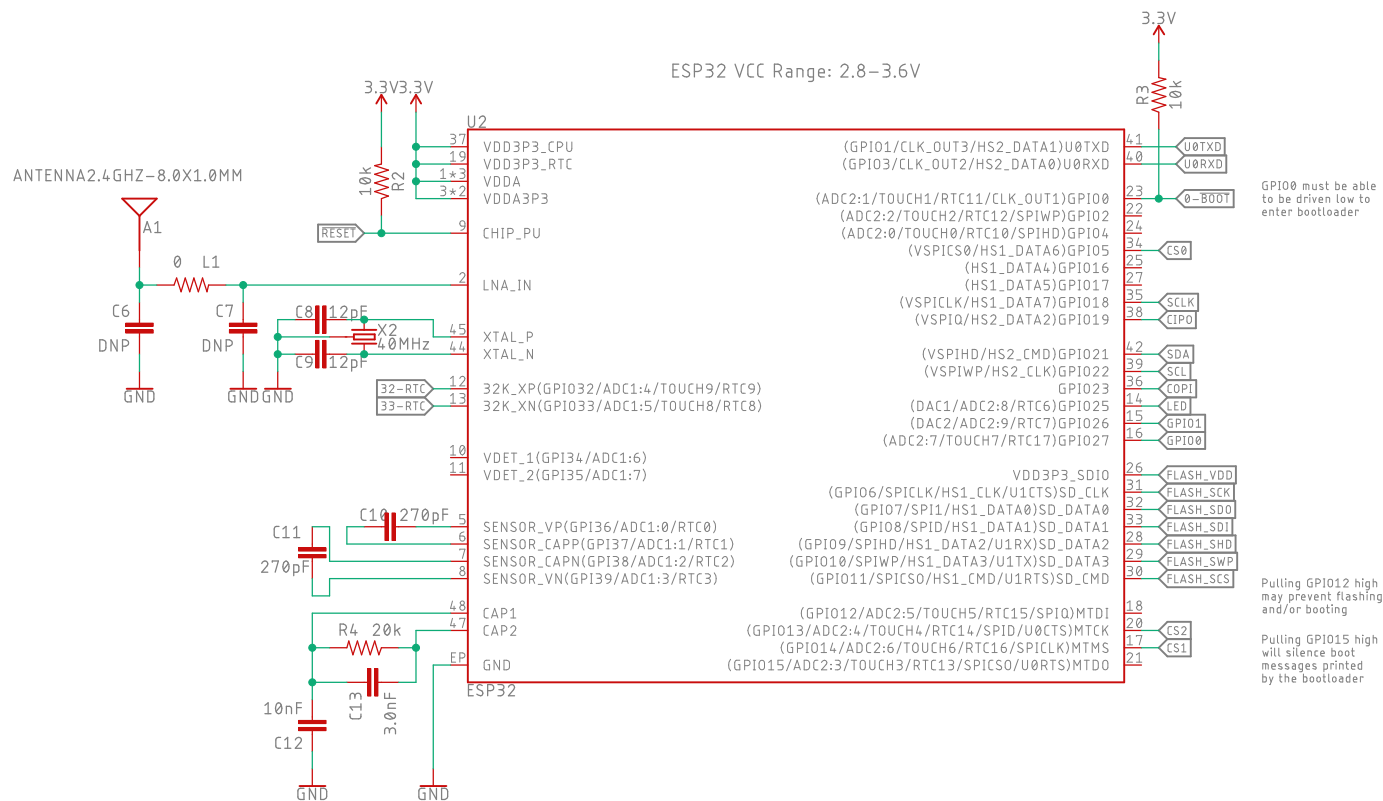
Vdrop (max @ 500mA): 500mV

Iq (typ): 80uA

Output discharge: None

The figure contains two pin connection diagrams. The left diagram, labeled 'Bottom' vertically, shows a 16-pin connector. Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16 are shown. Connections include: 3.3V to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16; GND to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16; and V_USB to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16. The right diagram, labeled 'Top' vertically, shows a similar 16-pin connector. Connections include: 3.3V to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16; GND to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16; and V_USB to pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16. Additional labels include PROC_PWR_EN, SCLK, C0P1, CIPO, CS0, CS1, CS2, GPIO0, GPIO1, SDA, and SCL.

ANTENNA2.4GHZ-8.0X1.0MM



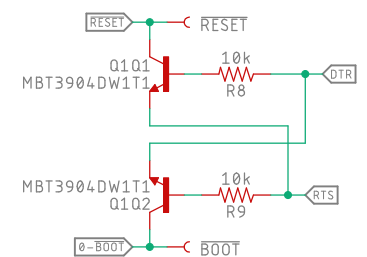
RF Track Impedance: Coplanar Waveguide with Ground Calculations
<https://chemandy.com/calculators/coplanar-waveguide-with-ground-calculator.htm>

JLCPCB JLC7628 4-Layer 1.2mm Impedance Control Stackup ($\epsilon_r = 4.6$)

Ground is on layer 2.
Prepreg thickness: 0.2mm
12 mil track with 4 mil gap = 49.5 Ohms

Boot Mode Configuration			
Pin	Default	Boot	Download
GPIO0	1	1	0
U0TXD	1	1	x
GPIO2	0	x	0
GPIO4	0	x	x
MTD0	1	x	x
GPIO5	1	1	x

If U0TXD, GPIO2, GPIO5 are floating, GPIO0 determines boot mode



If DTR is LOW, toggling RTS from HIGH to LOW resets to run mode.
If RTS is HIGH, toggling DTR from LOW to HIGH resets to bootloader.



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TITLE: SparkX_EZ_ESP32

Design by: Paul Clark

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Special Instructions
Special InstructionsREV:
X01

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