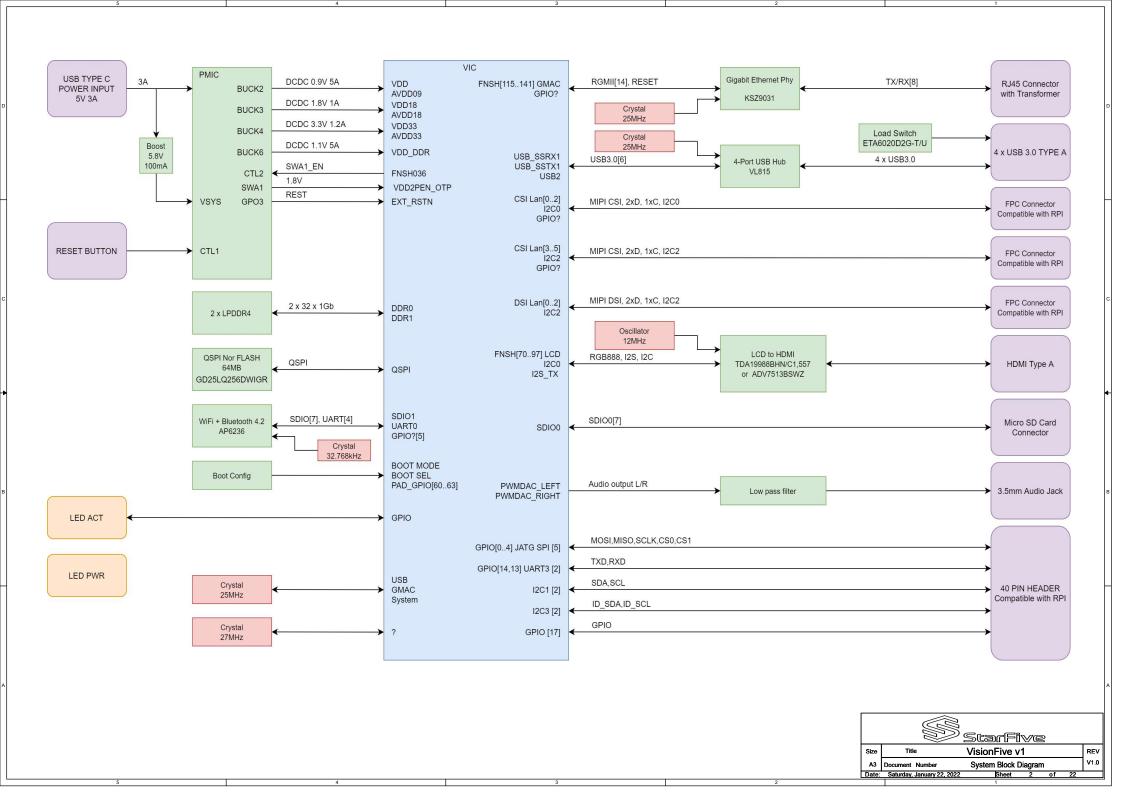
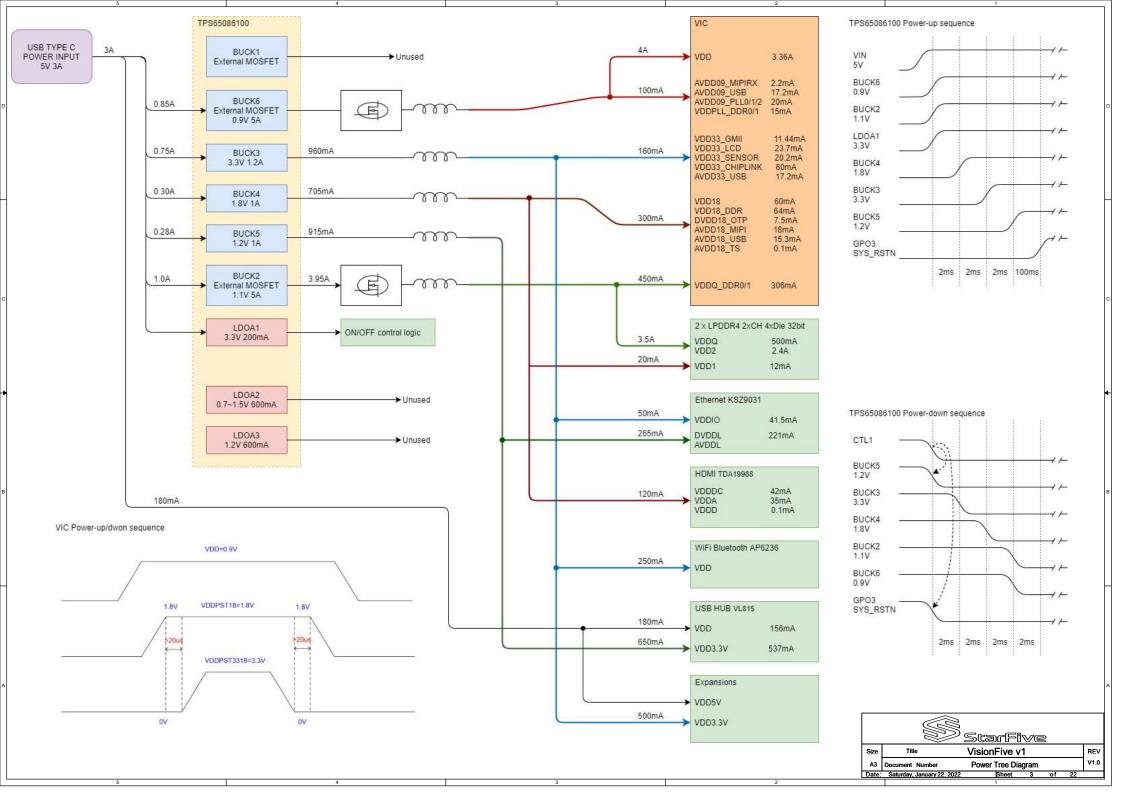
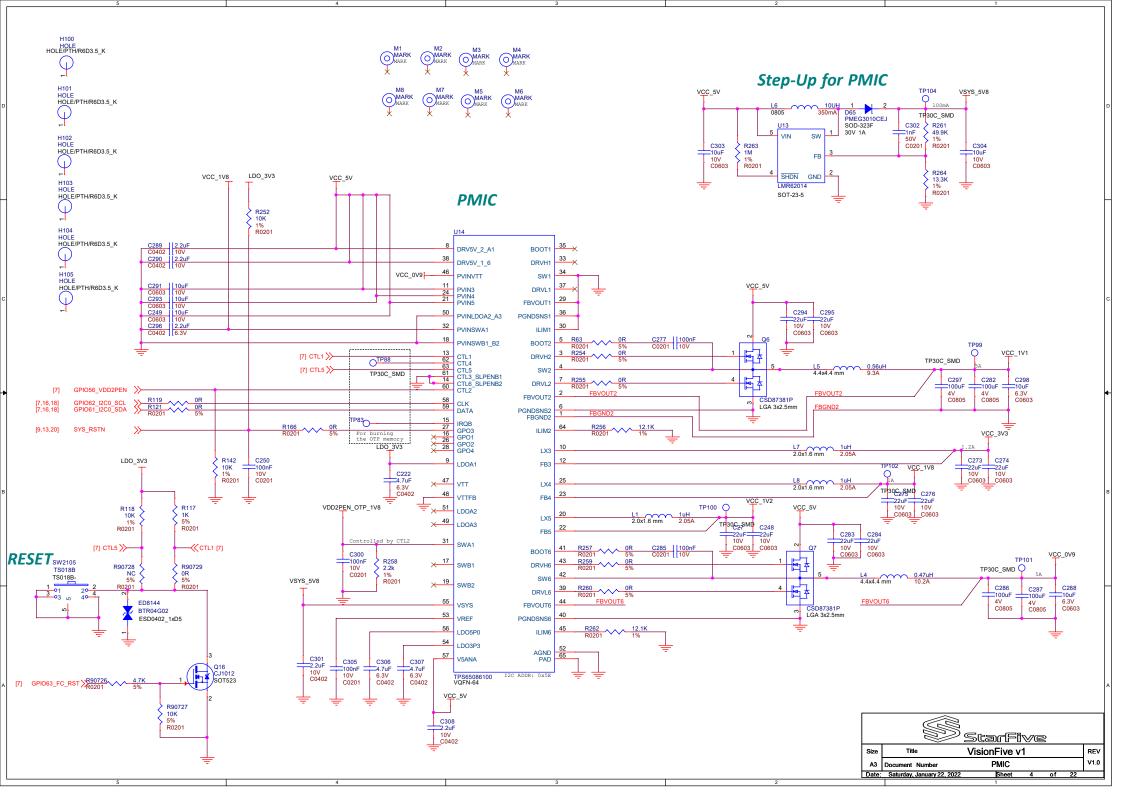
Schematic: Expansion Accessory

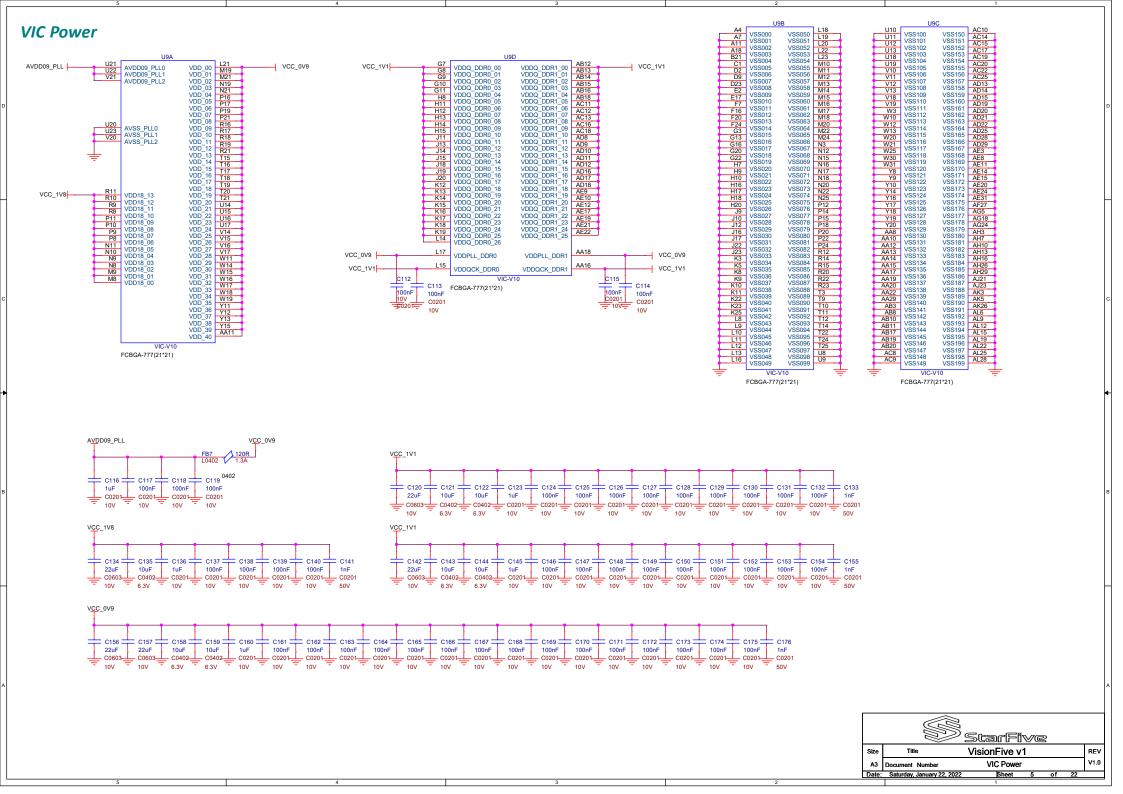
SHEET	SHEET NAME
01	Title/Revision History
02	System Block Diagram
03	Power Tree Diagram
04	PMIC
05	VIC Power
06	VIC DDR Ctrl
07	VIC ChipLink & CM
08	VIC LCD & GMII & GPIOs
09	VIC HighIF & Ctrl Other
10	LPDDR (A)
11	LPDDR (B)
12	Type C,uSD, QSIP Flash
13	USB 3.0 HUB
14	2 x USB TYPE A (A)
15	2 x USB TYPE A (B)
16	2 x CSI CONN
17	DSI, AUDIO JACK
18	HDMI FRAMER
19	WiFi, Bluetooth
20	10/100/1000 ETHERNET
21	RPI EXP CONN, LED, BUTTON
22	Power-DC IN

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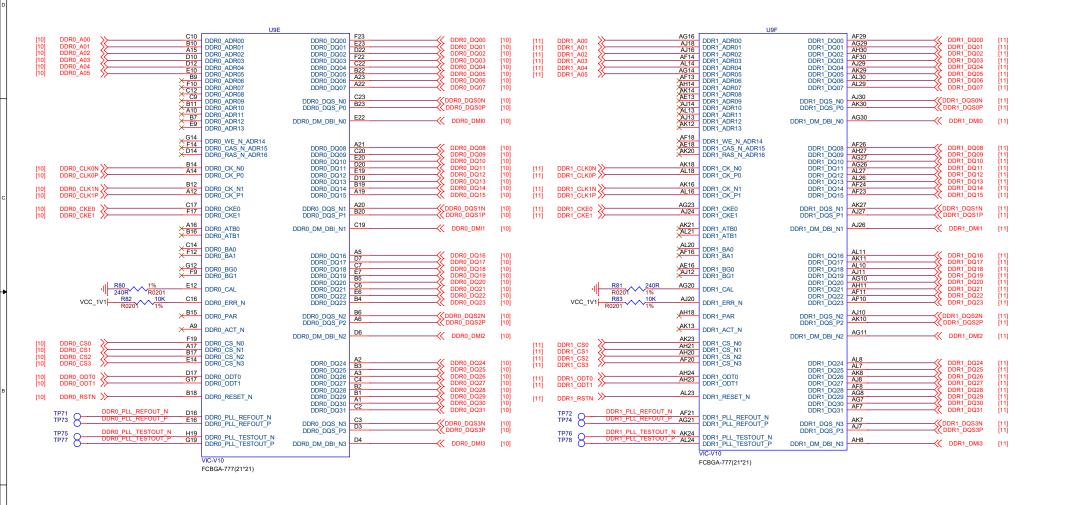




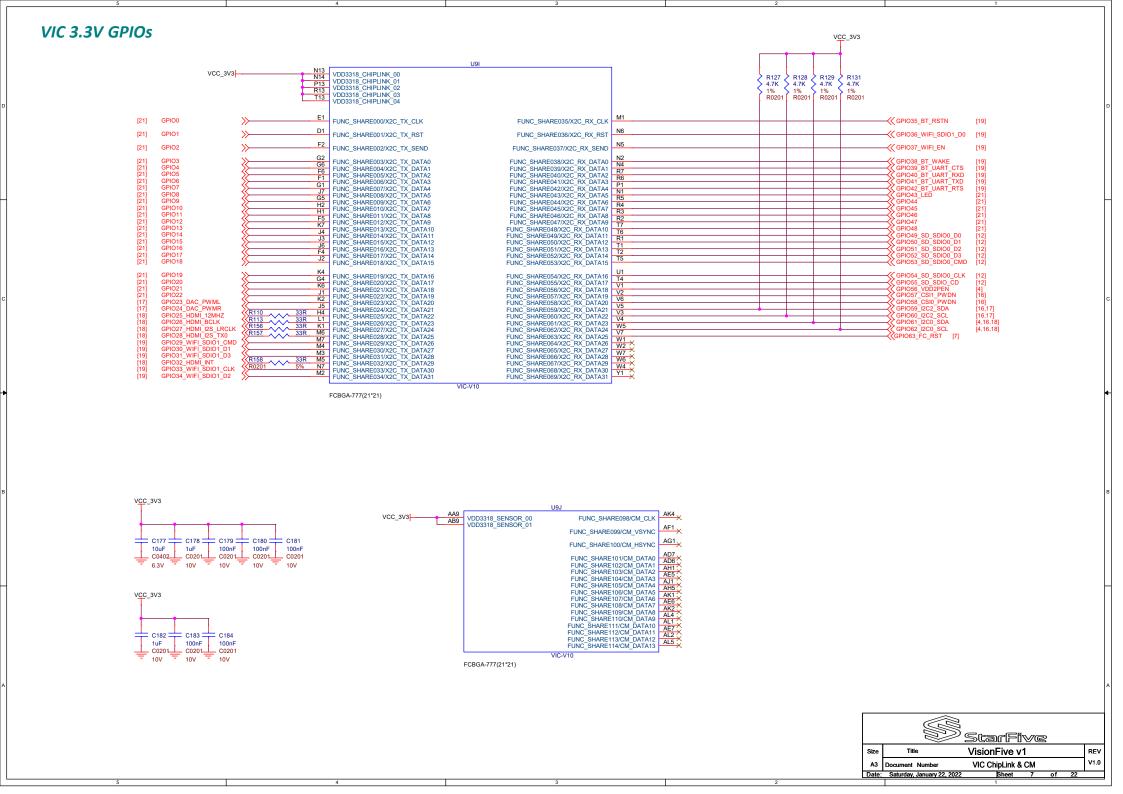


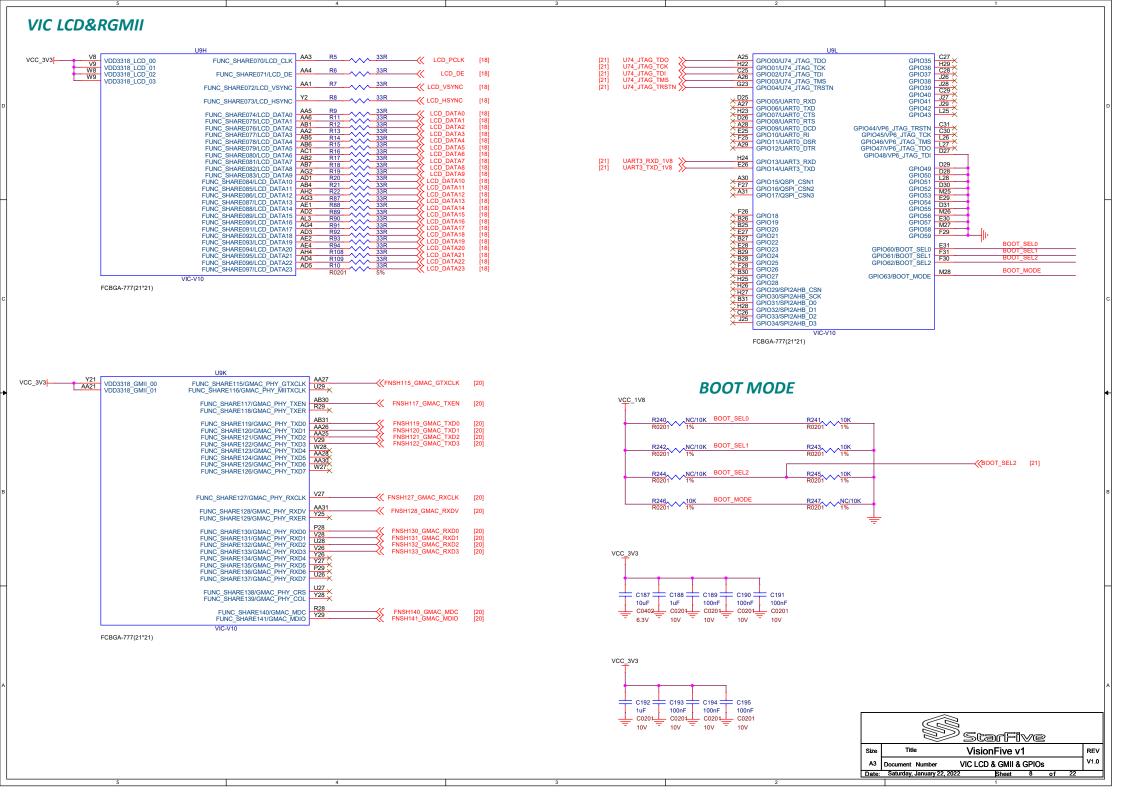


VIC DDR controller



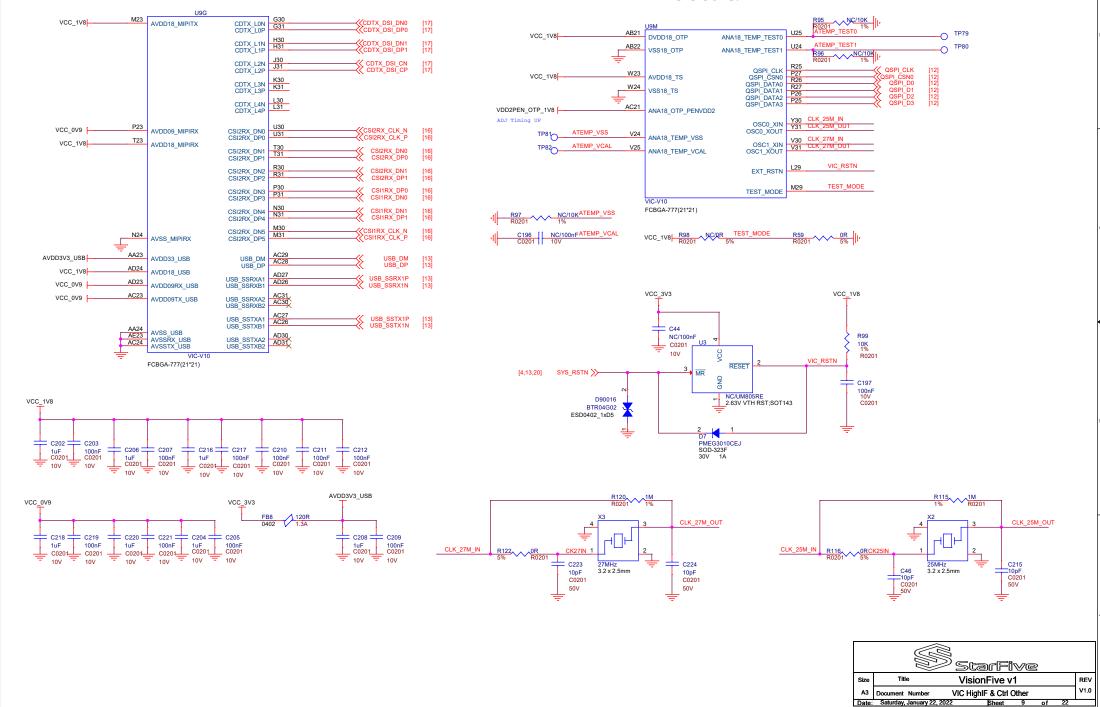


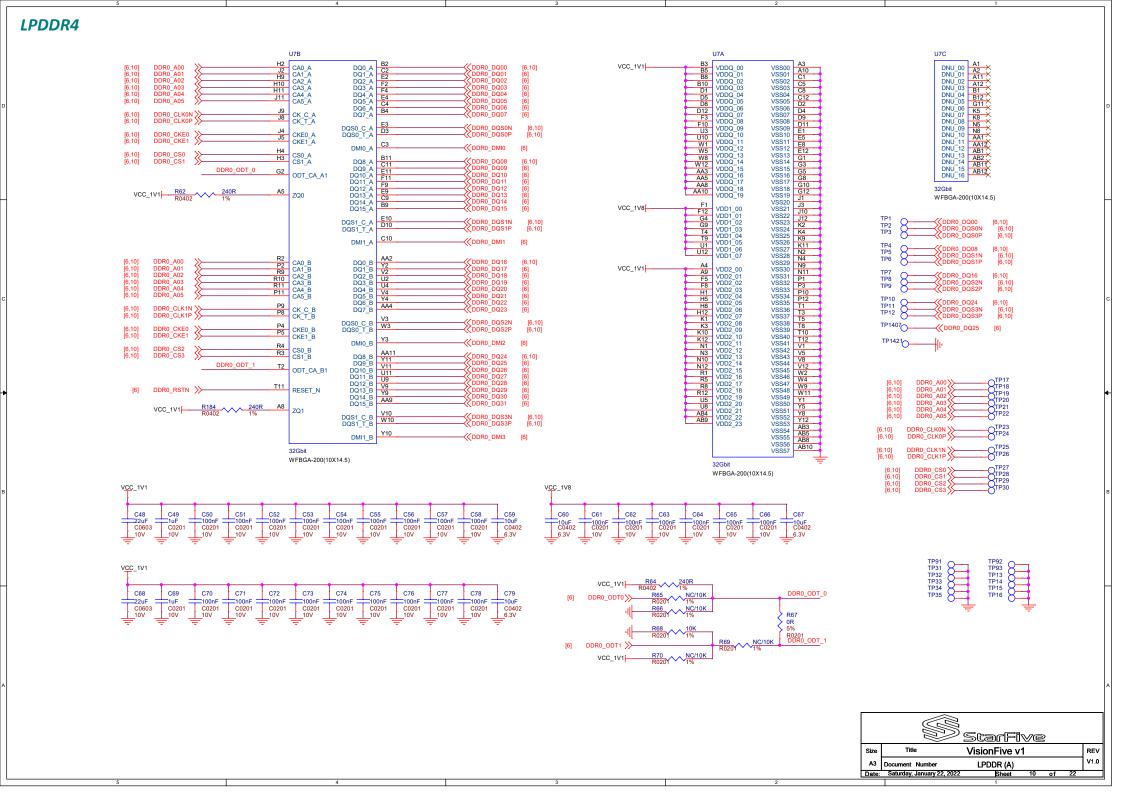




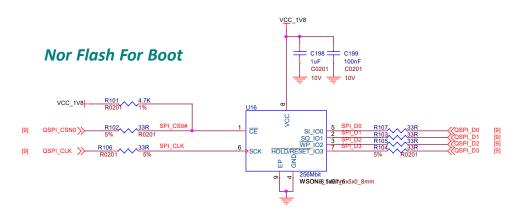
VIC MIPI&USB

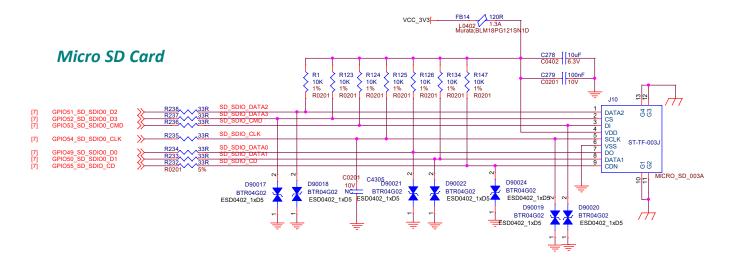
VIC Clock&



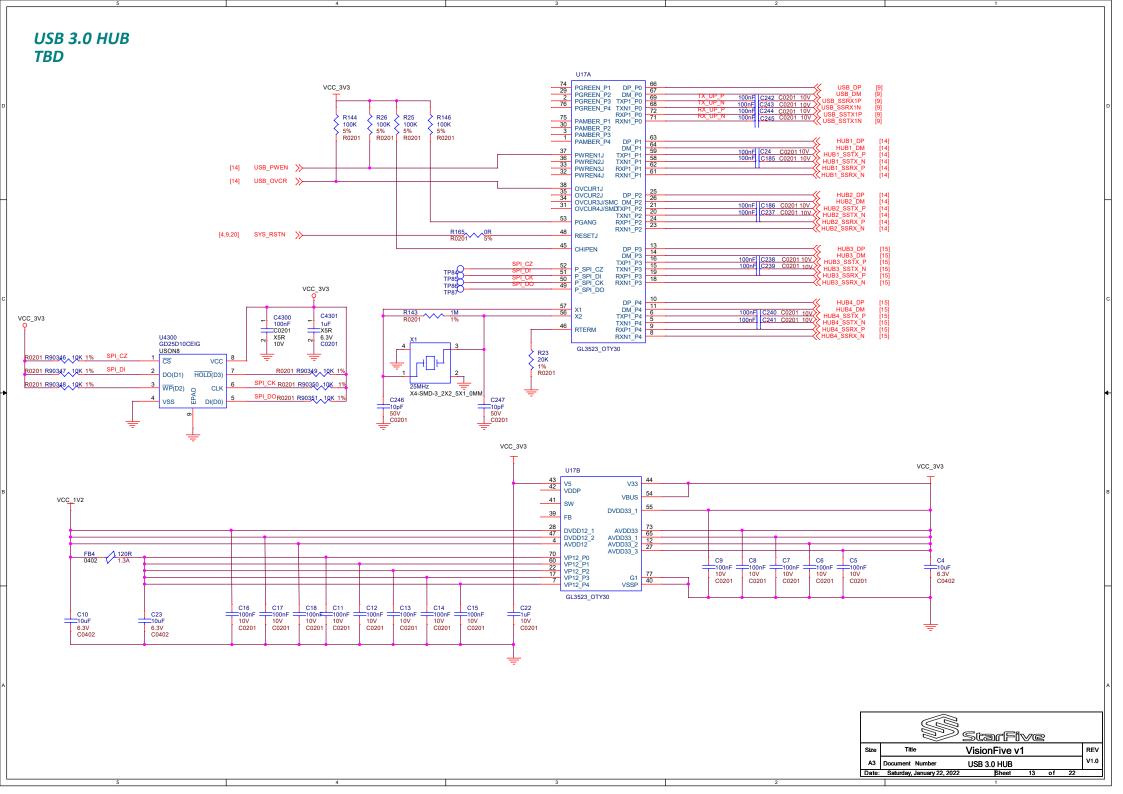


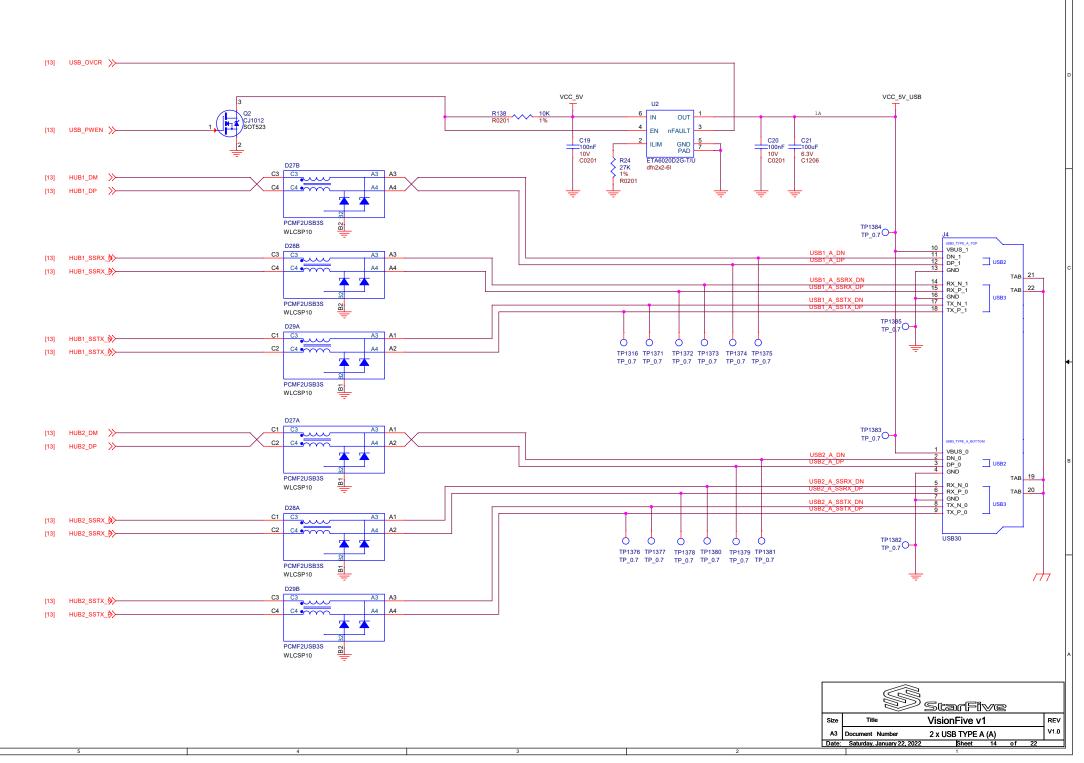
LPDDR4 U8B U8A U8C VSS00 A3
A10
VSS01 C1
VSS02 C5
VSS03
VSS04
VSS05
VSS06
D2
VSS06
D4
VSS07 H2 J2 CA1_A CA1_A CA2_A DDR1_A00 DDR1_A01 DDR1_A02 DDR1_A03 DQ0_A VCC_1V1 VDDQ_00 B5 B8 B10 DQ1_A DQ2_A DDR1 DQ01 VDDQ 01 DDR1_DQ02 DDR1_DQ03 VDDQ_02 CA3_A CA4_A DQ3_A DQ4_A VDDQ_03 VDDQ_04 D1 D5 D8 D12 H11 DDR1 A04 J11 CA4_/. CA5_A DDR1_A05 DQ5_A DQ6_A DDR1_D005 VDDQ_05 VDDQ_06 D12 VDDQ 07
F3 VDDQ 08
F10 VDDQ 08
F10 VDDQ 08
U3 VDDQ 10
U10
W1 VDDQ 11
W5 VDDQ 12
W8 VDDQ 18
W12 VDDQ 14
AA3 VDDQ 15
AA8 VDDQ 15
AA8 VDDQ 17
AA8 VDDQ 18
AA8 VDDQ 18
AA8 VDDQ 18
AA8 VDDQ 18 DDR1 CLK0N CK_C_A CK_T_A VDDQ_07 VDDQ_08 VSS07 VSS08 D9 D11 E1 E5 E8 E12 G1 G3 G5 G8 G10 DDR1_DQS0N DQS0_C_A VSS09 VSS10 CKE0 A DQS0 T A DDR1 CKE1 CKE1_A VSS11 C3 ✓ DDR1_DMI0 DMI0_A VSS12 H4 H3 CS1_A B11 DQ8_A DQ9_A DQ10_A DQ11_A DQ11_A DQ12_A F9 CDDR1 DQ08 [6.11] VSS14 DDR1_DQ09 VSS15 DDR1_ODT_0 G2 ODT_CA_A1 VSS16 VSS17 DDR1_DQ11 VSS18 VSS19 A5 ZQ0 R71 240R 1% AA10 G12 DDR1_DQ13 DDR1_DQ14 DDR1_DQ15 VCC_1V1 DQ13 A VDDQ_19 32Gbit DQ14_A VSS20 VSS21 WFBGA-200(10X14.5) F1 VDD1 00 F12 VDD1 01 F12 VDD1 01 F12 VDD1 01 VDD1 03 VDD1 05 VDD1 07 VCC_1V8 VDD1_00 VDD1_01 DQ15 A J10 J12 VSS22 DDR1_DQ00
DDR1_DQS0N
DDR1_DQS0P DOS1 C A VSS23 VSS23 VSS24 K4 **TP37** DDR1_DQS1P VDD1_04 VDD1_05 VDD1_06 VDD1_07 C10 DMI1_A -≪DDR1_DMI1 TP39 CDDR1 DQ08 [6,11] TP40 TP41 DDR1_DQS1N [6,11] [6,11] R2 P2 R9 R10 A4 VDD2_00
A9 VDD2_01
F5 VDD2_02
H1 VDD2_03
H5 VDD2_04
H8 VDD2_06
H8 VDD2_06 DDR1_A00 DDR1_A01 DDR1_A02 DDR1_A03 CA0_B CA1_B DQ0 B CDDR1 DQ16 DQ1 B VCC_1V1 TP42 CA2_B CA3_B CA4_B DDR1_DQ18 DDR1_DQ19 [6,11] [6,11] DQ2_B DQ3_B TP43 TP44 R11 P11 U4 V4 DQ4_B DQ5_B DDR1_DQ21 CA5_B TP45 DDR1_DQ24 DDR1_DQS3N DDR1_DQS3P [6,11] [6,11] [6,11] DQ6_B DQ7_B DDR1_DQ22 DDR1_DQ23 VDD2_05 VDD2_06 P9 TP46 [6,11] [6,11] CK_C_B DDR1 CLK1N H12 K1 K3 H12 VDD2 06
K1 VDD2 07
K3 VDD2 08
K10 VDD2 09
K12 VDD2 10
K13 VDD2 10
K12 VDD2 11
N3 VDD2 13
N10 VDD2 13
N12 VDD2 14
R1 VDD2 16
R8 VDD2 17
R12 VDD2 17
R12 VDD2 18 **TP47** P8 CK_T_B DQS0_C_B DQS0_T_B CDDR1 DQS2N [6,11] [6,11] DDR1_CKE0 DDR1_CKE1 CKE0 B DDR1_DQS2P P5 CKE1_B Y3 DMI0_B √CDDR1_DMI2 R4 R3 DDR1_CS2 CS0_B CS1_B AA11 ⟨CDDR1_DQ24 DQ8 B DQ9_B DQ10_B DDR1_DQ25 DDR1_DQ26 DDR1_ODT_1 T2 ODT_CA_B1 DDR1_DQ27 DDR1_DQ28 DDR1_DQ29 TP52 TP53 TP54 DDR1_A00 DQ12 B T11 DDR1_RSTN >> RESET_N DQ13_B VDD2_17 VDD2_18 VDD2_19 VDD2_20 VDD2_21 VDD2_22 R12 U5 U8 AB4 AB9 DDR1_A02 DDR1_A03 DDR1_DQ30 DQ14 B TP55 TP56 DQ15 B DDR1_DQ31 VSS50 R72 240R R0402 1% VCC_1V1 701 VSS51 VSS51 VSS52 VSS53 VSS54 TP57 ⟨CDDR1_DQS3N DQS1_C_B Y12 AB3 DQS1_T_B ⟨CDDR1_DQS3P VDD2_23 TP58 VSS54 VSS55 VSS56 AB8 AB10 Y10 -≪DDR1_DMI3 TP59 DDR1 CLK0P DMI1_B TP60 [6,11] 32Gbit VSS57 TP61 WFBGA-200(10X14.5) 32Gbit TP62 DDR1 CS0 S WFBGA-200(10X14.5) TP63 TP64 DDR1 CS1 DDR1 VCC_1V1 VCC_1V8 TP65 C80_ = C81 C82 C83 C84 C85 C86 C87 C88 C89 C92 C97 C99 C90 = C91 C93 C94 C95 C96 C98 100nF 100nF 100nF 100nF 100nF 100nF 100nF 22uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 10uF 10uF 100nF 100nF _C0201 <u></u> _C0201 __ \pm C0201 \pm C0201 -C0402 --C0201 -_C0201 ____C0201 _ C0201 -10V 10V 10V 10V 10V 10V 10V 10V 10V 10V 6.3V 10V 10V 10V 10V 10V 10V TP96 TP66 TP67 TP68 TP69 TP95 TP48 TP49 TP50 TP51 R73 240R R0402 1% VCC_1V1 VCC_1V1 DDR1_ODT_0 R74 NC/10K DDR1_ODT0 >> R75 NC/10K R76 C100 C101 C102 C103 C104 C105 C106 C107 C108 C109 C110 = C111 0R 5% 22uF 1uF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 100nF 10uF R77 10K R78 NC/10K -C0603 -C0201 -_C0201 C0201 =C0201 = C0201 C0201 C0201 = C0201 = C0201 C0201 -C0402 DDR1_ODT1 >> 10V 6.3V R79 NC/10K VCC_1V1 StarFive Title VisionFive v1 REV V1.0 A3 Document Number LPDDR (B) Date: Saturday, January 22, 2022

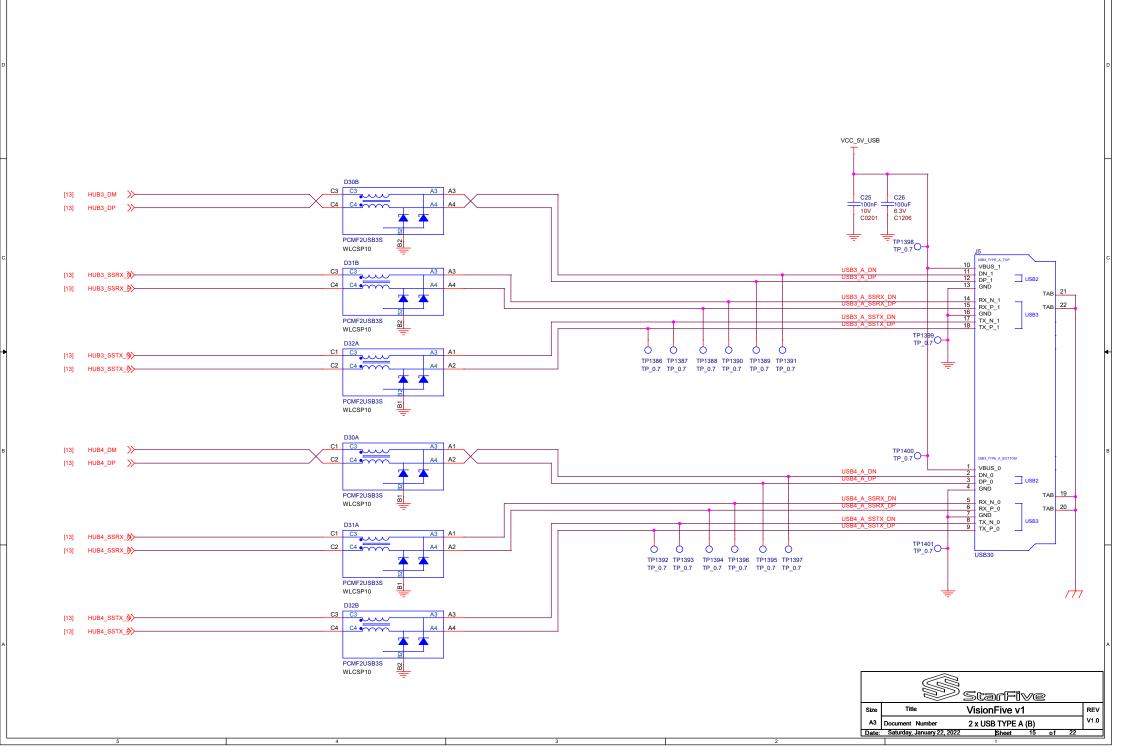


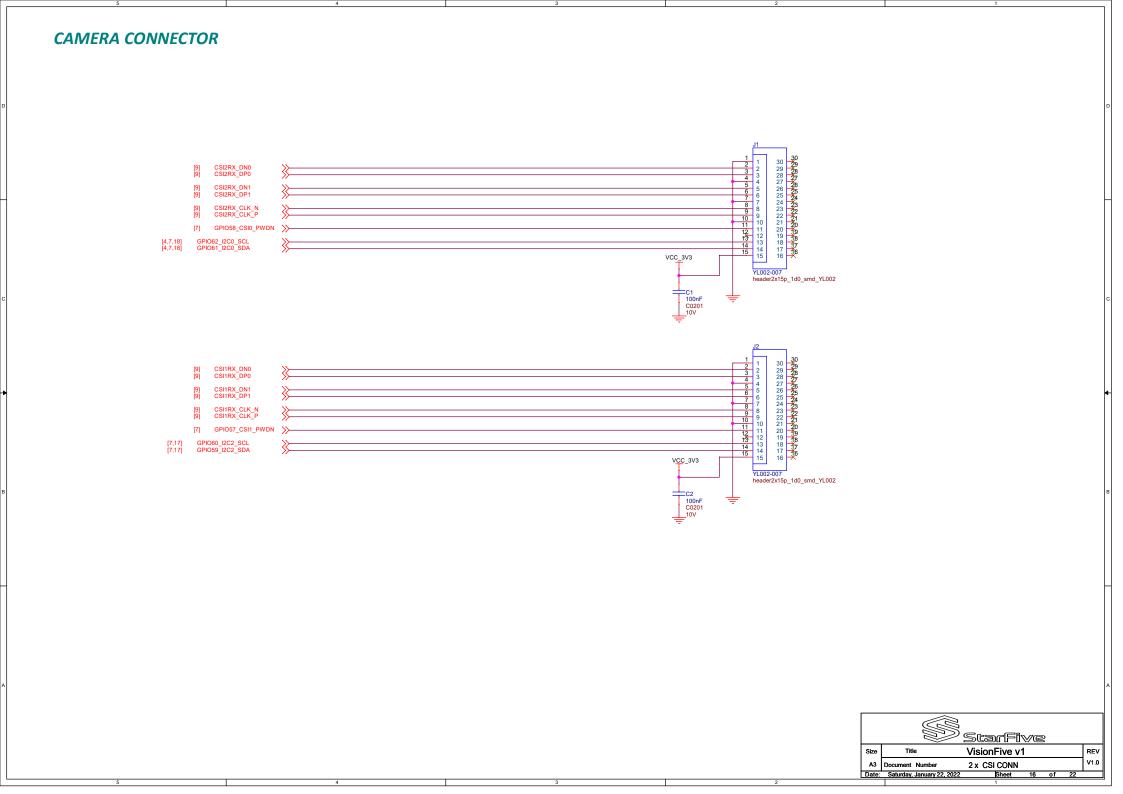


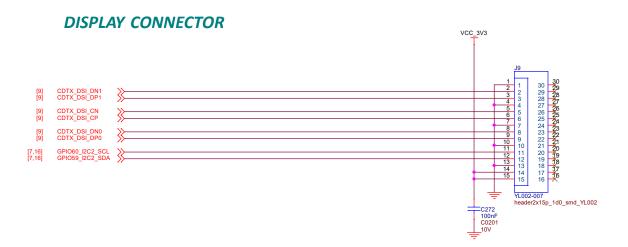
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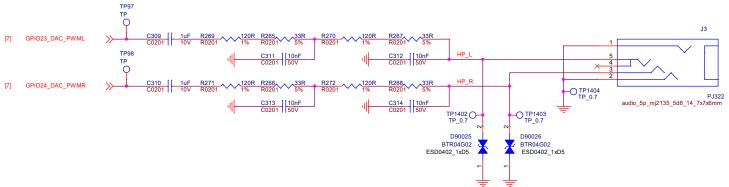












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