EXPT NO.: 10

DESIGN OF UP/DOWN COUNTER

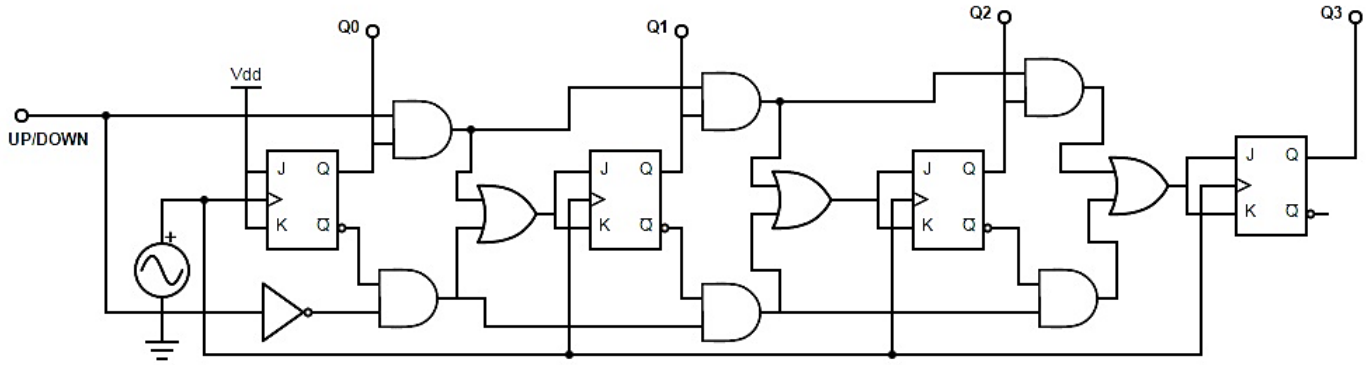
AIM:

To design and simulate a 4-bit up/down counter.

4-BIT UP/DOWN COUNTER:

A circuit used for counting the pulses is known as **counter.** An up/down counter can count in any direction depending on the direction control input.

The design of up/ down counter with JK flip flops is shown below:



The up/ down counter has “Up” and “Down” count modes by having 2 input AND gates, which are used to detect the appropriate bit conditions for counting operation. OR gates are used to combine the outputs of AND gate, from each JK flip flop.

We provide an up/ down control line which enables upper or lower series of AND gates to pass the outputs of JK flip flops, Q, Q’ to the next stage of flip flop, in the cascaded arrangement.

If the up /down control line is set to HIGH, then the top AND gates are in enable state and the circuit acts as UP counter. If the up /down control line is set to low, then the bottom AND gates are in enable state and the circuit acts as DOWN counter.

TRUTH TABLE:

RESET	UP/DOWN	CLOCK PULSE No.	OUTPUT			
			O_3	O_2	O_1	O_0
1	0	0	0	0	0	0
0	0	1	0	0	0	0
		3	0	0	0	1
		5	0	0	1	0
		7	0	0	1	1
		9	0	1	0	0
		11	0	1	0	1
		13	0	1	1	0
		15	0	1	1	1
		17	1	0	0	0
		19	1	0	0	1
		21	1	0	1	0
		23	1	0	1	1
		25	1	1	0	0
		27	1	1	0	1
		29	1	1	1	0
		30	1	1	1	1
	1	31	1	1	1	1
		33	1	1	1	0
		35	1	1	0	1
		37	1	1	0	0
		39	1	0	1	1
		41	1	0	1	0
		43	1	0	0	1
		45	1	0	0	0
		47	0	1	1	1
		49	0	1	1	0
		51	0	1	0	1
		53	0	1	0	0
		55	0	0	1	1
		57	0	0	1	0
		59	0	0	0	1
		60	0	0	0	0

- **It's advised to implement the counter using vhdl logic and the above truth table instead of the provided circuit diagram. Take a STD_LOGIC_VECTOR (3 downto 0) variable and use it to store the temporary counts and map it to the output vector.**

The i/o ports needed for the formation of up/down counter is given below:

Port Name	INPUT/OUTPUT	Bus
Up/Down	In	No
Reset	In	No
Clk	In	No
Count	Out	4-Bit Bus (3 downto 0)

- **NB: Use temporary variable where ever necessary.**