EXPT NO.: 12

DESIGN A 128 x 8 RAM

AIM:

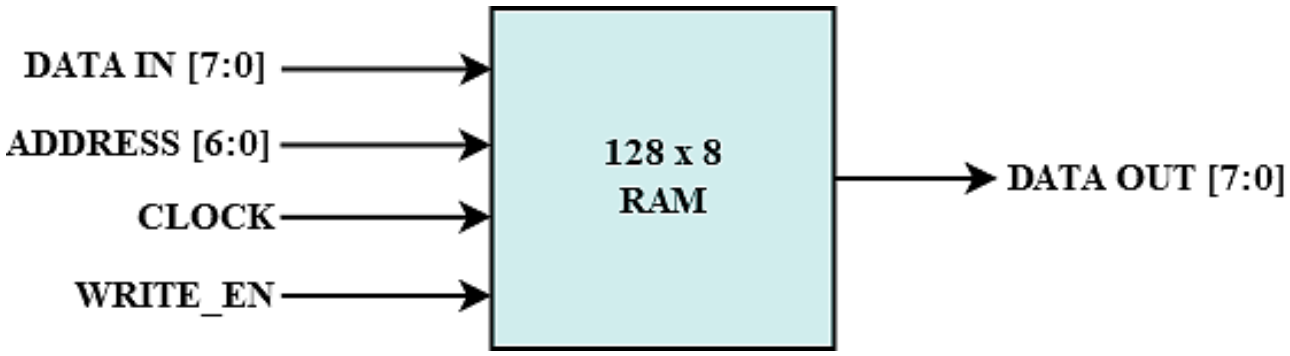
To design and simulate a 128 x 8 RAM.

128 x 8 RAM:

RAM (Random Access Memory) is a memory device that is used in the systems read/write and store the data. RAM is present ranging from small-scale systems such as embedded systems, smartphones to large-scale systems as Desktop, Laptops, etc. The RAM used in a system has a major impact on the system's performance. It's responsible for carrying out multiple tasks and storing data. The higher the version of a RAM, the higher it's performance.

Usually, memory is represented by ***M x N***, where ***M is the number of locations*** and ***N is the Data lines***. So here; 128 x 8, '128' represents 128 locations, or ***an array that has 128 locations***, with an address bus of 7 (2^7=128) bits and '8' represents 8 data lines. In simpler terms, a 128 x 8 RAM has 128 locations and each of these 128 locations can store 8-bit data. So, the total number of bits that can be stored by a 128 x 8 RAM is 1024 bits.

The block diagram of 128 x 8 RAM is shown below:



DESCRIPTION TABLE FOR RAM:

PIN	FUNCTION
DATA IN [7:0]	8-Bit Data Input
DATA OUT [7:0]	8-Bit Data Output
ADDRESS [6:0]	7-Bit Address Line
CLOCK	Clock
WRITE_EN	Write enable i.e., writes data to RAM for WRITE_EN = 1

The i/o ports needed for the formation of 128 x 8 RAM is given below:

Port Name	INPUT/OUTPUT	Bus
Address	In	7-Bit Bus (6 downto 0)
Data_in	In	8-Bit Bus (7 downto 0)
Clk	In	No
Write_en	In	No
Data_out	Out	8-Bit Bus (7 downto 0)

- **NB: Use temporary variable where ever necessary.**

VHDL Code for the ADDRESS ARRAY:

```
type RAM_ARRAY is array (0 to 127) of std_logic_vector (7 downto 0);
signal RAM: RAM_ARRAY :=(
        x"55",x"66",x"77",x"67",-- 0x00:
        x"99",x"00",x"00",x"11",-- 0x04:
        x"00",x"00",x"00",x"00",-- 0x08:
        x"00",x"00",x"00",x"00",-- 0x0C:
        x"00",x"00",x"00",x"00",-- 0x10:
        x"00",x"00",x"00",x"00",-- 0x14:
        x"00",x"00",x"00",x"00",-- 0x18:
        x"00",x"00",x"00",x"00",-- 0x1C:
        x"00",x"00",x"00",x"00",-- 0x20:
        x"00",x"00",x"00",x"00",-- 0x24:
        x"00",x"00",x"00",x"00",-- 0x28:
        x"00",x"00",x"00",x"00",-- 0x2C:
        x"00",x"00",x"00",x"00",-- 0x30:
        x"00",x"00",x"00",x"00",-- 0x34:
        x"00",x"00",x"00",x"00",-- 0x38:
        x"00",x"00",x"00",x"00",-- 0x3C:
        x"00",x"00",x"00",x"00",-- 0x40:
        x"00",x"00",x"00",x"00",-- 0x44:
        x"00",x"00",x"00",x"00",-- 0x48:
        x"00",x"00",x"00",x"00",-- 0x4C:
        x"00",x"00",x"00",x"00",-- 0x50:
        x"00",x"00",x"00",x"00",-- 0x54:
        x"00",x"00",x"00",x"00",-- 0x58:
        x"00",x"00",x"00",x"00",-- 0x5C:
        x"00",x"00",x"00",x"00",-- 0x60:
```

```
        x"00",x"00",x"00",x"00",-- 0x64:
        x"00",x"00",x"00",x"00",-- 0x68:
        x"00",x"00",x"00",x"00",-- 0x6C:
        x"00",x"00",x"00",x"00",-- 0x70:
        x"00",x"00",x"00",x"00",-- 0x74:
        x"00",x"00",x"00",x"00",-- 0x78:
        x"00",x"00",x"00",x"00",-- 0x7C:
);
```