

## **COMPUTER ARCHITECTURE LAB MANUAL (PCC-CS492)**

**EXPT NO.:** 6

#### **DESIGN A 4-BIT COMPARATOR**

### AIM:

To design and simulate a 4-bit magnitude comparator.

## **4-BIT MAGNITUDE COMPARATOR:**

The comparison of two numbers is an operator that determine one number is greater than or less than or equal to the other number. A magnitude comparator is a combinational circuit that compares two numbers A and B and determine their relative magnitude. The outcome of the comparator is specified by three binary variables that indicate whether A>B or A=B or A<B.

The two numbers A and B can be represented as:

$$A = A_3 A_2 A_1 A_0$$

$$B = B_3 B_2 B_1 B_0$$

The relative magnitude of pairs of significant digits starting from most significant position to least significant position is compared.

A = B is expanded as:

$$X_3 = \overline{A_3 \oplus B_3}; \quad X_2 = \overline{A_2 \oplus B_2}; \quad X_1 = \overline{A_1 \oplus B_1}; \quad X_0 = \overline{A_0 \oplus B_0}$$

$$A = B = X_3 X_2 X_1 X_0$$

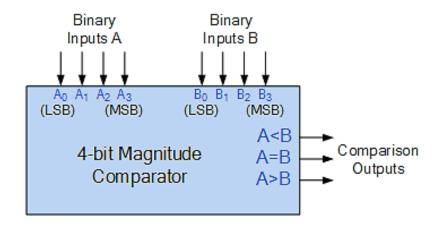
A > B is expanded as:

$$A > B = A_3 \overline{B_3} + X_3 A_2 \overline{B_2} + X_3 X_2 A_1 \overline{B_1} + X_3 X_2 X_1 A_0 \overline{B_0}$$

A < B is expanded as:

$$A < B = \overline{A_3}B_3 + X_3\overline{A_2}B_2 + X_3X_2\overline{A_1}B_1 + X_3X_2X_1\overline{A_0}B_0$$

The block diagram of a 4-bit comparator:

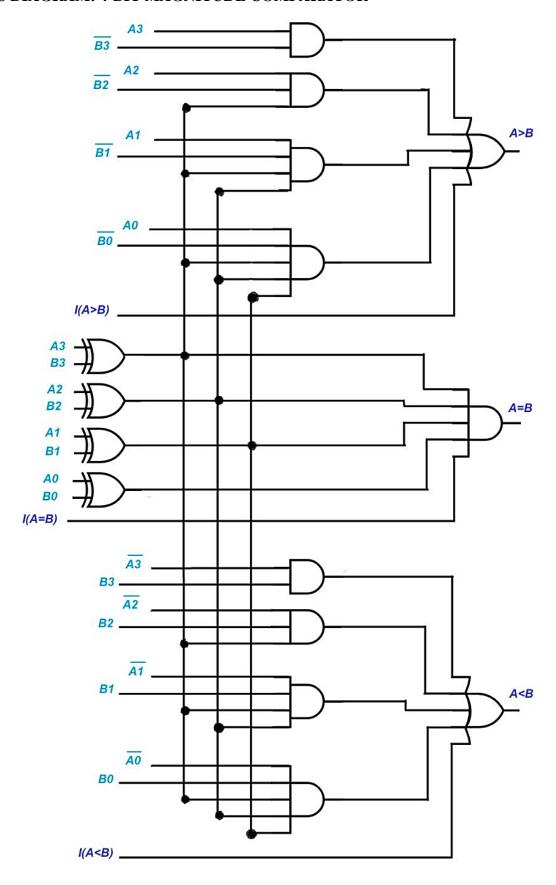


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## LOGIC DIAGRAM: 4-BIT MAGNITUDE COMPARATOR



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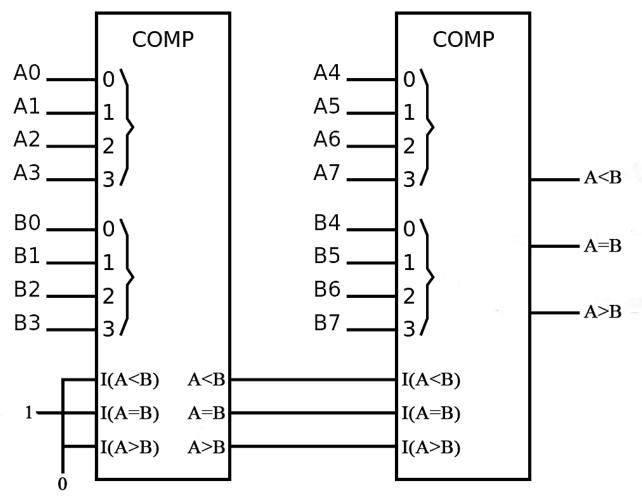
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# The i/o ports for the formation of 4-bit magnitude comparator is given below:

Port Name	INPUT/OUTPUT	Bus
A	In	4-Bit Bus (3 downto 0)
В	In	4-Bit Bus (3 downto 0)
IEq	In	No
IGt	In	No
ILt	In	No
Eq	Out	No
Gt	Out	No
Lt	Out	No

NB: Use temporary variable where ever necessary.

NB: Two 4-bit comparators can also be port mapped to make an 8-bit comparator. The I(A>B), I(A=B) and I(A<B) ports can be used to carry the output from the 1<sup>st</sup> 4-bit comparator to the 2<sup>nd</sup> one. The block diagram for the same is provided here. Everyone is encouraged to try this.



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