EXPT NO.: 7

DESIGN OF MULTIPLEXER AND DEMULTIPLEXER

AIM:

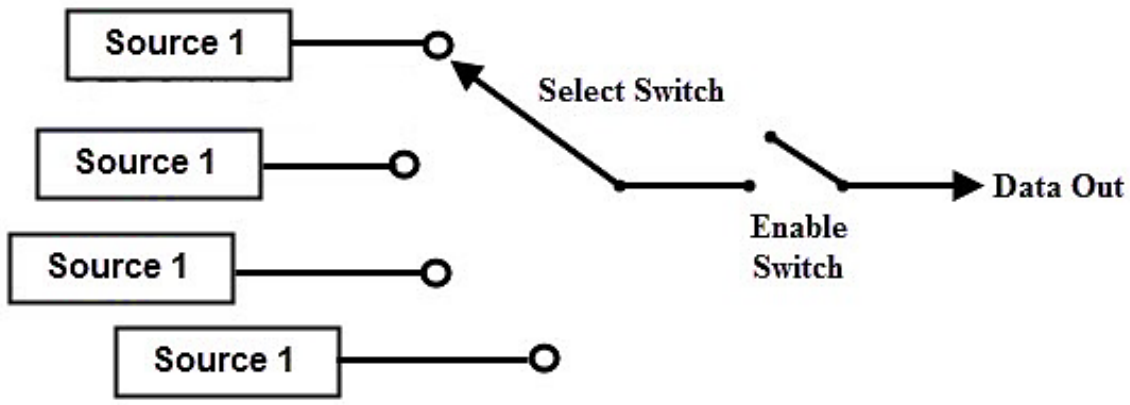
To design and simulate an 8:1 multiplexer and 1:8 demultiplexer using switch cases.

8:1 MULTIPLEXER:

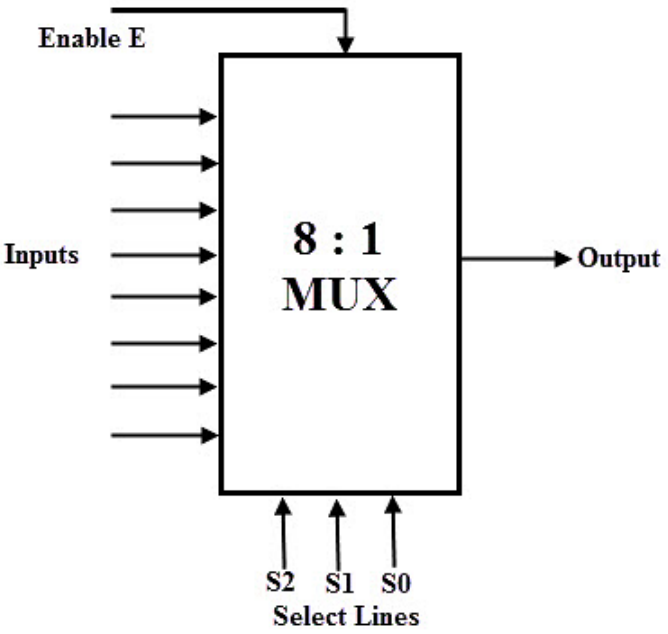
The multiplexer or MUX is a digital switch, also called as data selector. It is a combinational circuit with more than one input line, one output line and more than one select lines. It allows the binary information from several input lines and depending on the set of select lines, particular input line, is routed onto a single output line.

The basic idea of multiplexing is shown in figure below in which data from several sources are routed to the single output line when the enable switch is ON. That is how the multiplexers are also called as 'many to one' combinational circuits.

If there are m selection lines, then the number of possible input lines is 2^m. Alternatively we can say that if the number of input lines is equal to 2^m, then m selection lines are required to select one of n (consider $2^m = n$) input lines. So, for 8:1 multiplexer there will be $8 = 2^3$, so 3 select lines.



The truth table and block diagram of 8:1 mux is given below:



SELECT LINES			OUTPUT
S_2	S_1	S_0	_ = Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

The i/o ports needed to be declared for the formation of 8:1 mux is given below:

Port Name	INPUT/OUTPUT	Bus
Data	In	8-Bit Bus (7 downto 0)
Select	In	3-Bit Bus (2 downto 0)
Out_Data	Out	No

NB: Use temporary variable where ever necessary.

Syntax for switch case in VHDL:

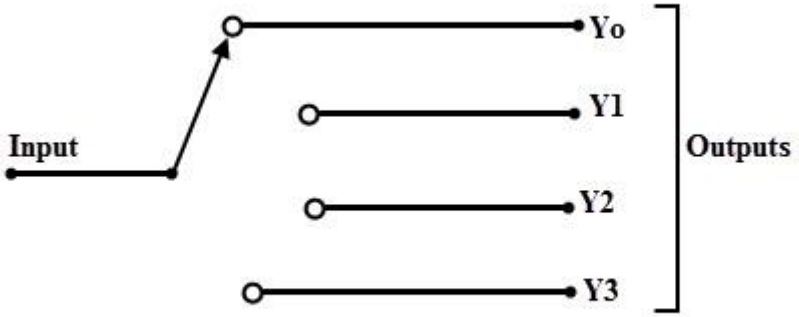
```
process(variable/expression)
        begin
                case variable/expression is
                        when choice => sequential statement;    //when "000" => o<=d(0);
                        when choice => sequential statement;    //when "001" => o<=d(1);
                        .
                        .
                        .
                        when others => sequential statement;    //all the possible choices are to be
                mentioned, i.e., for a case with 3-bit bus, total number of choices will be 7 + others.
                end case;
```

1:8 DEMULTIPLEXER:

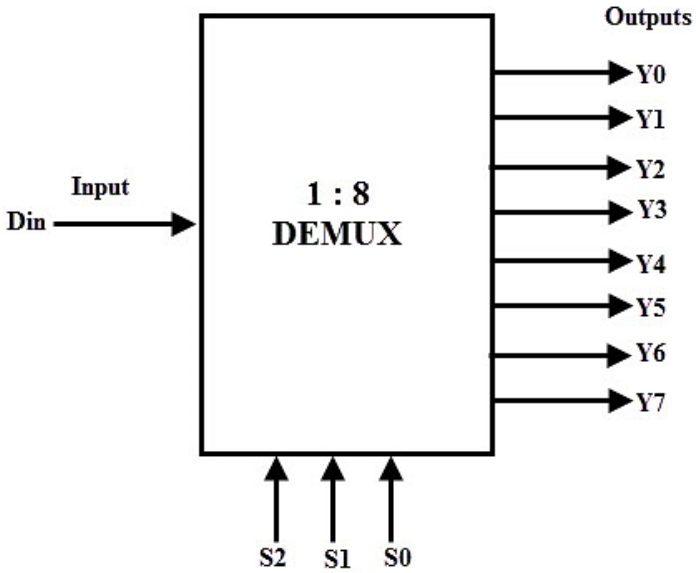
The process of getting information from one input and transmitting the same over one of many outputs is called de-multiplexing. A de-multiplexer is a combinational logic circuit that receives the information on a single input and transmits the same information over one of 2^m possible output lines.

The bit combinations of the select lines control the selection of specific output line to be connected to the input at given instant. The below figure illustrates the basic idea of de-multiplexer, in which the switching of the input to any one of the four outputs is possible at a given instant.

It consists of 1 input line, n output lines and m select lines. In this, m selection lines are required to produce 2^m possible output lines (consider 2^m = n). For example, a 1:8 de-multiplexer requires 3 (2^3) select lines to control the 8 output lines.



The truth table and block diagram of 8:1 mux is given below:



SELECT LINES			OUTPUT
S_2	S_1	S_0	D =
0	0	0	Y_0
0	0	1	Y_1
0	1	0	Y_2
0	1	1	Y_3
1	0	0	Y_4
1	0	1	Y_5
1	1	0	Y_6
1	1	1	Y_7

The i/o ports needed to be declared for the formation of 1:8 demux is given below:

Port Name	INPUT/OUTPUT	Bus
Data	In	No
Select	In	3-Bit Bus (2 downto 0)
Out_Data	Out	8-Bit Bus (7 downto 0)

NB: Use temporary variable where ever necessary.