OLLSCOIL TEICNEOLAÍOCHTA BHAILE ÁTHA CLIATH
DUBLIN
TECHNOLOGICAL UNIVERSITY DUBLIN

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

**Programme: DT008 / 2**
**ELEK2108 Electronics 1**
**Laboratory Technical Report**

| | Name | Student Number |
|---|---|---|
| **Author:** | **TALHA TALLAT** | **D18124645** |

| | |
|---|---|
| **Laboratory Number:** | **C** |
| **Semester Week Number:** | **4** |
| **Date:** | **25/02/2019** |

**Submission Checklist and Declaration**

To ensure that the focus of the assessment of your laboratory report can include the development of higher order skills and competences associated with a Level 7 qualification, please complete the checklist and declaration below.

| **I declare that the report that I am submitting:** | **Confirm** |
|---|---|
| • is my original work, with secondary sources acknowledged; | ☒ |
| • was proofread thoroughly for typographical errors; | ☒ |
| • contains citations with references formatted in the IEEE citation style. | ☒ |
| I understand that my work can be returned uncorrected if the criteria are unfulfilled. | |

**Signature:**

## 1.0 Laboratory Aim

- Describe the purpose of the laboratory or the research.

  The aim of this lab is to use the Vivado Design Environment to design simulate and synthesise a combinational logic.

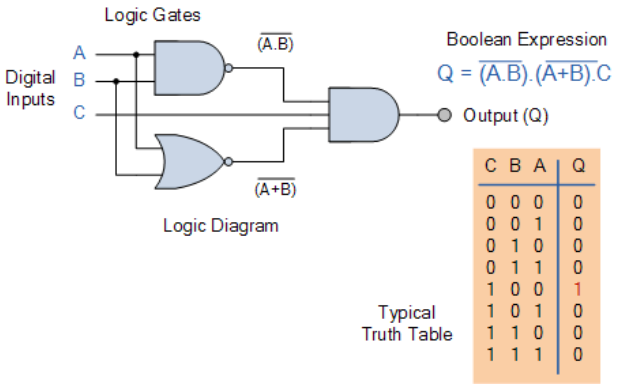
  The purpose of this lab is to create VHDL behavioural design source code and simulate code for testing the design and test combination logic on Artix-7 development board and apply signals throw the switch to confirm that the design works according to the plan.

## 2.0 Laboratory Procedure

- Describe the actions taken during the work.

  The purpose of the lab was to design a Combinational logic. In order to do design, we are using Vivado design Enirоment, which allows us to design sourse code and simulate the code for testing a design.

  The combination logic is type of a digital logic which is apply with Boolean circuit, where output is depended on the multiple logic inputs terminals.




Combinational Logic circuits are memoryless digital logic circuit whose output at any instant in time depends only on the combination of its inputs. The Truth table pattern was given, in order to complete register for active votes.

*Figure 1 – Combinational Logic*

The new project was created in Vivdo in order to design and simulate. New source file was created “Combinational.vhd” and a “Constraints.cx” file was created later with Basys3 board type selected. All the ports were set in Behavioral with their names and direction. The design code was implemented by completing the equations, which are set out by the truth table in the source file. Then new testbench file “Combinational_tb” was created and 5 of the i/o ports were set with their name and direction.

Then the design source code was copied and pasted in the online Test bench editor to generate simulation code structure, which is copied and pasted in the test bench code and added the stimulus code to “Combinational_TB.vhd” in order to test all possible combinations of the four input switches, which are B,K,R and S with the design code: 0000, 0001, 0010, 0011, 0100 up to 1110, 1111. The behavioural simulation was run with runtime of 160ns.

The Simulation was run and reflected the design code as expected and the elaborated design was open to examine the logic circuit schematic.

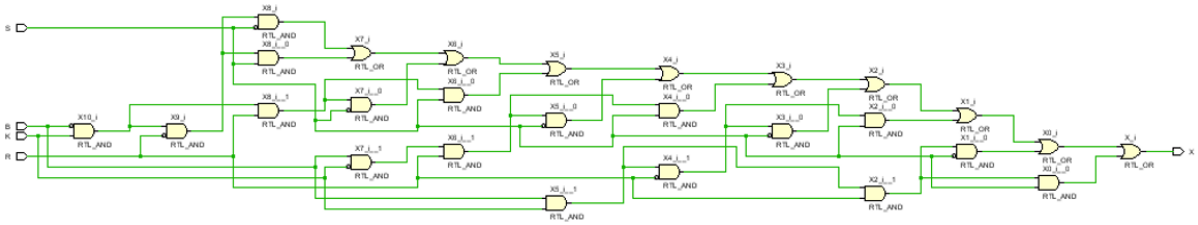


*Figure 2 – Schematic diagram of Combinational*

The new constraints file is created and selected I/O pins voltage levels to LV CMOS 3.3v and select I/O pins and I/O planning view. The files were saved just in case they get losed.

| Signal | Pin | I/O |
|---|---|---|
| B | W17 | SW0 |
| K | W16 | SW1 |
| R | V16 | SW2 |
| S | V17 | SW3 |
| X | U16 | LD0 |

*Figure 3 – planning view pins*

*Figure 4 – Planning View Package*

And running Synthesis.

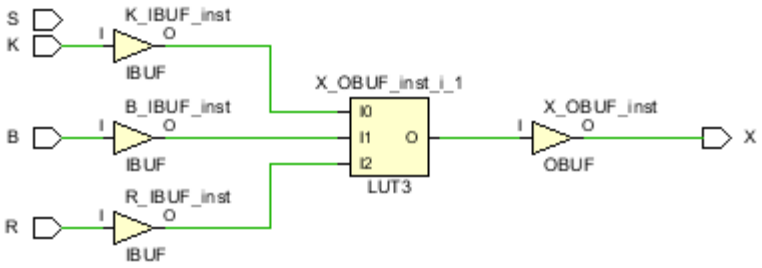



*Figure 5 – Synthesized design schematic*

Edit device properties to run the implementation and generating bit stream.

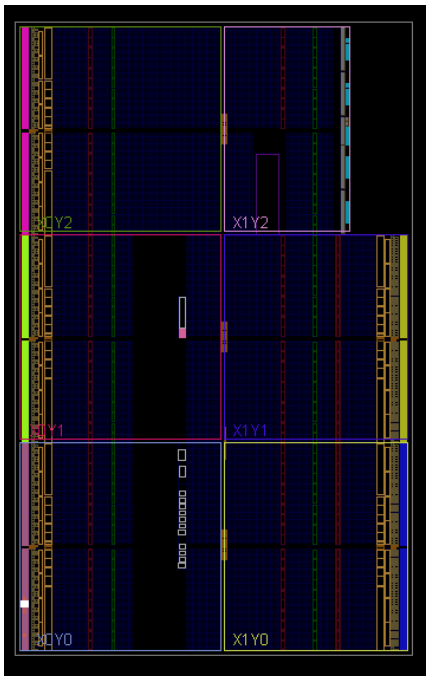



*Figure 6 – Implemented design*

After everything the hardware was open to program the board.

## Results

- Present the results recorded from the investigation.

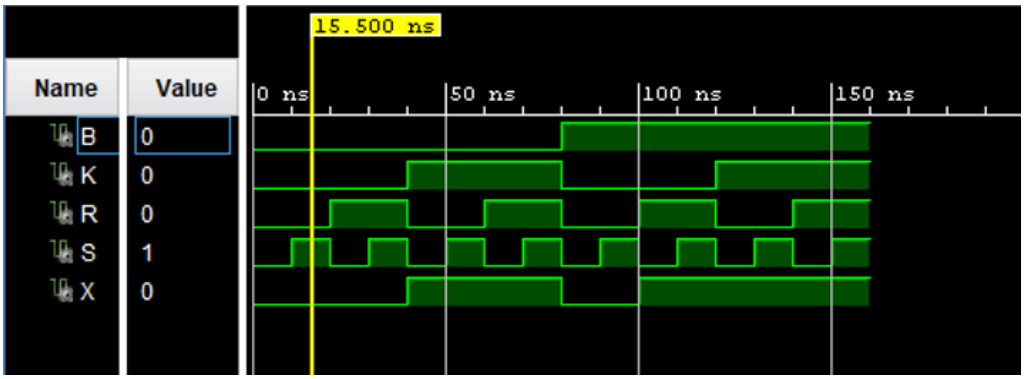



*Figure 7 – simulation*

The result of the comparator can be seen on the BASYS 3 board, shown below in the photo. The board shows the logic when four switches takes their logic the light turn as shown below.

| Truth Table | | | |
|---|---|---|---|
| Design | | Performance Check | |
| BKRS | OUTPUT? | Simulation OK? | Hardware OK? |
| 0000 | | 0 | 0 |
| 0001 | | 0 | 0 |
| 0010 | | 0 | 0 |
| 0011 | | 0 | 0 |
| 0100 | ~BK~R~S | 1 | 1 |
| 0101 | ~BK~RS | 1 | 1 |
| 0110 | ~BKR~S | 1 | 1 |
| 0111 | ~BKRS | 1 | 1 |
| 1000 | | 0 | 0 |
| 1001 | | 0 | 0 |
| 1010 | B~KR~S | 1 | 1 |
| 1011 | B~KRS | 1 | 1 |
| 1100 | BK~R~S | 1 | 1 |
| 1101 | BK~RS | 1 | 1 |
| 1110 | BKR~S | 1 | 1 |
| 1111 | BKRS | 1 | 1 |

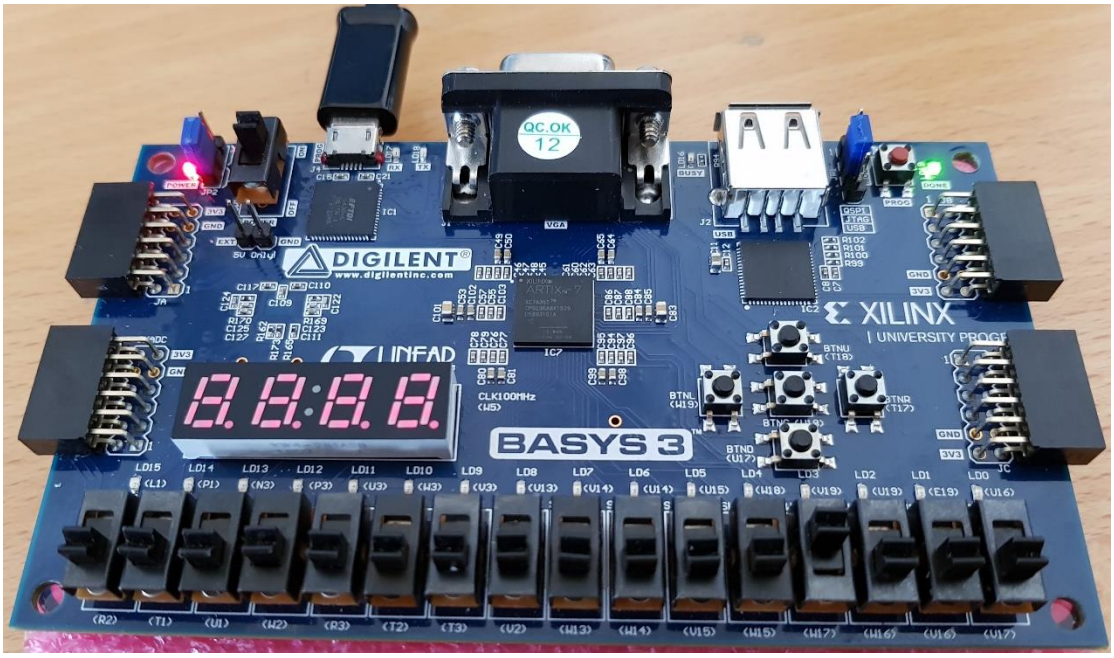



*Figure 8 – Logic 1*

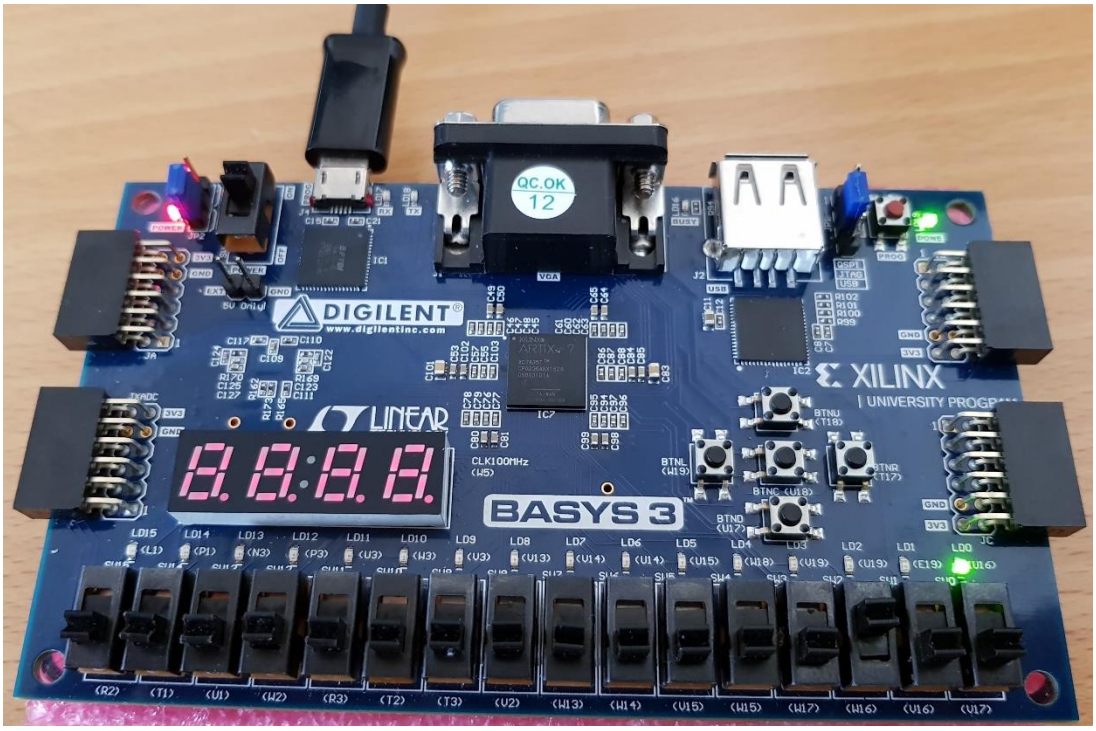



*Figure 9 – Logic 2*

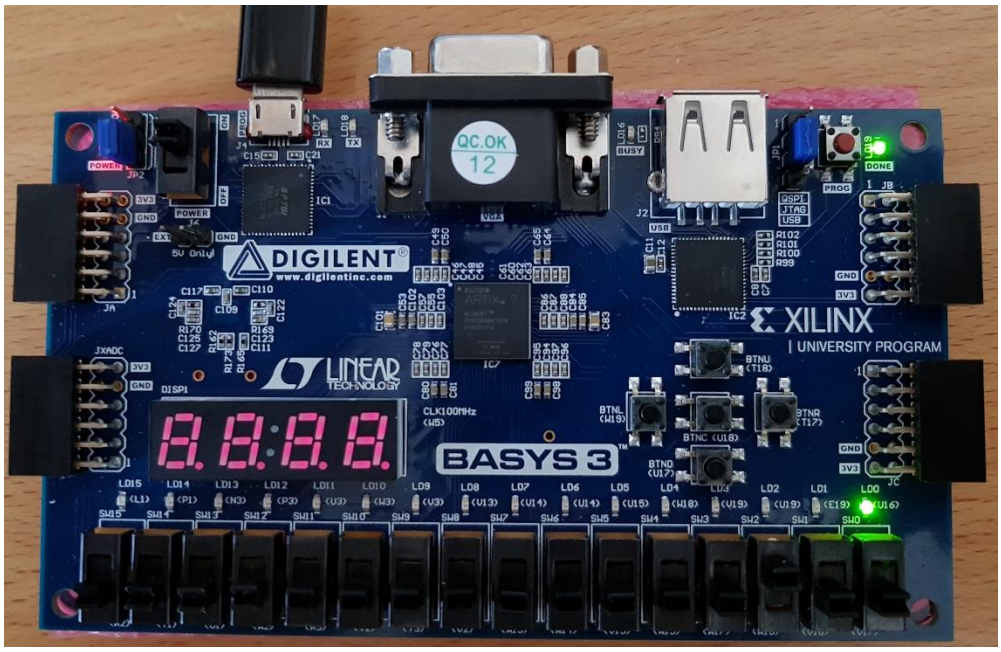



*Figure 10 – Logic 3*

## 3.0 Analysis

- Provide some comments that interpret what the results indicate or prove.

  The simulate and hardware result proves the combination logic gate works flawlessly on the board as well as on the Vivado.

## 4.0 Conclusions

- Develop the conclusion to convincingly state any understanding gained from the results or the research findings.

  The knowledge about the board is increased, this lab helped me to get to learn how to program the BASYS 3 and learned how to use Vivado.

  The most things learned while watching few videos during the lab about the Basys 3 board. This board has a lot good capabilities such as, 20,800 6-input Look Up Tables, 41,600 flip-flops, 1800 Kbits of fast block Ram, 90 DSP slices and On-chip analogue/digital converter. The more important I have learned is how to simulate the in Vivado.

  Can you suggest how to improve the laboratory exercise?

  The labaratory exercise can be improved by involving more practical work, for e.g if students are learning something about electronics BASYS 3 theorys, it is important to work practically to be able to understand better which helps to gain knowledge same as improves practical work experince.

## 5.0 References

- Use the IEEE citation style.

Electronics Tutorials – Combinational Logic Circuit :

https://www.electronics-tutorials.ws/combination/comb_1.html

Submission Checklist

1. The cover page is appropriately complete. ☒
2. The six sections in the body of the report are complete. ☒
3. The constructive feedback from a collaborator is addressed. ☒
4. A final spell-check is completed. ☒
5. A backup copy of the report is online. ☒