OLLSCOIL TEICNEOLAÍOCHTA BHAILE ÁTHA CLIATH
TECHNOLOGICAL UNIVERSITY DUBLIN

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

Programme: DT008 / 2
ELEK2108 Electronics 1
Laboratory Technical Report

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Laboratory Number:	**B**
Semester Week Number:	**3**
Date:	**11/02/2019**

Submission Checklist and Declaration

To ensure that the focus of the assessment of your laboratory report can include the development of higher order skills and competences associated with a Level 7 qualification, please complete the checklist and declaration below.

I declare that the report that I am submitting:	**Confirm**
• is my original work, with secondary sources acknowledged;	☒
• was proofread thoroughly for typographical errors;	☒
• contains citations with references formatted in the IEEE citation style.	☒
I understand that my work can be returned uncorrected if the criteria are unfulfilled.	

Signature:

1.0 Laboratory Aim

- Describe the purpose of the laboratory or the research.

  The aim of this lab is to use the Vivado Design Environment to design simulate and synthesise a digital comparator circuit.

  The purpose of this lab was to get familiar with the Vivado application and how to use it to program BASYS 3 and more importantly get to know how to program BASYS 3 via Vivado.

  In this lab we programed BASYS 3 with the help of Vivado to perform a XNOR gate logic.

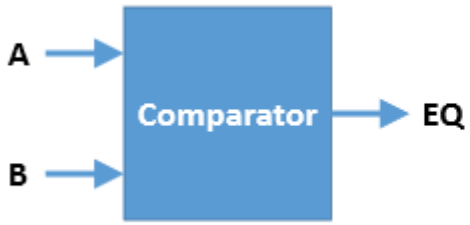
  The functionality of the finished design will be tested by implementing it and programming it onto the Artix-7 FPGA of the Digilent Basys 3 board.

2.0 Laboratory Procedure

- Describe the actions taken during the work.

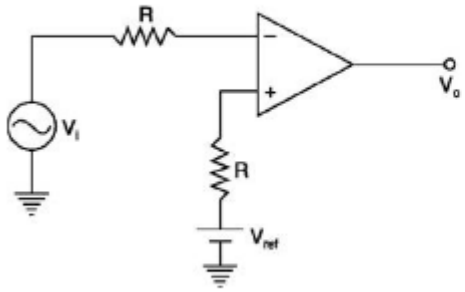
  The lab action that was taken during the lab, Creating the VHDL design sourse code, create a VHDL simulate code to test the design.

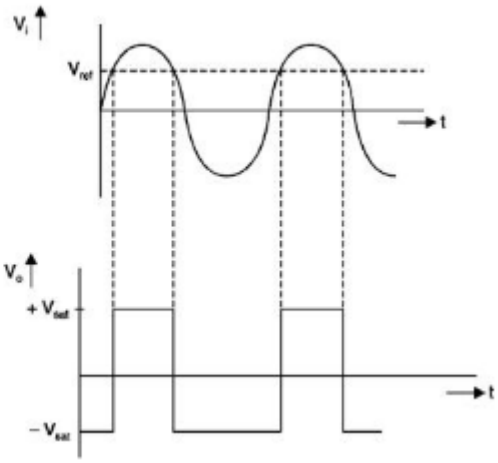
  Implemnent the design on the Basys 3 development board on Artix-7 FPGA and apply signals to the board via the switches to confirm that the design works as planned. The comparator that is used in this circuit is a XNOR logic gate which means it depends on the 2 inputs to determine the output signal, as shown in the diagram below.



A	B	EQ
0	0	1
0	1	0
1	0	0
1	1	1

The output of the analogue comparator is high when the input of a signal equals or exceeds the reference signal.

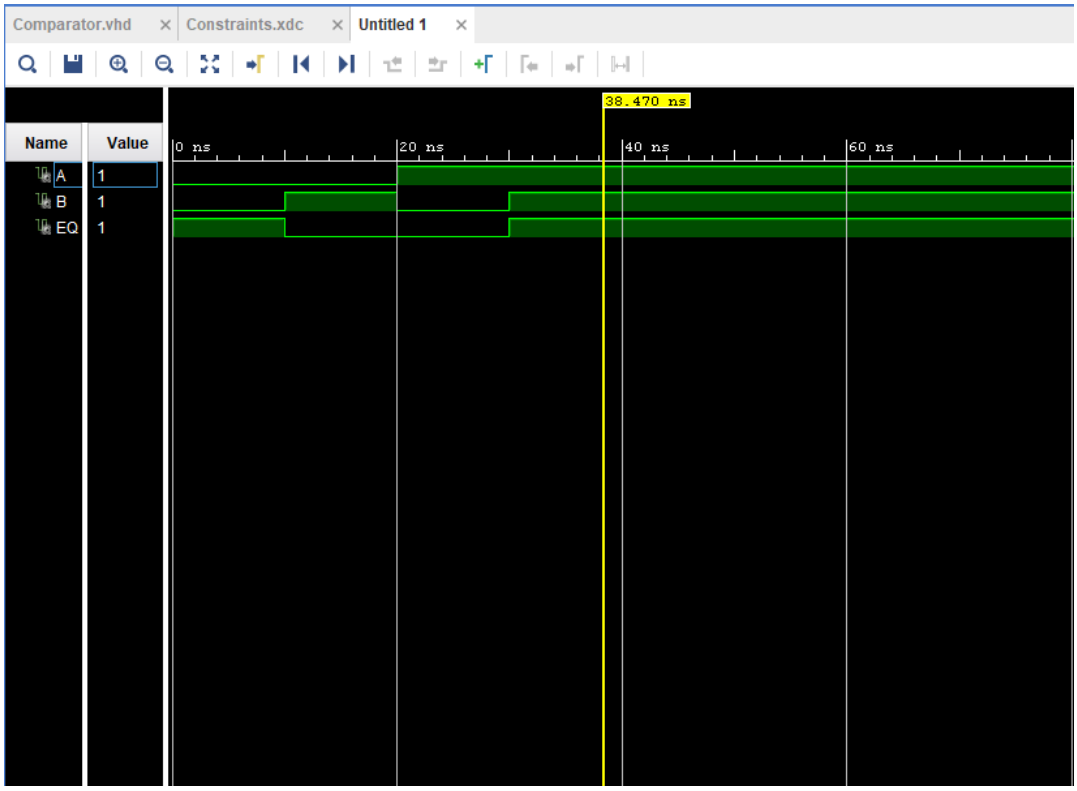




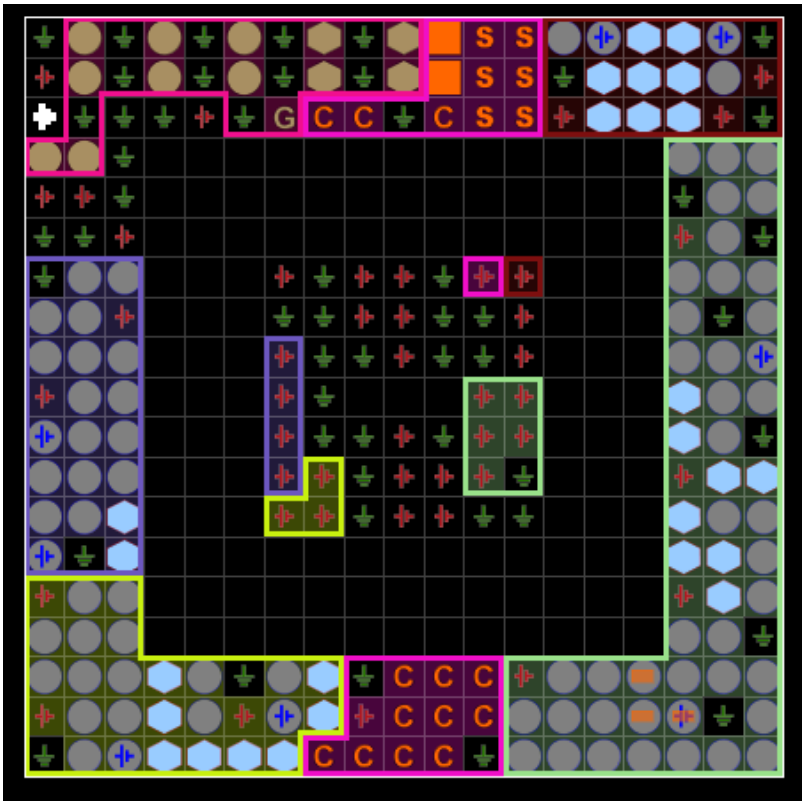
The new project was created in order to program the board and simulate. The test bench source file was created “Compared_TB” to set the I/O ports, then the following link was used in order to generate VHDL code with the help of source code.

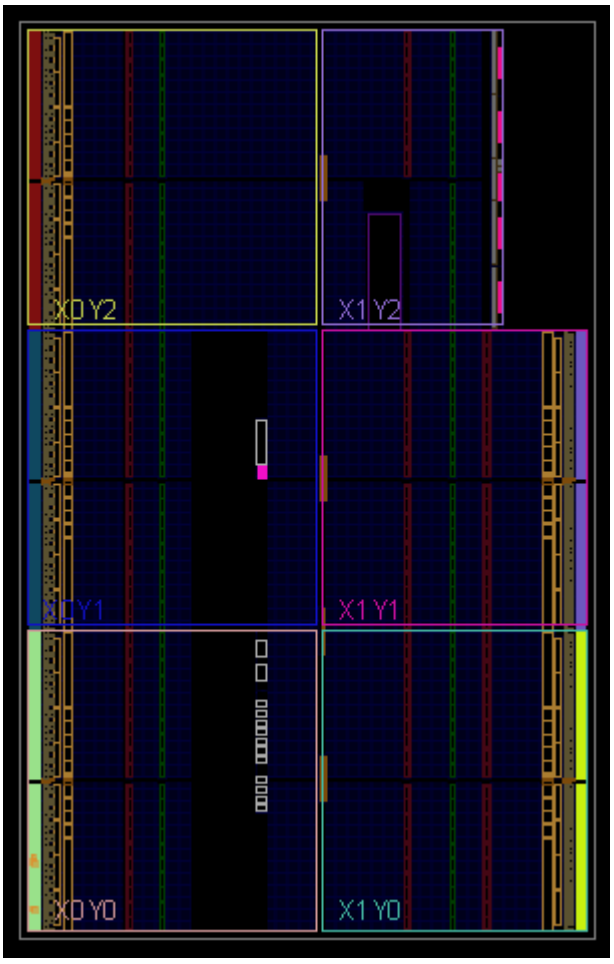
https://www.doulos.com/knowhow/perl/testbench_creation/

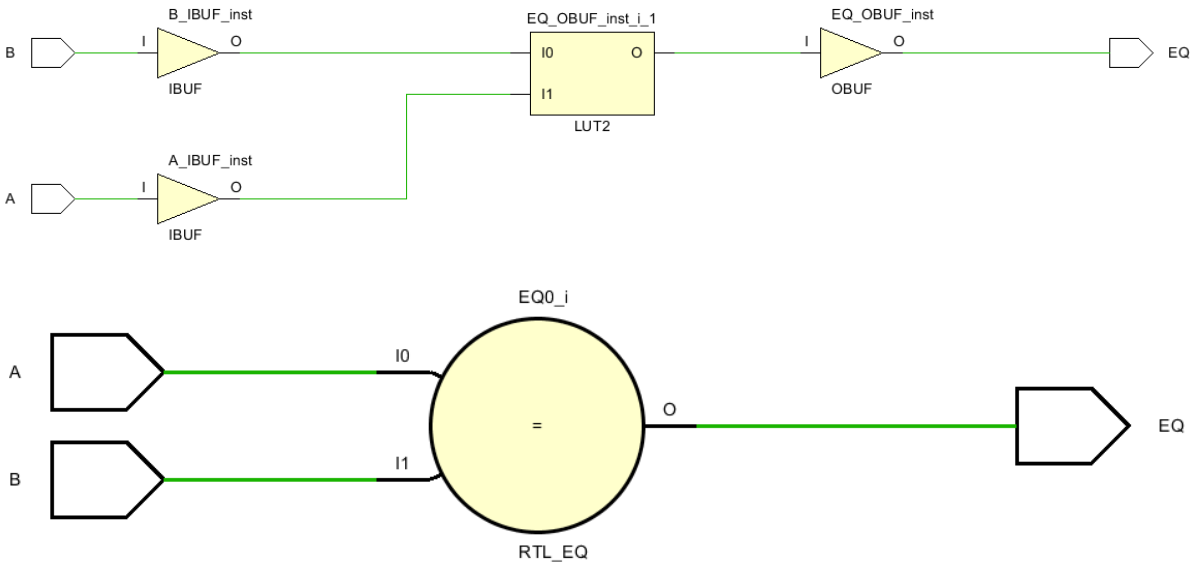
The simulate run time was set to 100 ns to run the behavioural simulation. The result of the simulation shows that if we receive 1 in both inputs then we will receive 1 in the output.



The elaborated design.


S S
S S
G C C C S S
C C C
C C C
C C C C

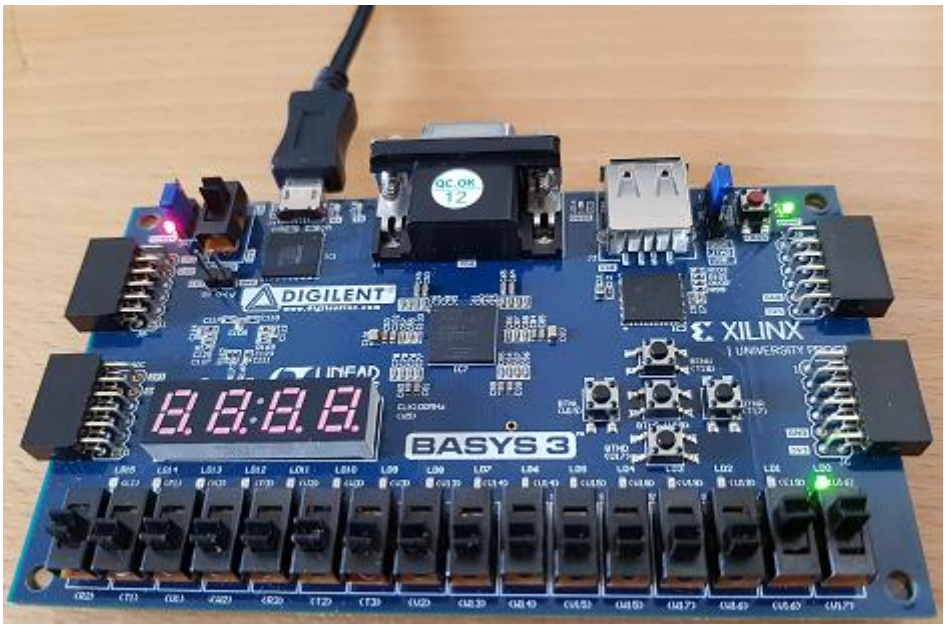

X0 Y2
X1 Y2
X0 Y1
X1 Y1
X0 Y0
X1 Y0



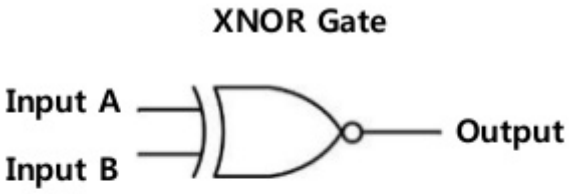
3.0 Results

- Present the results recorded from the investigation.

  The result of the comparator can be seen on the BASYS 3 board, shown below in the photo. The board shows the logic when both switch are on the light turn as shown bottom right coroner.



The XNOR gate is a digital logic gate whose function is the logical complement of the exclusive OR gate. The two-input version implements logical equality, behaving according to the truth table shown below.



Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	1

A ⊙ B = Y

4.0 Analysis

- Provide some comments that interpret what the results indicate or prove.

  The result proves that logic XNOR gate works flawlessly on the board as well as on the Vivado. The result show that if we receive both positive (1) inputs the output will be positive (1) and if we receive both negative (0) inputs then the output will be also positive, However if the comparator receive 1 positive input the logic output will be low (0). The board proves that well.

5.0 Conclusions

- Develop the conclusion to convincingly state any understanding gained from the results or the research findings.

  The knowledge about the board is increased, this lab helped me to get to learn how to program the BASYS 3 and learned how to use Vivado.

  The most things learned while watching few videos during the lab about the Basys 3 board. This board has a lot good capabilities such as, 20,800 6-input Look Up Tables, 41,600 flip-flops, 1800 Kbits of fast block Ram, 90 DSP slices and On-chip analogue/digital converter. The more important I have learned is how to simulate the in Vivado.

  Can you suggest how to improve the laboratory exercise?

The labaratory exercise can be improved by involving more practical work, for e.g if students are learning something about electronics BASYS 3 theorys, it is important to work practically to be able to understand better which helps to gain knowledge same as improves practical work experince.

6.0 References

- Use the IEEE citation style.

1300 Henley Court Pullman, WA 99163 509.334.6306 www.digilentinc.com
https://reference.digilentinc.com/_media/basys3:basys3_rm.pdf

Submission Checklist

1. The cover page is appropriately complete. ☒
2. The six sections in the body of the report are complete. ☒
3. The constructive feedback from a collaborator is addressed. ☒
4. A final spell-check is completed. ☒
5. A backup copy of the report is online. ☒