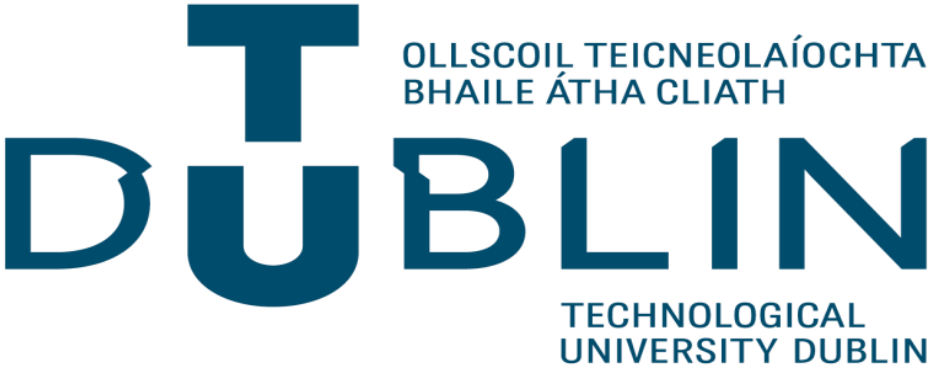

TIMEBASE BLOCK DIAGRAM

DT008/3 – Electronics 2 Laboratories

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1. Introduction

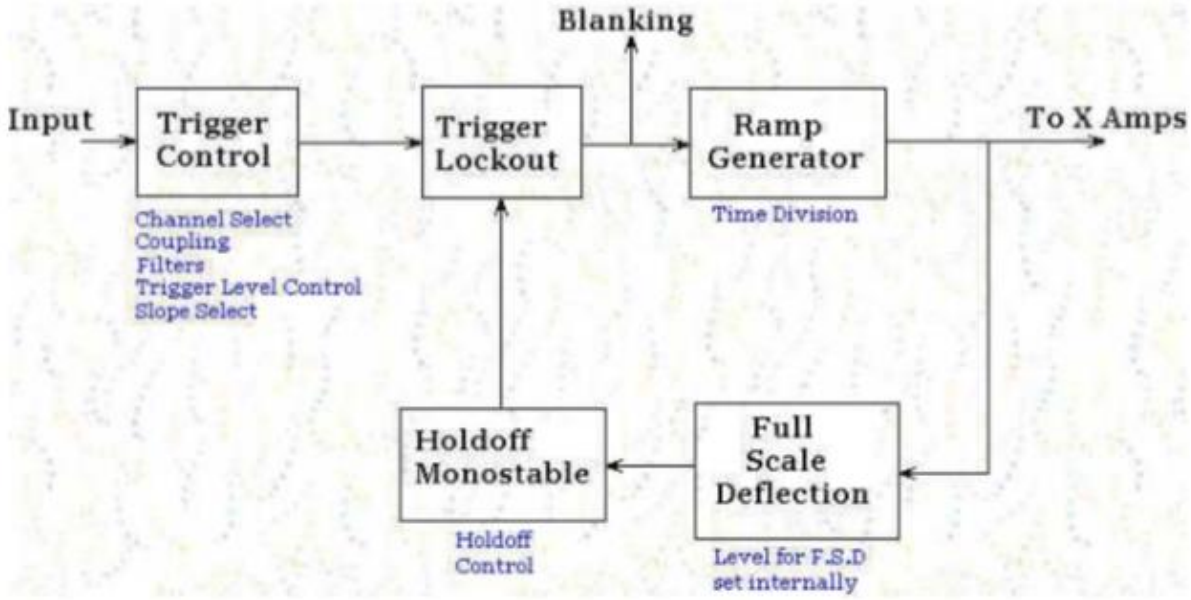


Figure 1 - Timebase circuit diagram

1.2. Procedure

1. The system shown below is a basic triggered mode oscilloscope time base circuit.

2. You are required to complete this circuit in stages as outlined in the following lab sheets.

3. Once the circuit is complete you will be required to submit an overall formal report as part of your laboratory assessment. Your laboratory supervisor will give the hand-up date to you in due course.

4. Board layout requirements, etc., will be discussed with you during the first laboratory session.

5. You must record any observations you make (good or bad) in your logbook.

6. You will be required to simulate the operation of this circuit using PSpice and compare simulation results with measured results.

7. In your summary/conclusions you are required to discuss the viability or otherwise of your results.

2. The front end of the Bootstrap circuit

Calculating appropriate values in the lab book for the resistor, R and R_B, and the capacitor C to meet the specification above, using the following equations:

- $V_C = E(1-e^{-\frac{t}{CR}})$
- $\frac{E}{CR}$ = Initial ramp slope
- $t_f = C.Vc_{max} / I_D$

The circuit diagram for the front end of the bootstrap in PSpice:

The values that are used in the circuit diagram fig. 2 are calculated in the logbook for resistor, R and R_B, and the capacitor C. The values that were calculated are:

R1 = 187500 ohms.

R_B = 10.75 k ohms.

C1 = 800 pF.

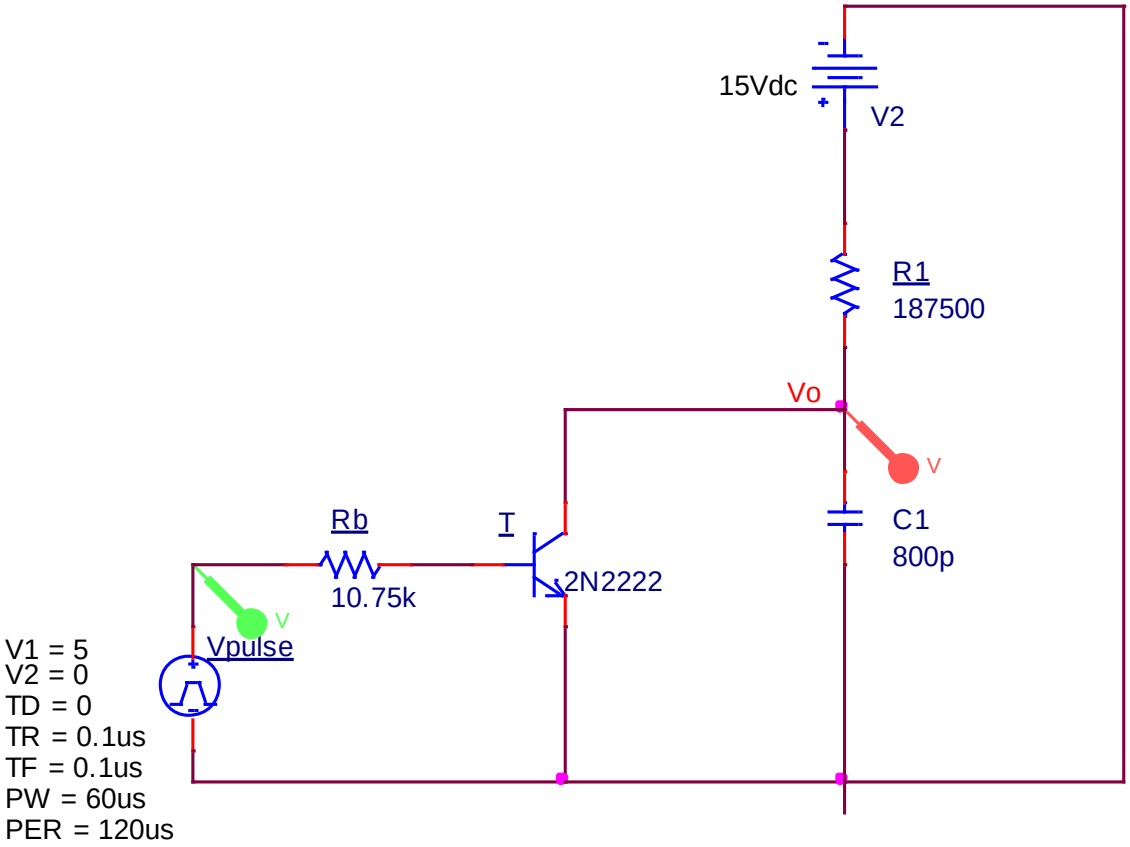
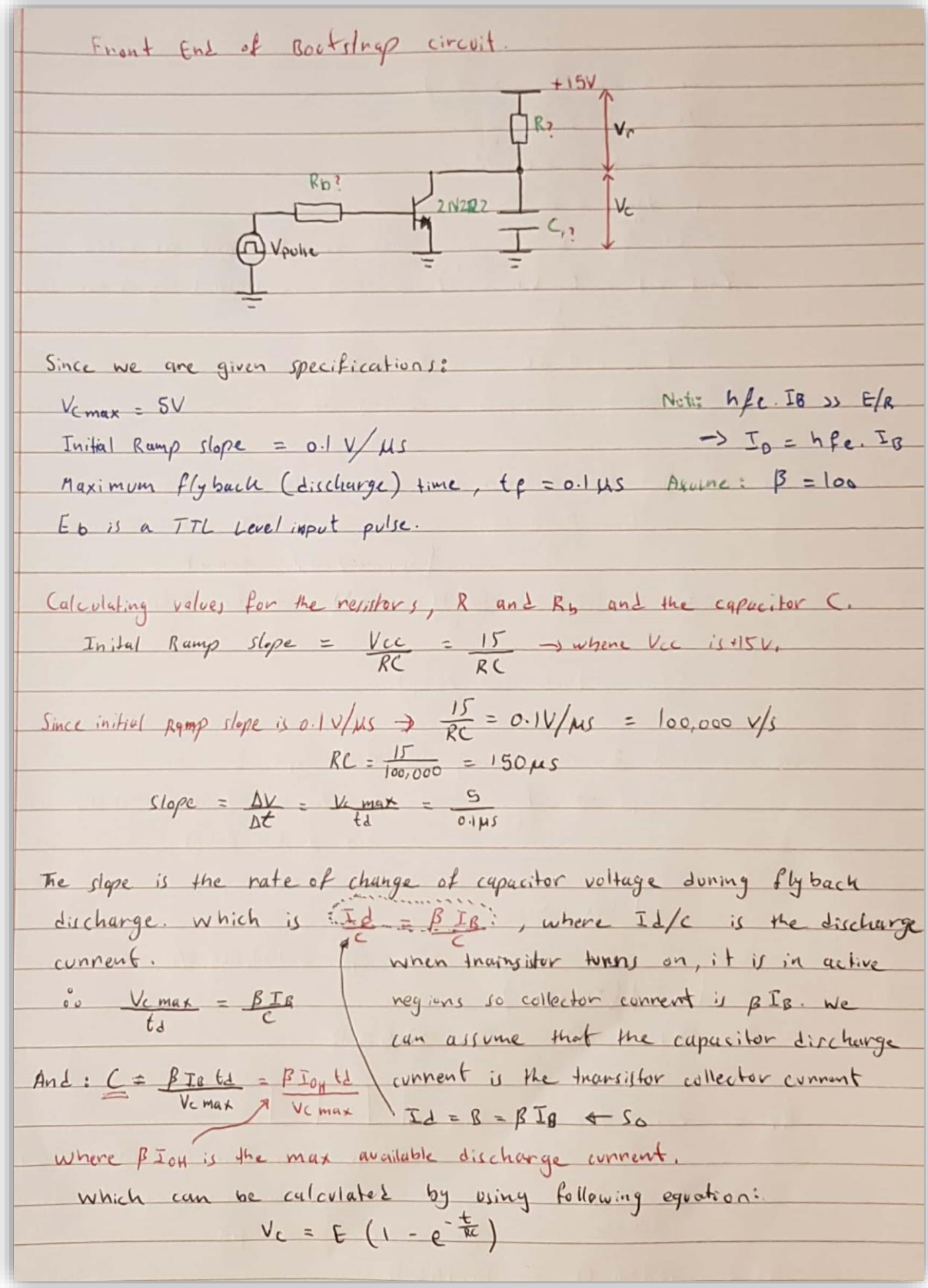


Figure 2 - Circuit diagram of the Front end of the bootstrap

Calculated values for R, R_B, and C are calculated in the logbook as shown below.



$(I_{OH\ Max}) = 400\mu A$ - setting the max available base current for T.

Since we got the formula for C1, which is

$C_1 = \frac{\beta I_B t_d}{V_{c\,max}}$ - Assume $\beta = 100$

$I_{OH\ Max} \Rightarrow I_B = 400\mu A$

$C_1 = \frac{100(400\times10^{-6})(0.1\times10^{-6})}{5}$ → $t_d = 0.1\mu s$ → $V_{cmax} = 5V$

$C_1 = 0.8nF \Rightarrow 800pF$

we can find R when using the initial slope formula:

Initial Slope $= \frac{E}{RC_1}$ → $E = V_{cc} = 15V$, Initial Slope $0.1/\mu s$

R ?, $C = 800pF$

$R = \frac{E}{\text{Initial slope} \cdot C_1}$

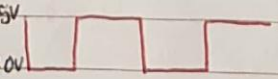
$R = \frac{15}{\left(\frac{0.1}{10^{-6}}\right)(800\times10^{-12})}$ Slope $= \frac{0.1}{10^{-6}} = 100,000\ V/s$

$R = 187500\ \Omega \Rightarrow 187.5K\Omega$

$R_B = \frac{V_{in} - V_{BE}}{I_B}$

$= \frac{5 - 0.7}{400\times10^{-6}}$

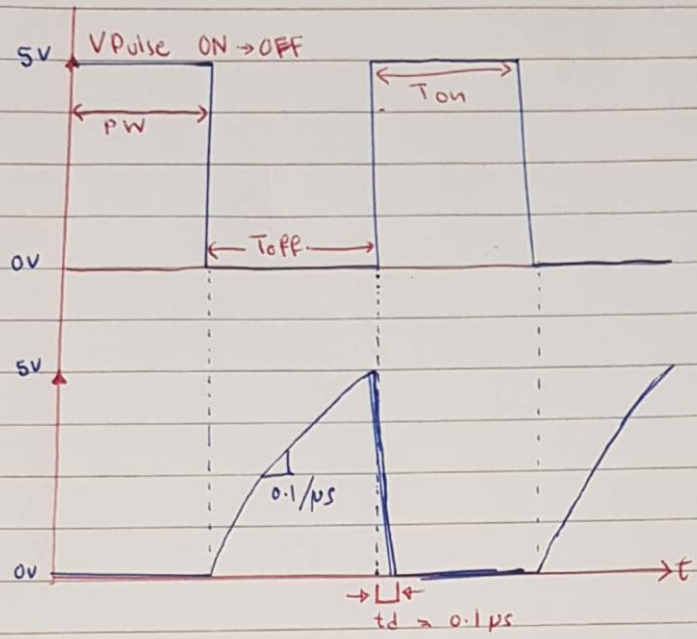
$R_B = 10750\ \Omega \Rightarrow 10.75K\Omega$



V_{in}

V_{BE} = Voltage across Base to emitter is 0.7V due to the diode, which requires 0.7V to turn on.

$I_B = I_{OH} = 400\mu A$



when the transitor (2N2222) turns off, means, when the Pulse is at 0V, Then the Capacitor charges due to voltage coming from 15Vdc throw resistor. The voltage in the capacitor rises expenentialy providing the Voltage ramp given by this formula.

t_{ramp}

$$V_{C,max} = E\left(1 - e^{-\frac{t}{RC}}\right)$$

$$\frac{V_c}{V_{cc}} = 1 - e^{-\frac{t}{RC}}$$

$$\frac{V_c}{V_{cc}} - 1 = -e^{-t/RC}$$

$$1 - \frac{V_c}{V_{cc}} = e^{-\frac{t}{RC}}$$

$$\left(1 - \frac{5}{15}\right) = e^{-\frac{t}{RC}} \rightarrow \text{Since } V_c = 5V \text{ and } V_{cc} = 15V$$

$$\ln\left(\frac{2}{3}\right) = \ln\left(e^{-t/RC}\right) \rightarrow \text{taking the log of both side}$$

$$-0.4 = -\frac{t}{RC}$$

$$t = 0.4\,RC \Rightarrow RC = 150\mu s$$

$$t = 0.4(150 \times 10^{-6})$$

$$t = 60\mu s$$

$$187500\,(800 \times 10^{-12}) = RC$$

$$RC = 0.15ms \Rightarrow 150\mu s$$

The calculation shown above is for calculating time ramp (t_{ramp}), t_{ramp} is the time, that transistor needs to stay off, so that the Capacitor can change up to 5v, depending on, how long the transistor takes to stay switched off.

The simulated PSpice “Front end of the bootstrap” circuit diagram shows the voltage pulse and Vc1 voltage.

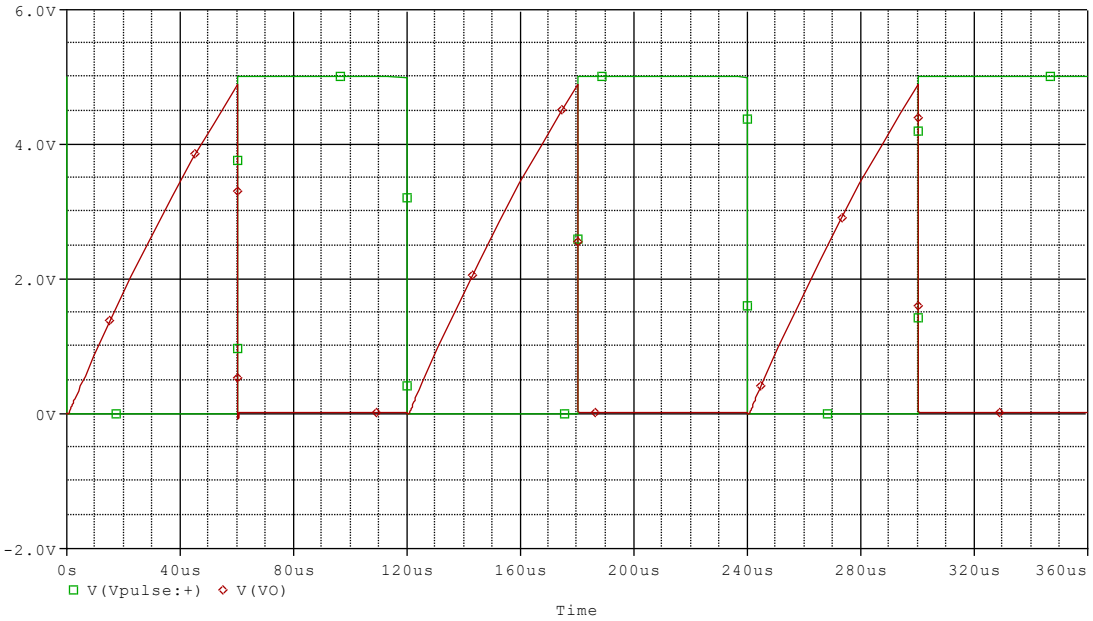


Figure 3 - Simulated circuit shows the voltage ramp generated in red & pulse voltage in green

The capacitor begins to charge when the transistor receives low (0v) input to the base from the pulse. The voltage in the capacitor begins to rise and reaches up to 5v constant. As soon as the transistor receives a high (5v) pulse throw the R_B into the base of the transistor, current flows from the base to the emitter (0.7v), turns on the diode which closes the junction allowing current passing throw from collector to emitter, so all the current goes to the ground which discharges the capacitor.

The ramp time was also calculated to be ***60us*** to give the voltage ramp enough time to reach 5v.

The time that takes to discharge is measured in the simulation to be approximately **0.12us** which is very close to the expected value.

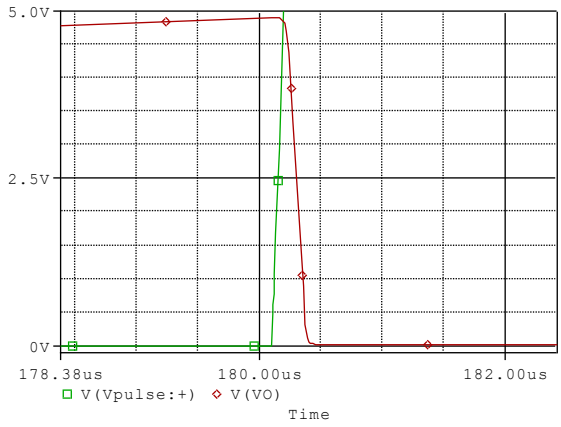
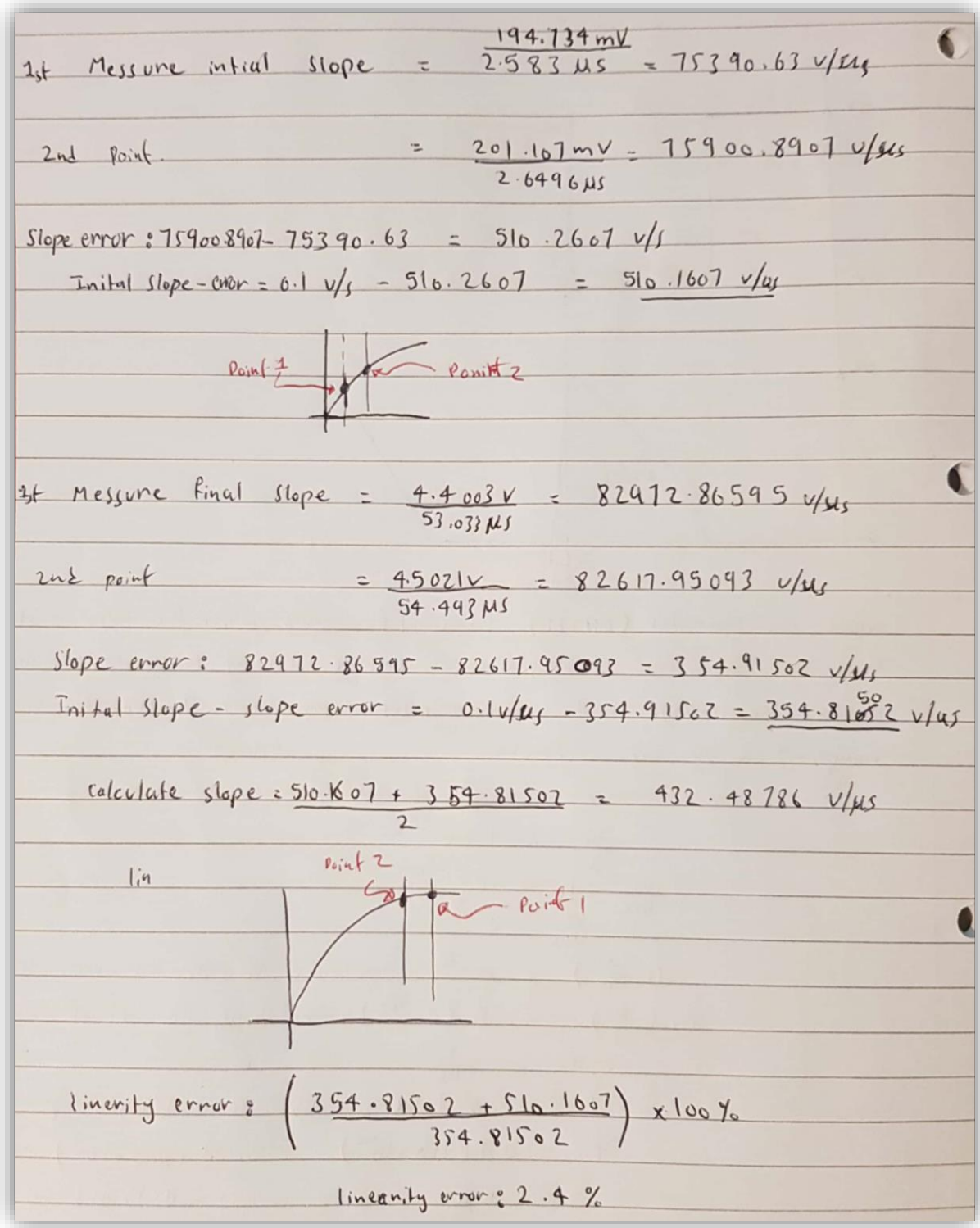


Figure 4 - Propagation delay (time delay)

The time delay is hard to notice in fig.3, however, fig. 4 shows the propagation delay clearly. There is also an unexpected small spike in voltage after the transistor is turned on and similarly a small dip in the voltage when the capacitor fully discharges. This is due to the distance and materials in the junction which affects the junction of the transistor and every type of transistor has different effects on their switching on and off-speed. It can cost more if switching is a priority.

The front end of the bootstrap circuit diagram does meet the specifications.

Measured slope and linearity:



2. Bootstrap Ramp Generator

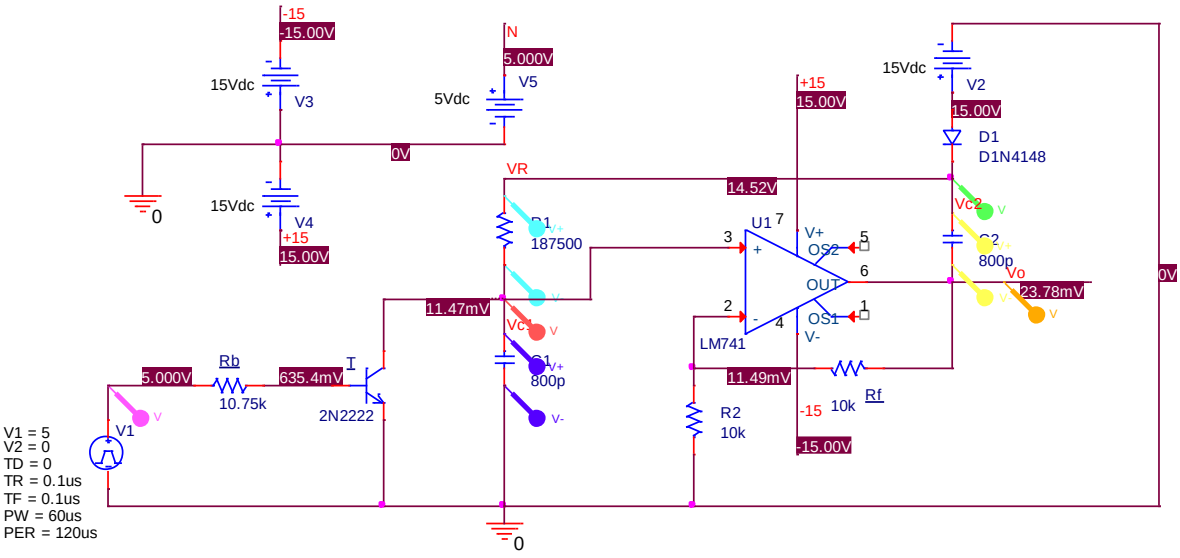


Figure 5 - Circuit diagram of Bootstrap Ramp Generator

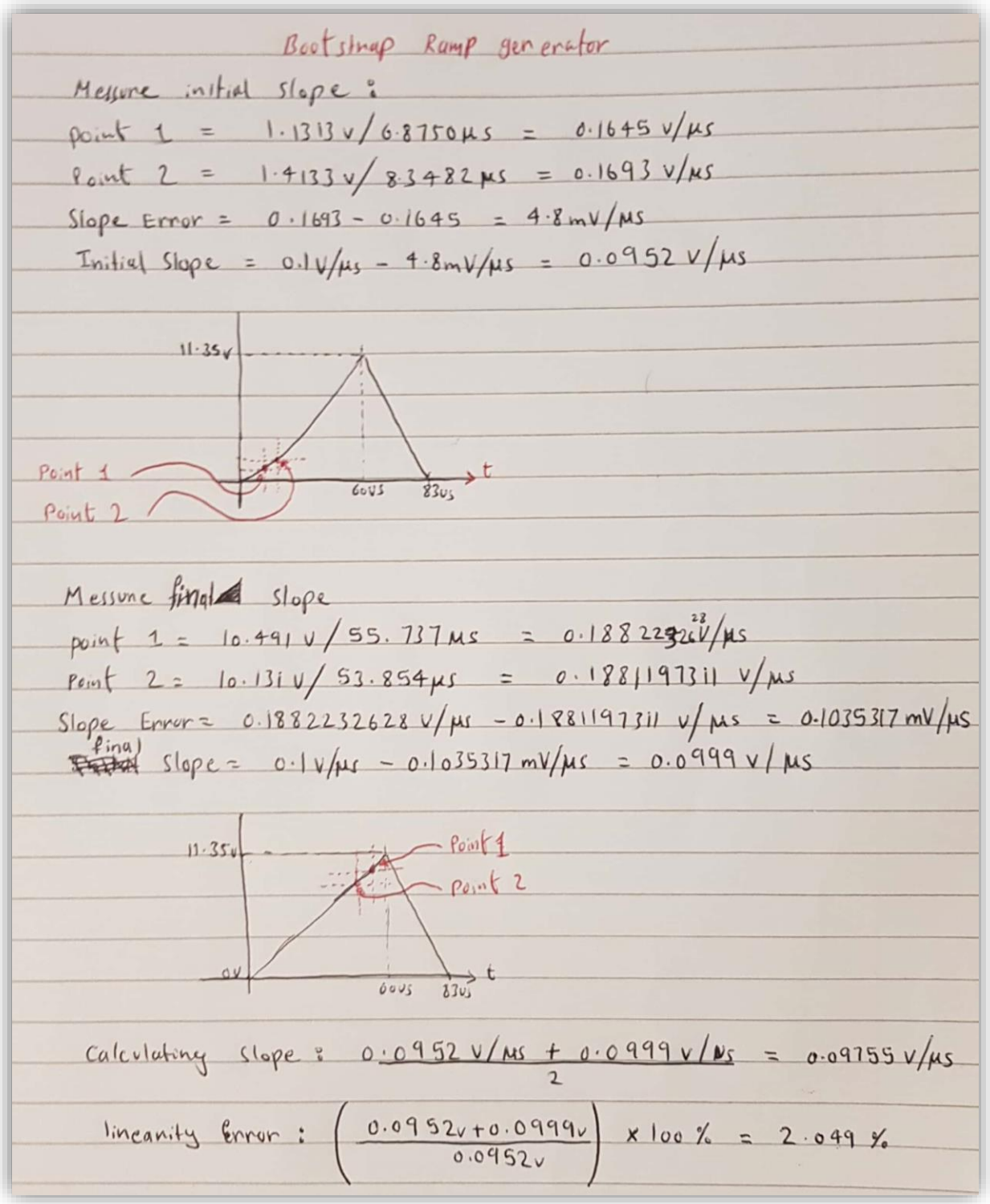
This is a bootstrap ramp generator that uses an (LM741) op-amp, which is necessary to generate a sufficiently high voltage ramp to move the electron beam in the cathode ray tube across the small screen. The amplifier is used to boost the signal to get the constant ramp with a gain of 2.
The configuration of the op-amp is a non-inverting amplifier. Which has a gain of **2**, because the gain is dependent on Rf and R2.
Where Rf = 10k, R2 = 10k.

$$Gain = 1 + \frac{R_f}{R2}$$

$$Gain = 1 + \frac{10k}{10k} = 2$$

The flyback time must be greater than the discharge time, this is due to the gain factor of the op-amp. This is shown in the simulated Vout.

Measuring the slope of the amplified and its linearity at the output voltage (Vout).



With the bootstrap ramp generator circuit, the voltage becomes much more linear. But the voltage ramp reaches a higher voltage before C1 discharges.

The output (Vout) in orange colour and voltage across the capacitor (Vc1) in red colour is shown in fig. 6.

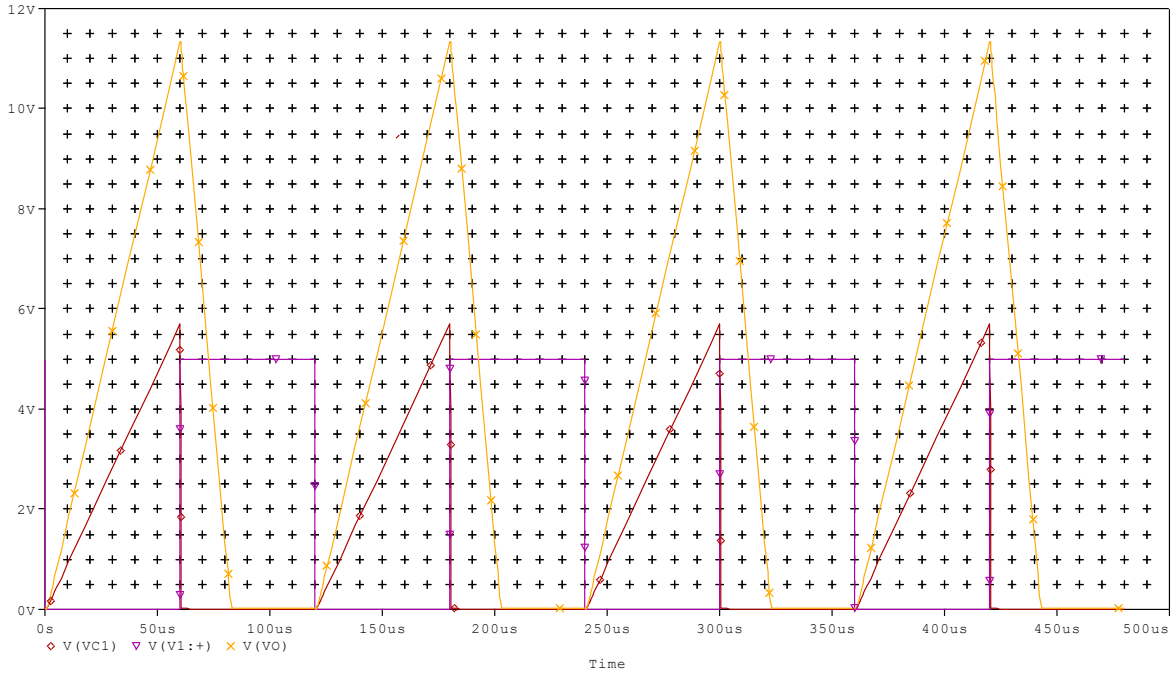


Figure 6 - Comparing the Vc1 vs output (Vout) of the bootstrap ramp generated

The Vout is doubled due to the gain of 2. Vout = 2*Vc1. The output of the op-amp is boasted signal, from C1, so the signal is amplified with the gain of 2 to get the amplified ramp signal (Vout).

The flyback time of (Vout = 23.797us) is much greater than the discharge time due to the gain and slew rate of the (LM741) ap-amp. Flyback is the time, that takes the capacitor to discharge when the transistor turns on from the Vpulse as shown in the purple colour in fig. 6.

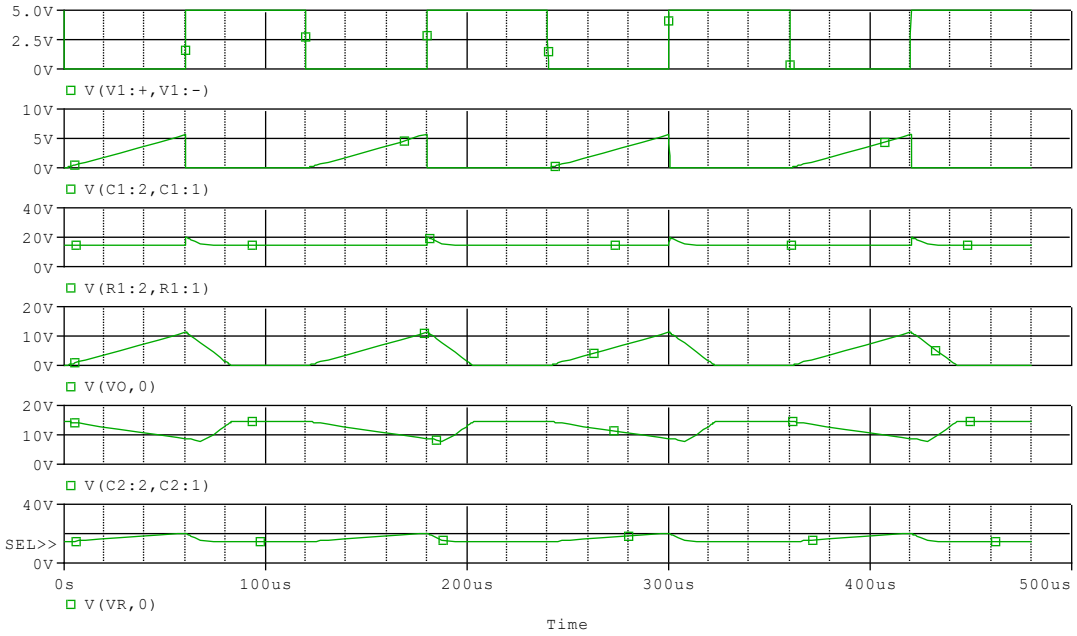


Figure 7 - Plot waveforms for Eb, Vc, Vr, Vo, Vc2, Vx

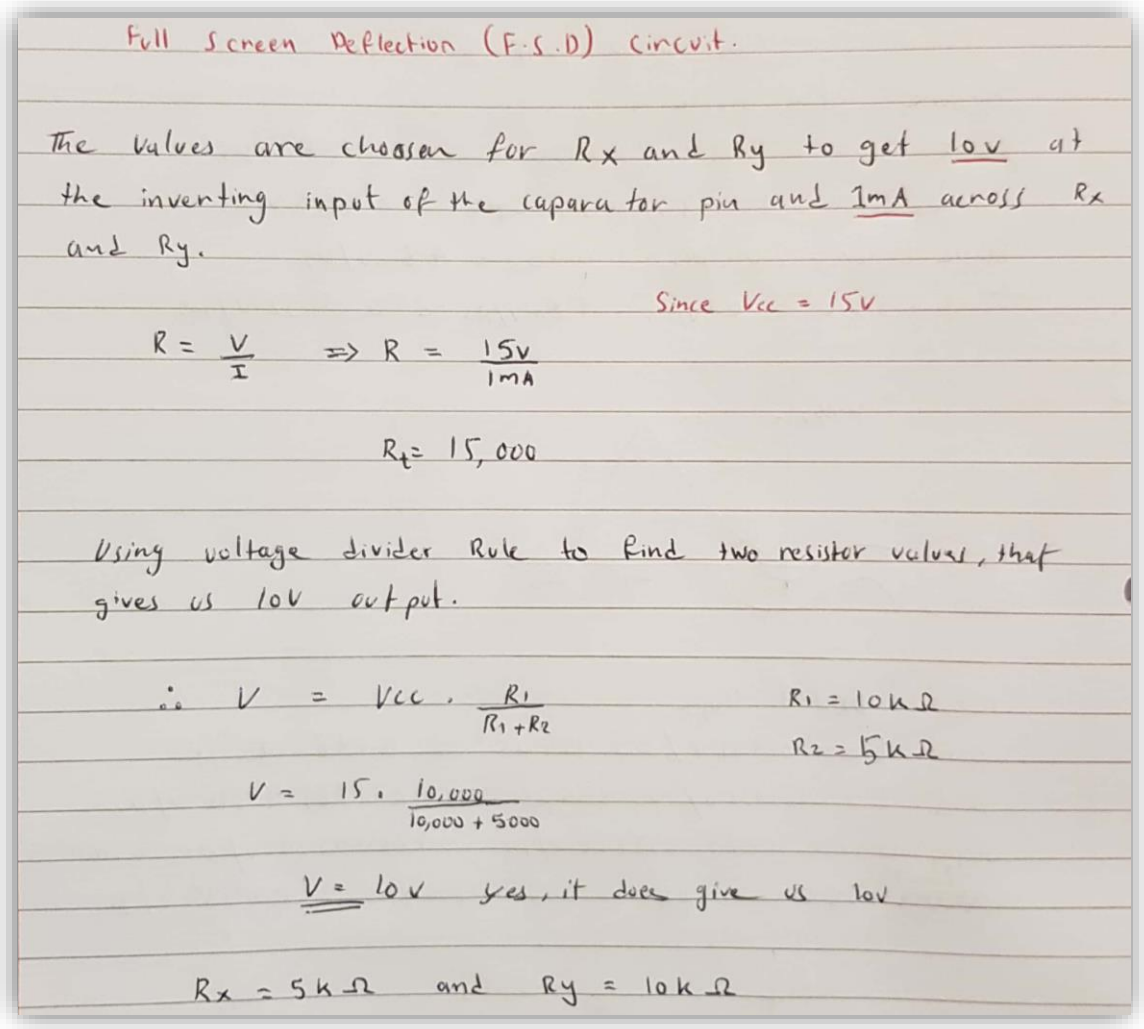
When the transistor gate closes, the current from Vcc passes through the capacitor 1 must be constant to get the linear voltage ramp at Vc. This constant current is ensured by keeping a constant voltage across the resistor R(Vr).

When the transistor turns off the voltage in Vc1 rises and at the same time Vc2 discharges its voltage after being charged by the +15v supply and increases the voltage across the resistor R.

Both capacitors have equal capacitance causing one to charge at the same rate as the other one discharges. Vc2 discharges slower due to the slew rate of the LM741 op-amp.

3. Full-Screen Deflection (F.S.D) Circuit

The logbook appropriate calculated values are shown below.



Full screen Deflection (F.S.D) circuit.

The values are choosen for Rx and Ry to get 10v at the inverting input of the capacitor pin and 1mA across Rx and Ry.

Since Vcc = 15V

$R = \frac{V}{I} \Rightarrow R = \frac{15v}{1mA}$

$R_t = 15,000$

Using voltage divider Rule to find two resister values, that gives us 10V output.

$\therefore V = Vcc \cdot \frac{R_1}{R_1 + R_2}$

$R_1 = 10k\Omega$

$R_2 = 5k\Omega$

$V = 15 \cdot \frac{10,000}{10,000 + 5000}$

$V = 10v$ yes, it does give us 10V

$Rx = 5k\Omega$ and $Ry = 10k\Omega$

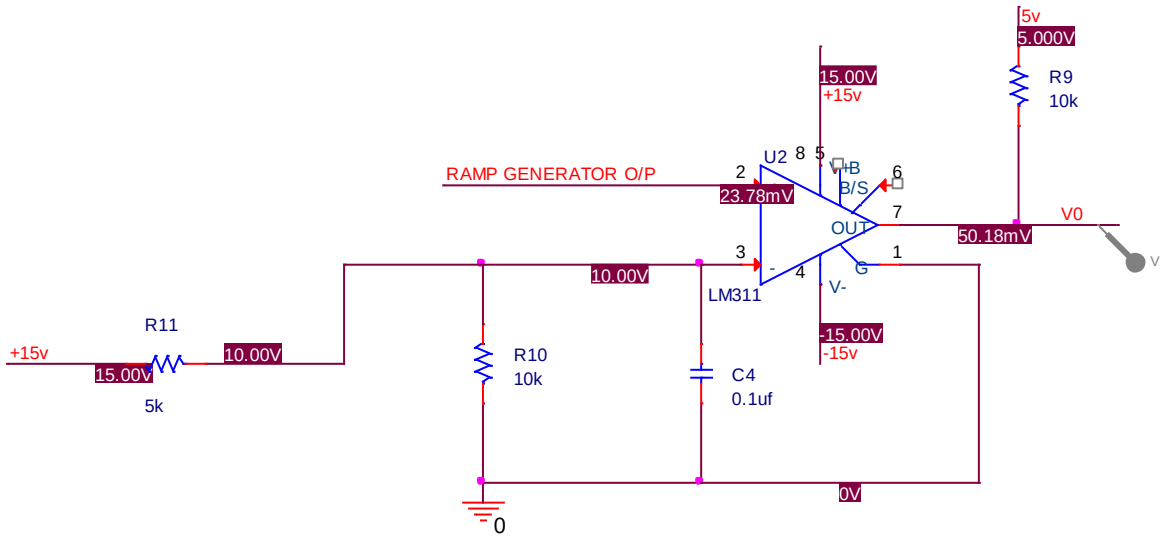


Figure 8 - Circuit diagram of full-screen deflection (F.S.D)

The values for the resistors calculated in the log turned out to be:

Rx = 10k ohms

Ry = 5k ohms

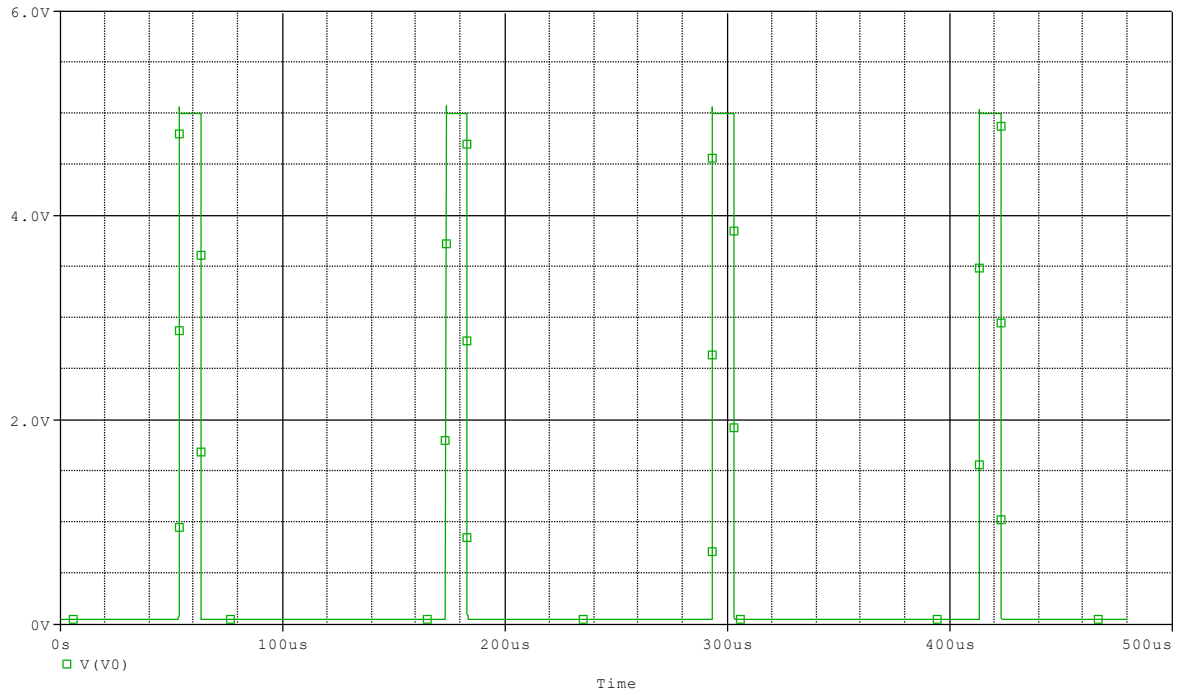


Figure 9 - Output of the full-screen deflection

The green waveform represents FSD output. As the voltage ramp reaches 10v the FSD circuit switches to 5v and as the voltage ramp drops below 10v the output of the FSD switches to low. That's exactly what was expected to happen.

4. Holdoff circuit

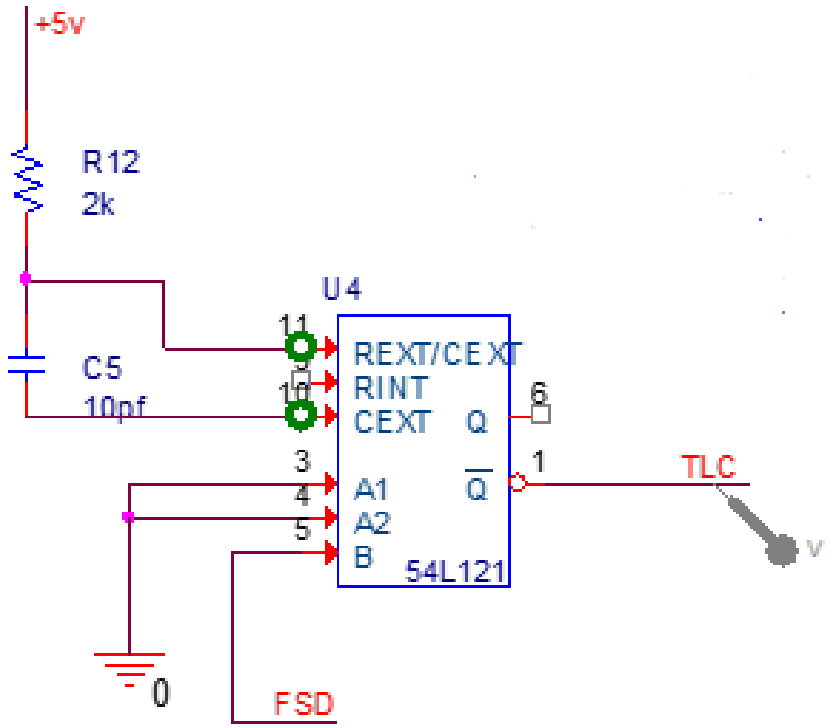


Figure 10 - The circuit diagram of the holdoff

The hold off monostable circuit is designed to reset and hold the trigger lockout circuit when the hold off circuit detects a rising edge from the FSD circuit. When the FSD output detects the rising edge and sets the output of the holdoff circuit to low. The 2 components R and C are used to determine the hold-off time of the circuit. The hold off time must be long enough to allow the voltage ramp to settle back down to its initial stage.

According to the circuit specification:

$t_{HO} \approx 0.7CR$

R in the range 2kΩ to 30kΩ

C in the range 10ρf to 10μf.

Therefore:

The hold off time = 2* flyback time = 2*23us = 46us

If a value of 15kΩ is used for the resistance for R6, then using the circuit specification we can calculate an appropriate value for capacitor C3 and therefore the appropriate RC time constant.

$$Hold\ off\ time = 0.7RC => C = \frac{Hold\ off\ time}{0.7R} = \frac{46us}{0.7(2k\Omega)} = 32.85nF$$

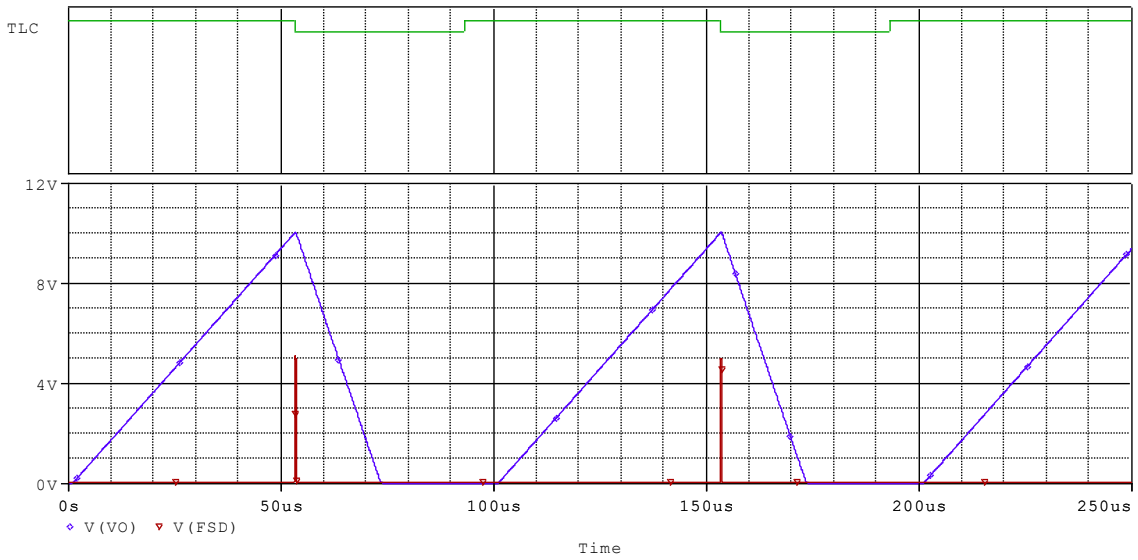


Figure 11 - HOLD OFF nonstable

The output goes low and stays low for 40us when the F.S.D goes high the holdoff.

5. The trigger lockout circuit

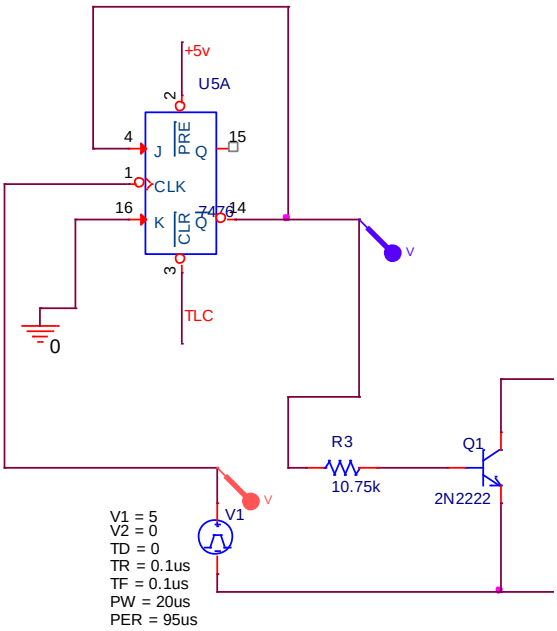


Figure 12 - Circuit diagram of the lockout

The trigger lockout circuit starts the voltage ramp whenever the flip flop is clocked by an input signal and ignores any other input after. The trigger circuit is held off until the fly back is complete.

J	K	Q
0	0	IGNORES CLOCK TRIGGER
1	0	SET

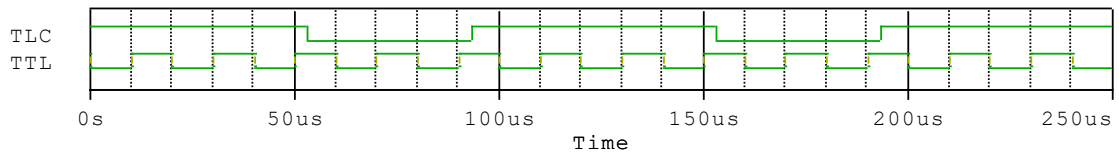
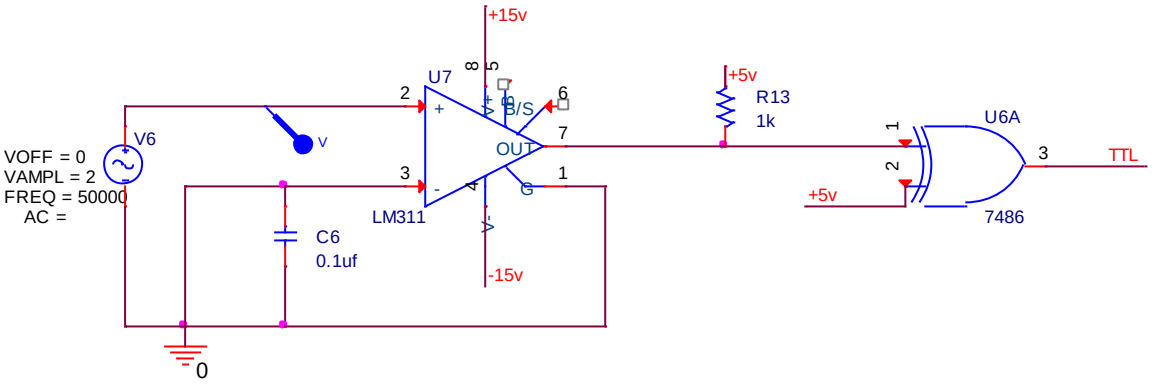
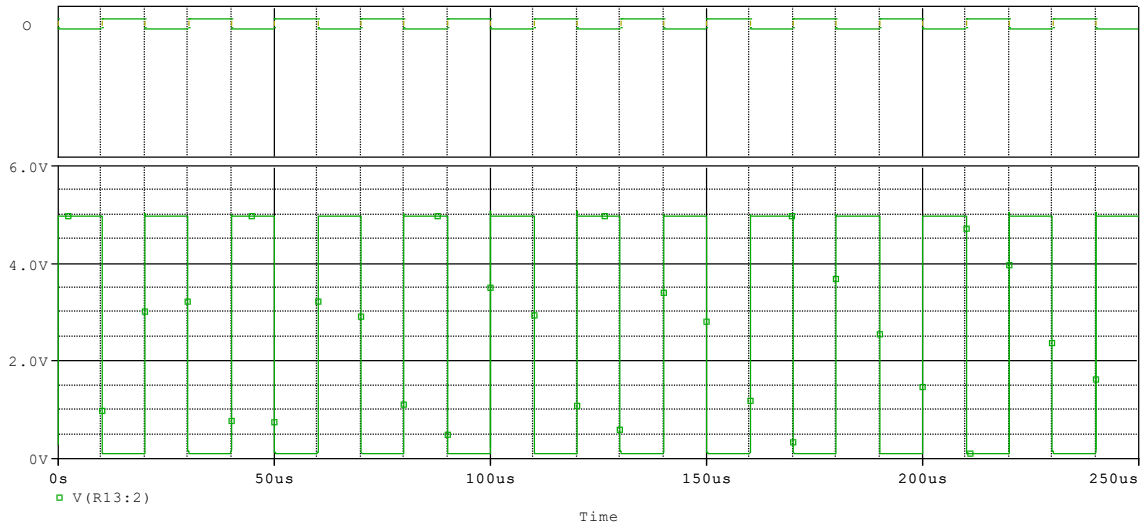


Figure 13 - Trigger control and gold off

6. Trigger control & slope select



When the slope selection is set to 5v, the ramp starts at zero when the ramp reaches 10v.



The trigger select is set to at 0v as it is connected to the ground (0v). Every time the sin wave process 0 it acts as a trigger.

Therefore, in this case, the 7.5v is the trigger level and will pull the output of the comparator high and low whenever the sinewave passes it. The XOR gate (U6A) acts as the slope select circuit. The output of the comparator is fed into one input of the XOR gate while the slope is controlled at the other input by connecting a low input (GND) or a high input (5v). Connecting 5v selects the trigger level at the positive slope while

7. Oscilloscope

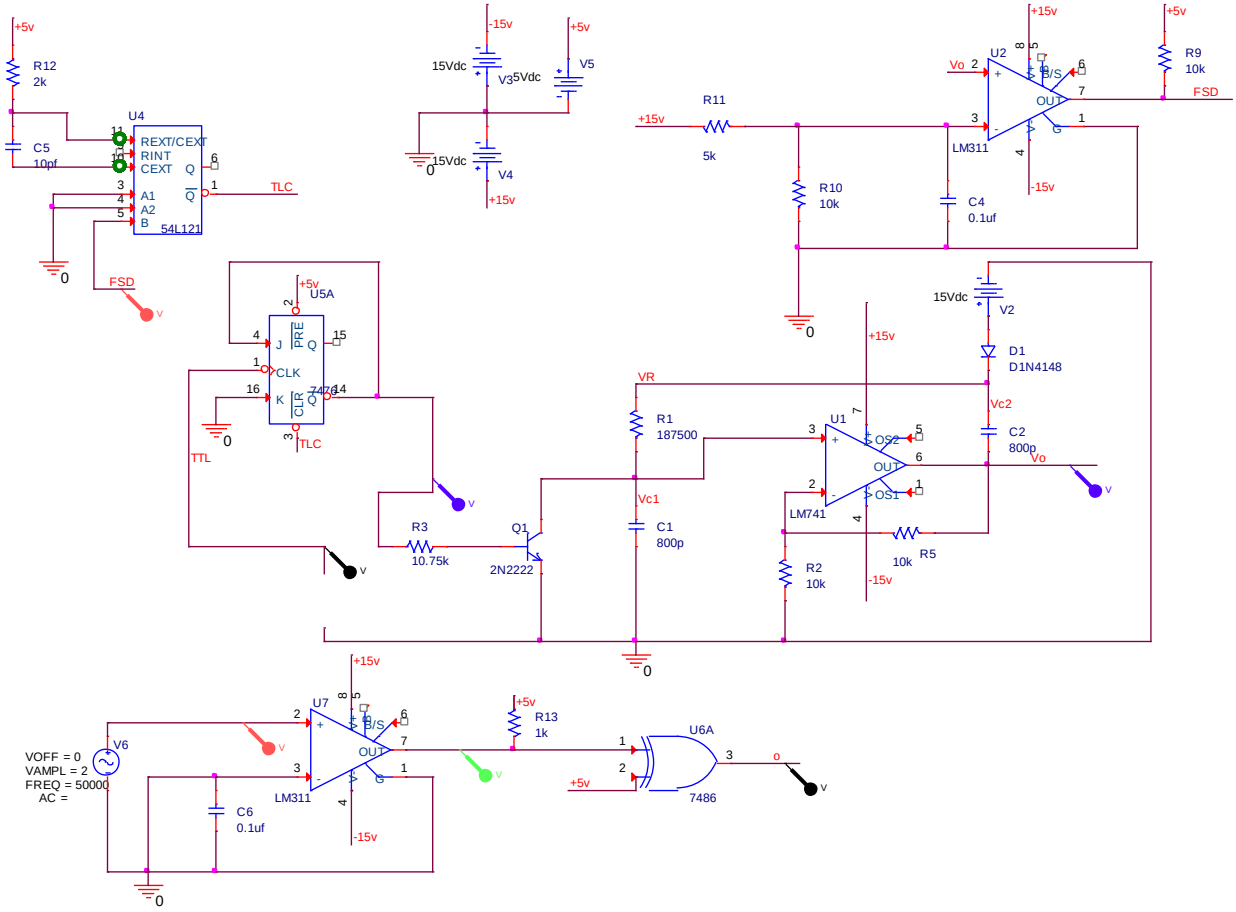


Figure 14 - the full-time base circuit

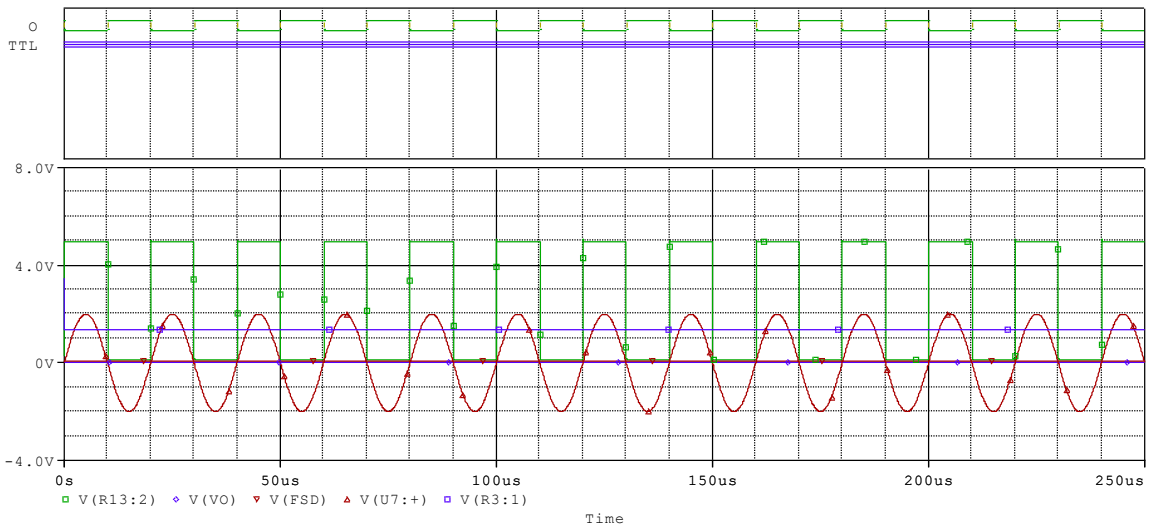


Figure 15 - Result for the time base circuit