Programme: DT008 / 2
ELEK2108 Electronics 1
Laboratory Technical Report

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Collaborator 3:	-	-

Laboratory Number:	**E**
Semester Week Number:	**10**
Date:	**25/03/2019**

Submission Checklist and Declaration

To ensure that the focus of the assessment of your laboratory report can include the development of higher order skills and competences associated with a Level 7 qualification, please complete the checklist and declaration below.

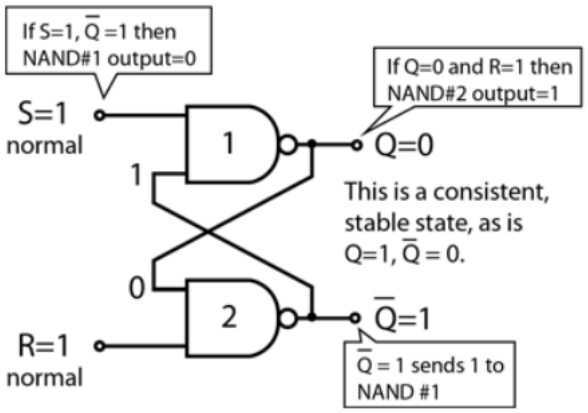
I declare that the report that I am submitting:	**Confirm**
• is my original work, with secondary sources acknowledged;	☒
• was proofread thoroughly for typographical errors;	☒
• contains citations with references formatted in the IEEE citation style.	☒
I understand that my work can be returned uncorrected if the criteria are unfulfilled.	

Signature:

1.0 Laboratory Aim

- Describe the purpose of the laboratory or the research.

The Purpose of this lab was to create a memory NAND cell. This diagram that is shown below shows the states of the NAND cells and how they operate.



Truth Table

Set	Reset	Output
1	1	No change*
0	1	Q=1
1	0	Q=0
0	0	Invalid state

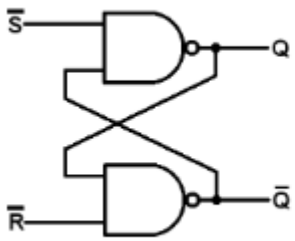
* can be used for data storage

2.0 Laboratory Procedure

- Describe the actions taken during the work.

The NAND cell circuit contains 2 NAND gates connected together a pair of cross-coupled 2-inputs to simply make basic single bit set-rest SR flip-flop.

The Memory circuit functions by storing the voltage present on an input signal whenever they are triggered by a control signal and they keep store voltage until the next true state of the control (or trigger) signal.



Time		Time + 1
$\bar{S}$	$\bar{R}$	Q
0	0	1
0	1	1
1	0	0
1	1	NO CHANGE

If two inputs S and R of the NAND cell are active low (0) at the same time output Q goes high (1). If both inputs S and R of the NAND cell are high same time then the feedback loop can become unstable and the memory device can get temporary stuck in a stable region.

3.0 Results

- Present the results recorded from the investigation.

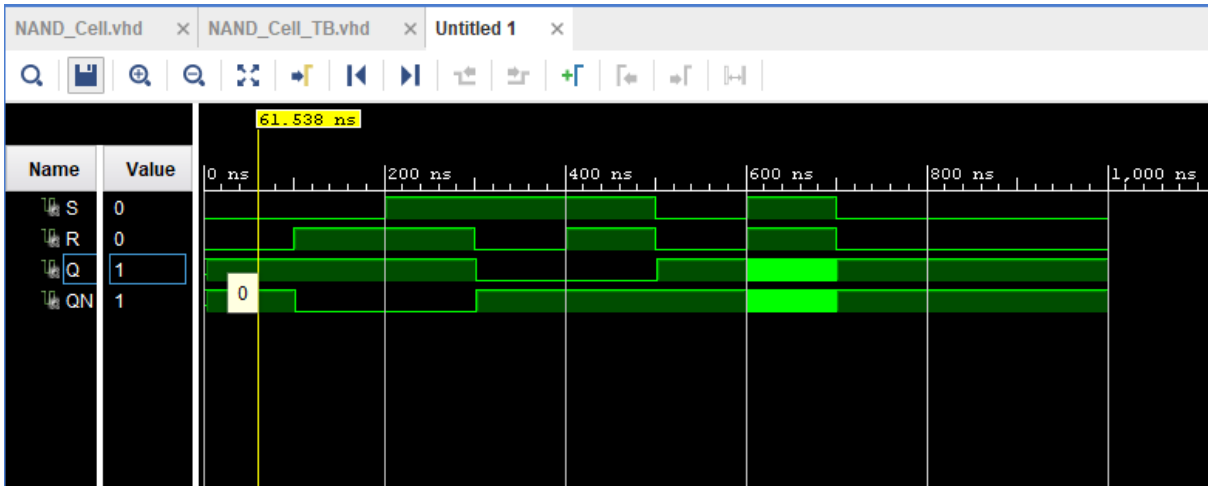


Figure 1 - Test simulator

NAND			
S	**R**	**Q**	**QN**
0	0	1	1
0	1	1	0
1	1	1	0
1	0	0	1

Operation	Waveform Timing (ns)
A set operation	200 ns
A reset operation	100 ns
A '0' being stored in memory	
A state where the Q and QN outputs are both driven to the same value	300 ns
A metastable state	700ns

Operation	Waveform Timing (ns)
A set operation	300 ns
A reset operation	500 ns
A '0' being stored in memory	300 ns
A state where the Q and QN outputs are both driven to the same value	500 ns
A metastable state	700 ns

4.0 Analysis

- Provide some comments that interpret what the results indicate or prove.

  When S and R change their state, it changes the state of Q.

5.0 Conclusions

The result met the conditions, and the simulation reflected the design.

6.0 References

NAND cell diagram:

http://hyperphysics.phy-astr.gsu.edu/hbase/Electronic/ietron/nandlatch.png

NAND cells Research:

https://www.electronics-tutorials.ws/sequential/seq_1.html

Submission Checklist

1. The cover page is appropriately complete. ☒
2. The six sections in the body of the report are complete. ☒
3. The constructive feedback from a collaborator is addressed. ☒
4. A final spell-check is completed. ☒
5. A backup copy of the report is online. ☒