Programme: DT008 / 2
ELEK2108 Electronics 1
Laboratory Technical Report

	Name	Student Number
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Collaborator 1:	-	-
Collaborator 2:	-	-
Collaborator 3:	-	-

Laboratory Number:	**D**
Semester Week Number:	**9**
Date:	**11/03/2019**

Submission Checklist and Declaration

To ensure that the focus of the assessment of your laboratory report can include the development of higher order skills and competences associated with a Level 7 qualification, please complete the checklist and declaration below.

I declare that the report that I am submitting:	**Confirm**
• is my original work, with secondary sources acknowledged;	☒
• was proofread thoroughly for typographical errors;	☒
• contains citations with references formatted in the IEEE citation style.	☒
I understand that my work can be returned uncorrected if the criteria are unfulfilled.	

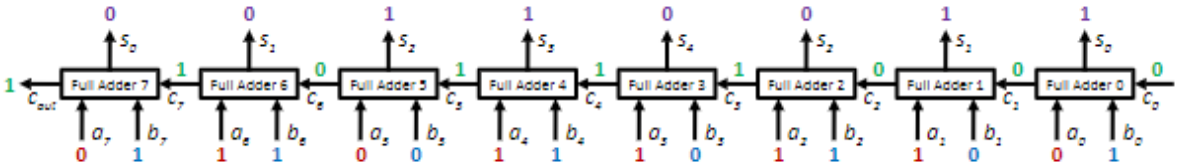
Signature:

1.0 Laboratory Aim

- Describe the purpose of the laboratory or the research.

The aim of this lab was to build a Cascaded 8 bit adder in Vivado.

- Importing:
  - VHDL behavioural design source code
  - VHDL library source code
  - A VHDL simulation (Test bench) code to test the design
- Implement the design on the Artix-7 FPGA via the Basys3 development board
- Apply signals tot eh board switches to confirm that the design works as planned



2.0 Laboratory Procedure

- Describe the actions taken during the work.

  The new project was created in the Vivado and was given a ame and location. The Register Transfer level (RTL) was selected to be able to add sourse, run RTL analysis, sythesis and design planning and analysis.

  The sourse files was added from the bright space 'ByteAdd.vhd' this file will be added/copied to the Byte_Adder.xpr project thatv just been created.

  The Board was selected and libray was added using "Add a design sourse" and the XSE.vhd was selected. The "testBench" simulation sourse file was added along with the ByteADD_tb.vhd testbench.

  The limit for the simulation runtime was set to 50ns and the behavioural simulation was run.

3.0 Results

- Present the results recorded from the investigation.

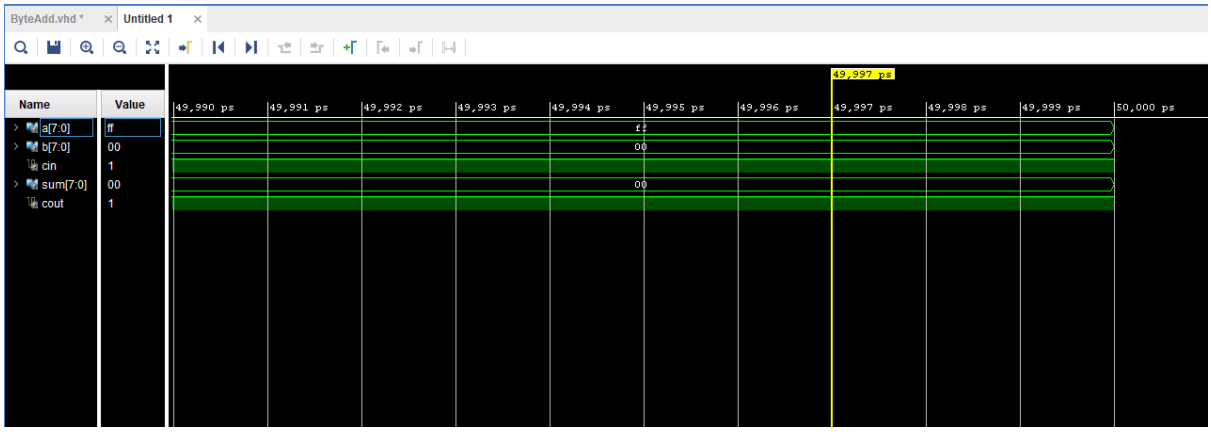


Figure 1 – Simulation Result

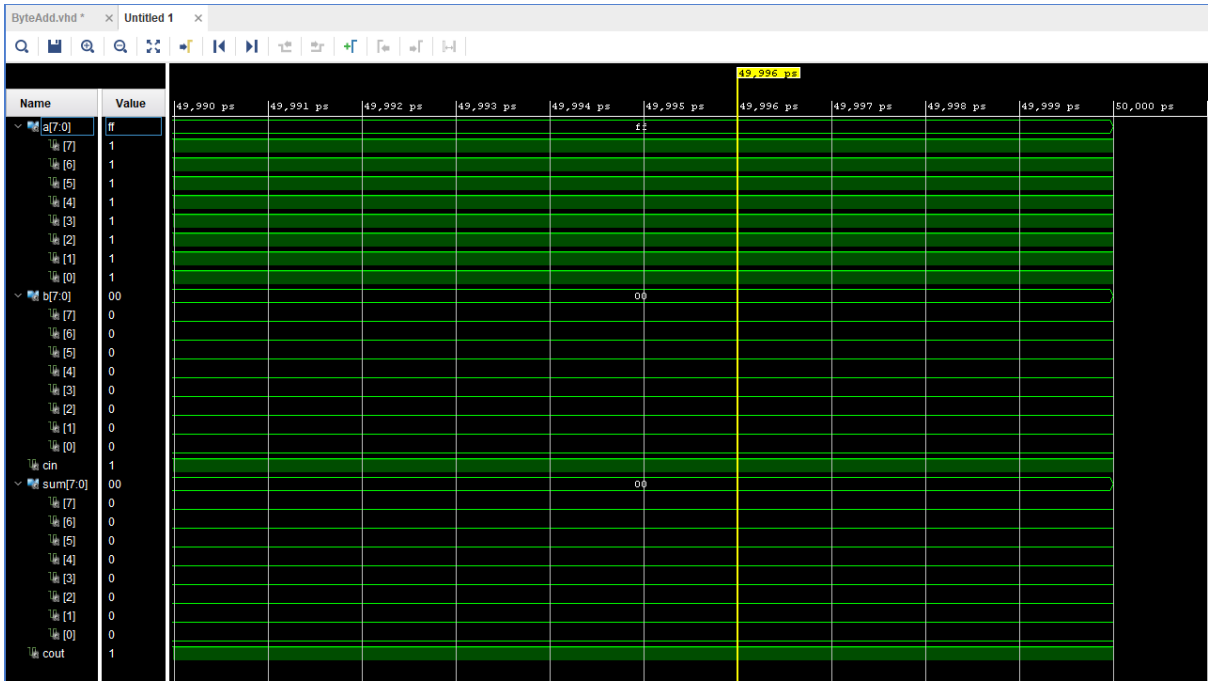


Figure 2 - Simulation Result

A	B	Cin	EXPECTED SUN (A+B)	EXPECTED Cout	Correct? t/f
00000000	00000000	0	00000000	0	t
00000100	00001100	0	00010000	0	t
11111111	00000000	1	00000000	1	t
01011110	11010101	0	00110011	1	t

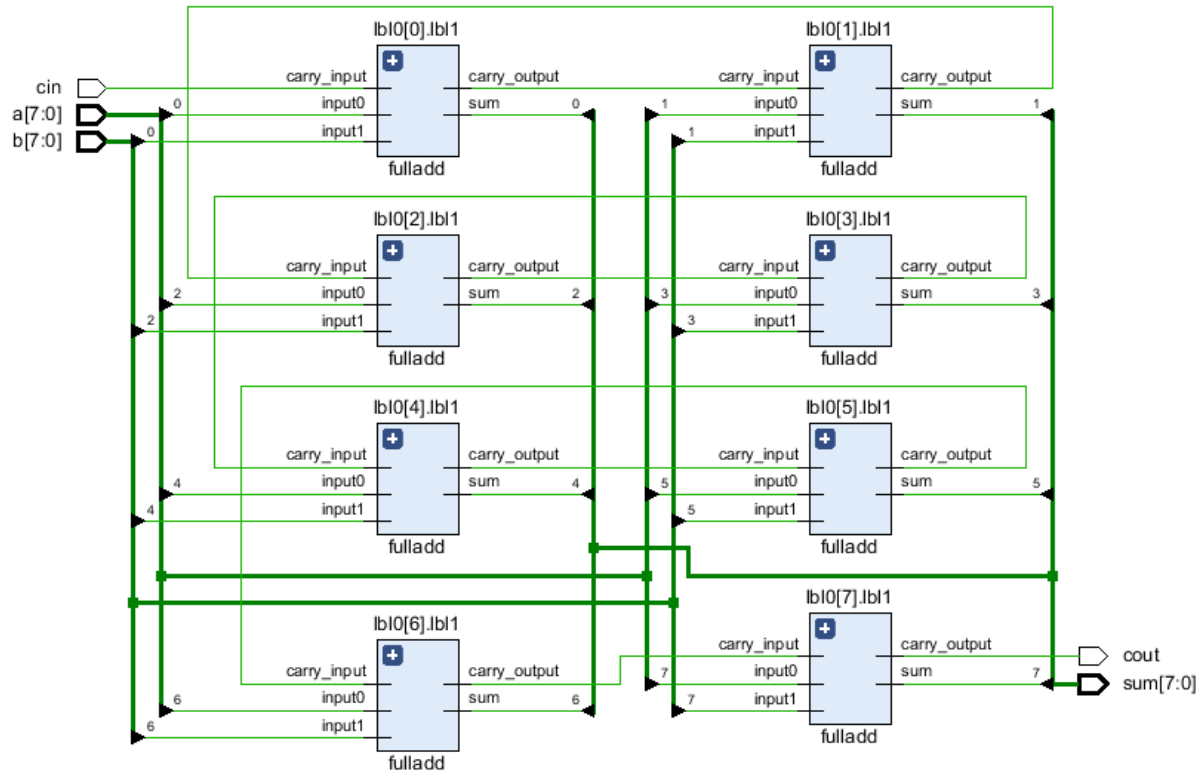


Figure 3 – Analysis Schematic diagram

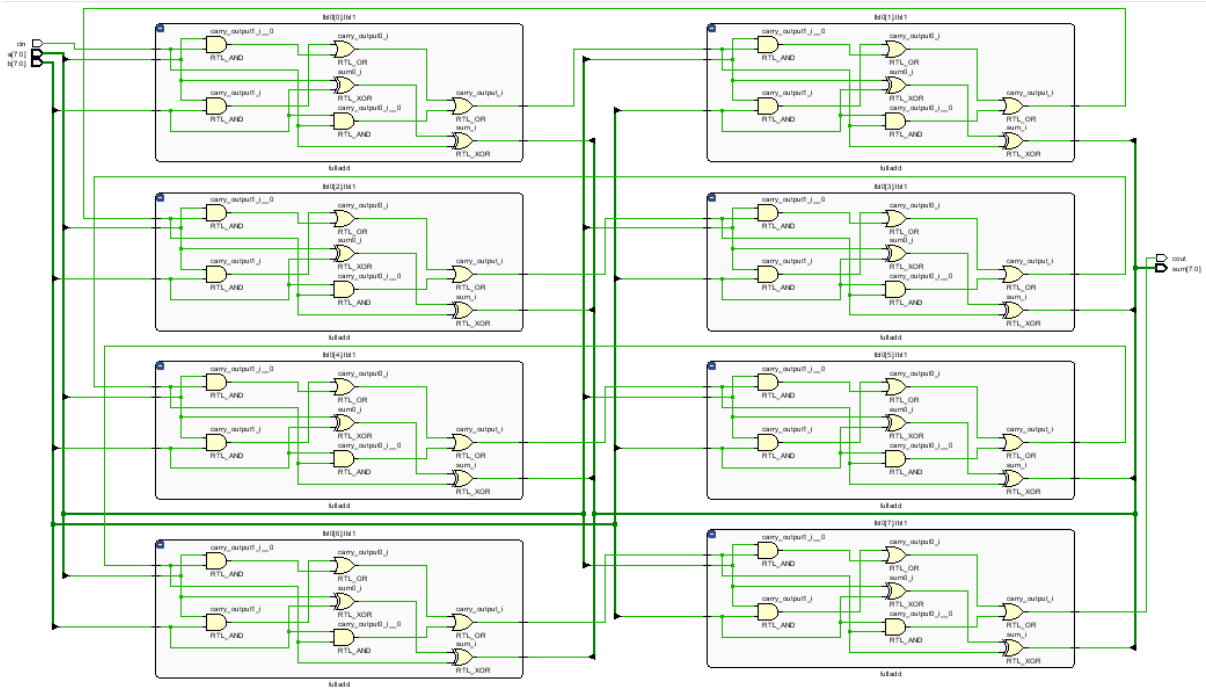


Figure 4 - Analysis Schematic diagram with logic gates

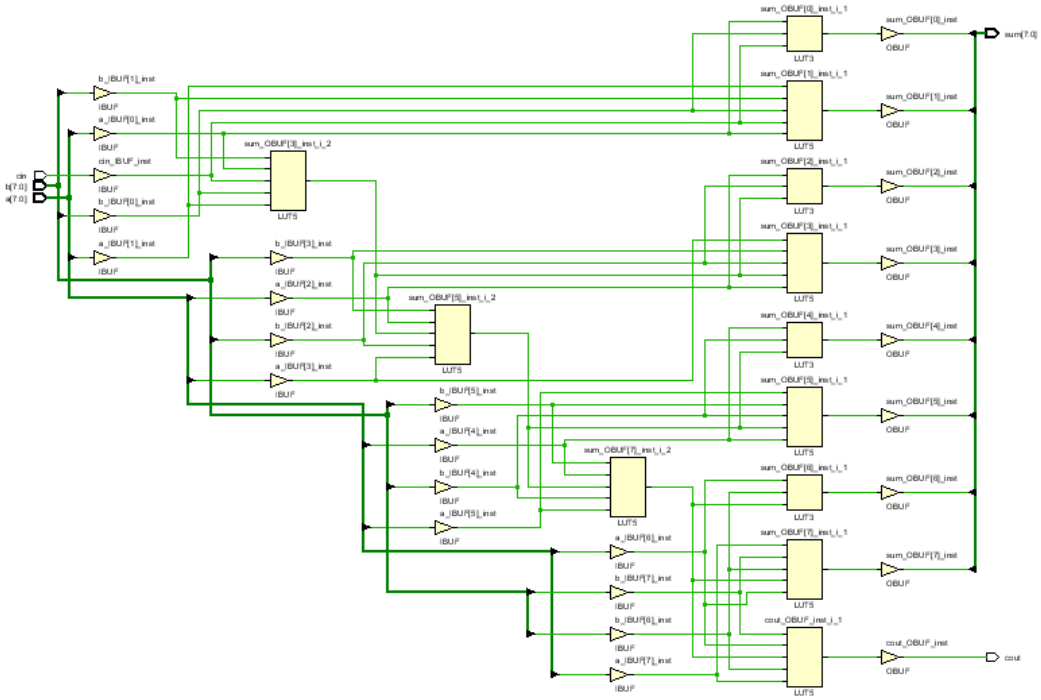


Figure 5 – Circuit diagram

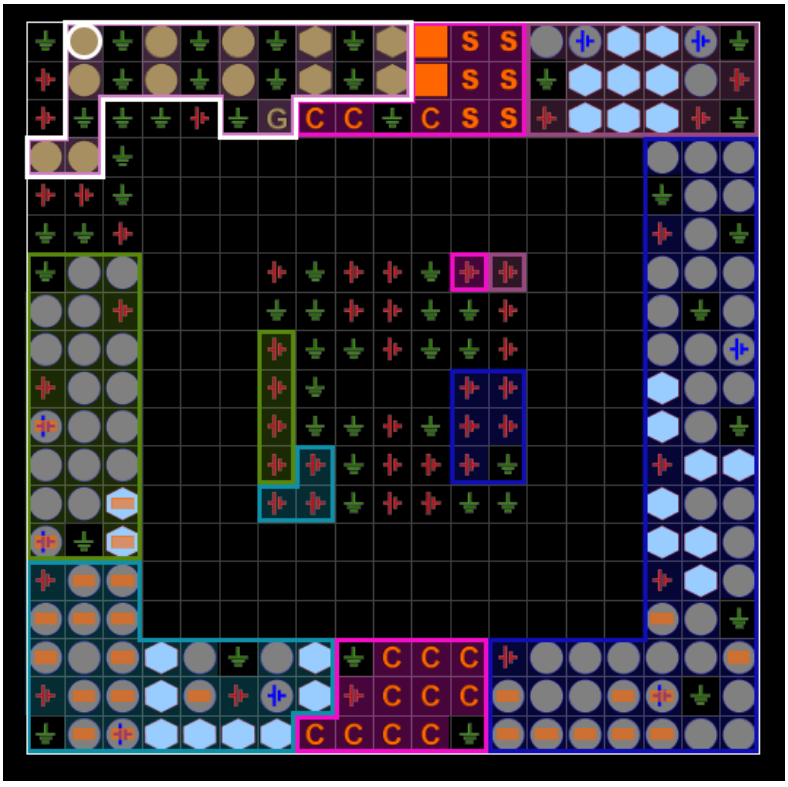


Figure 6 – Elebart design

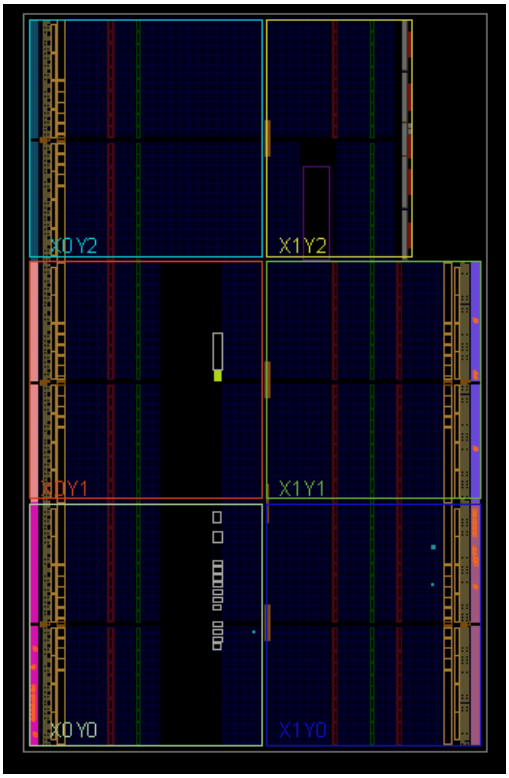
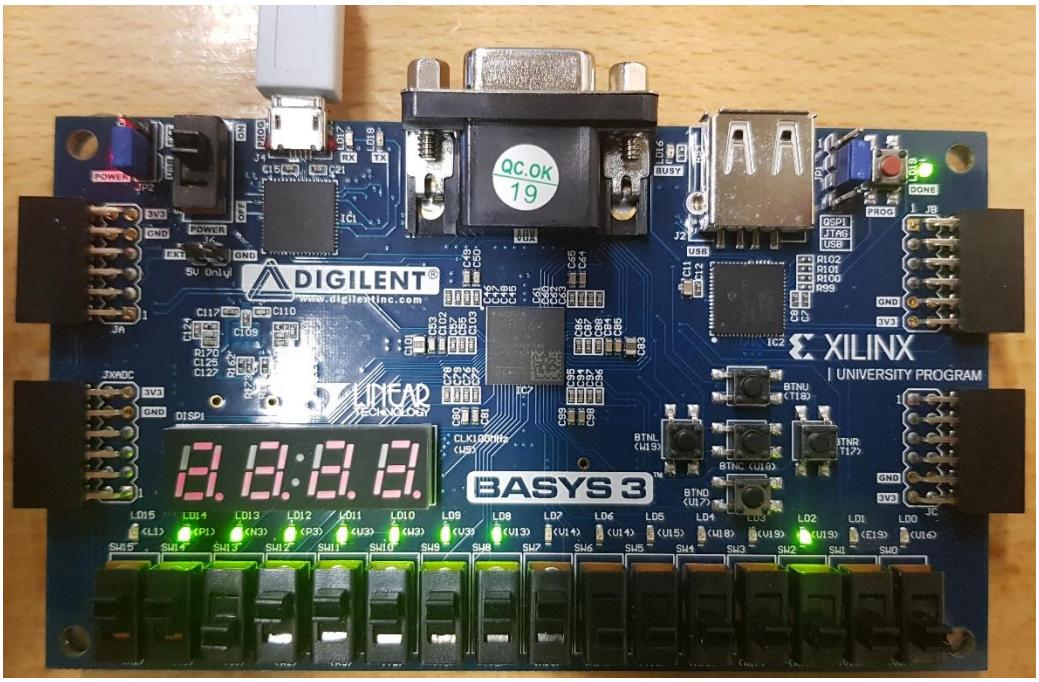
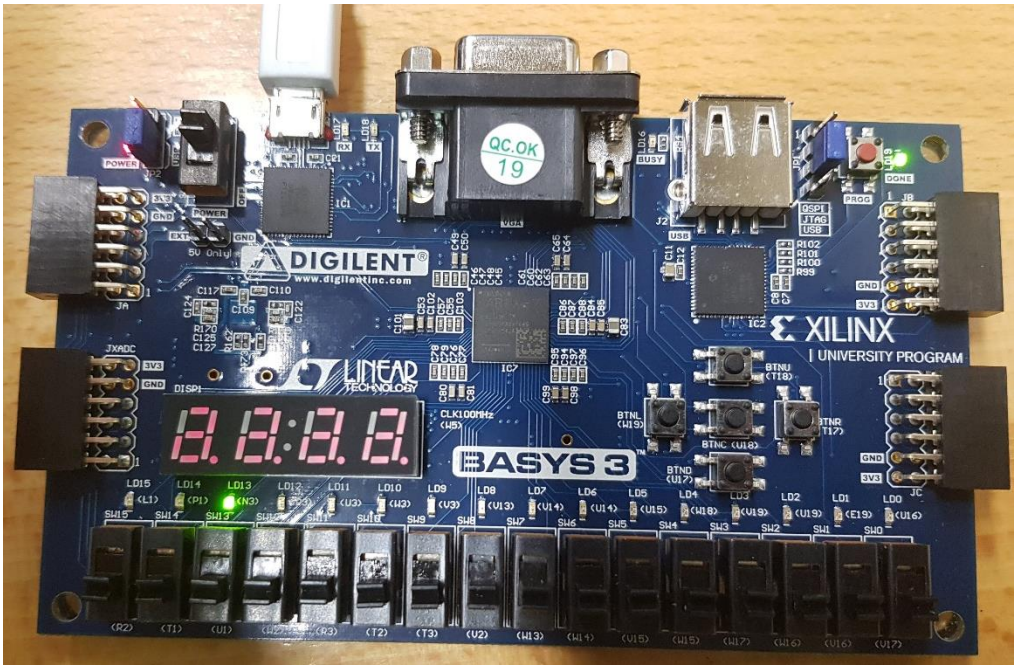


Figure 7 – Device

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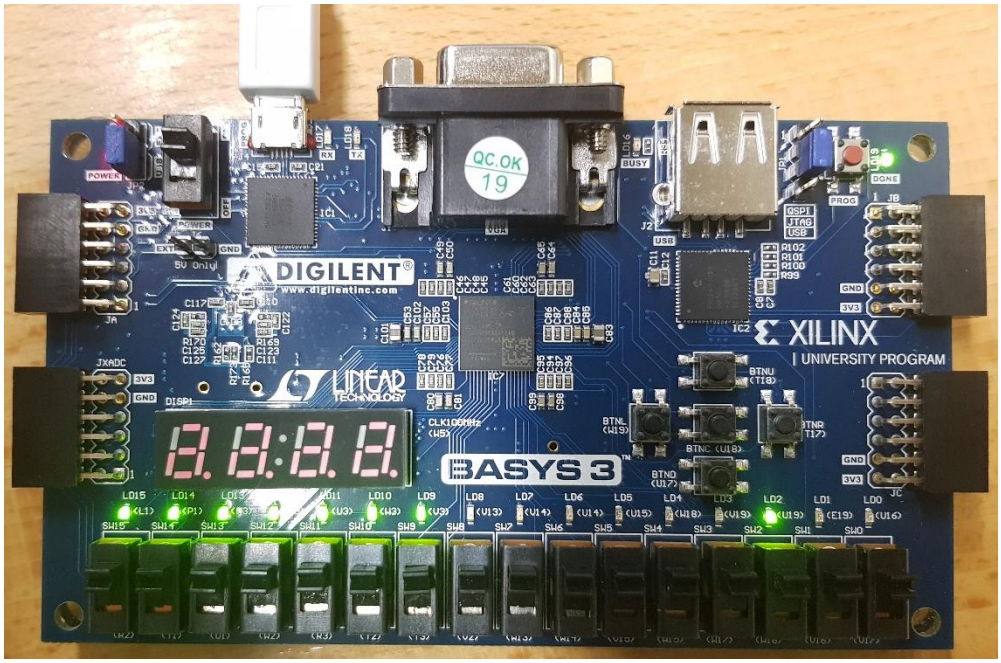
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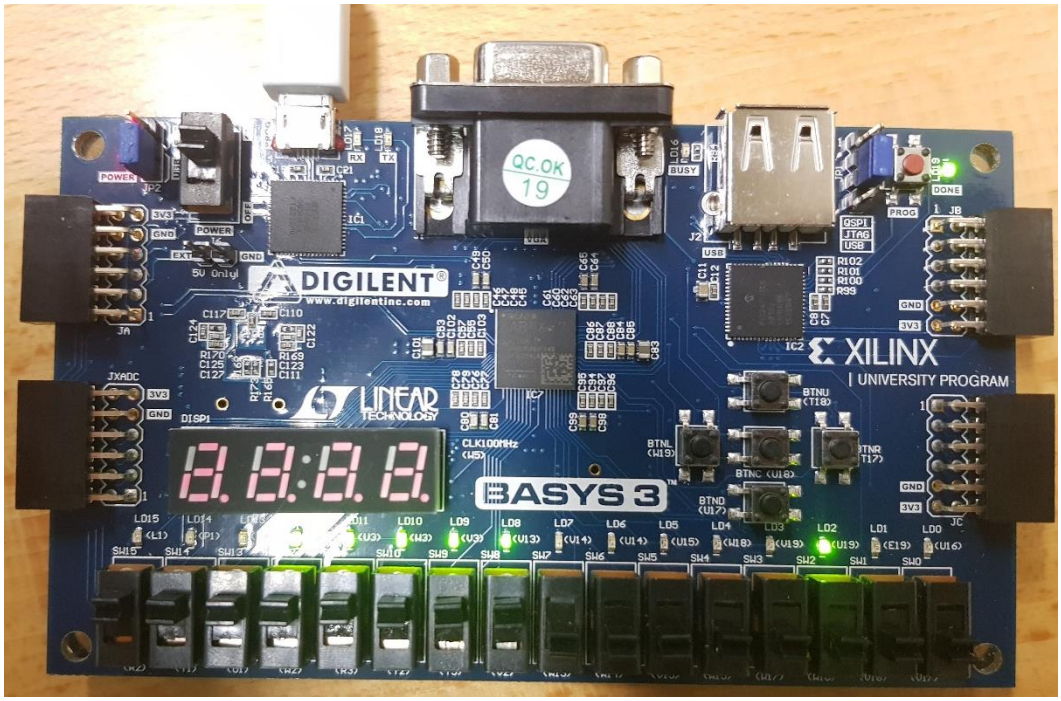

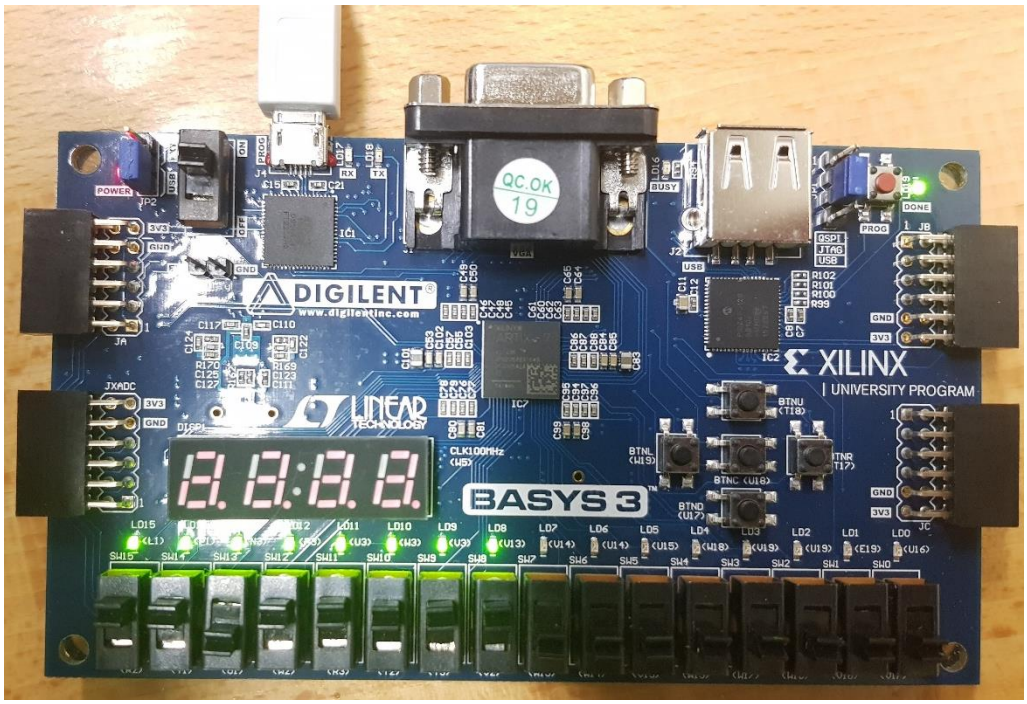

4.0 Analysis

- Provide some comments that interpret what the results indicate or prove.

  We saw two binary signals been inputted and we saw an output through the 8 bit adder.

5.0 Conclusions

The things I have learned about the 8 bit adder that a full adder is made by combining two half-adders and an additional OR-gate. A full adder has the carry in capability and so allows cascading which results in the possibility of multi-bit addition. The circuit diagram for a full adder is given below, note that the two separate half-adders are each enclosed in a box to help understand this circuit.

6.0 References

https://www.bing.com/images/search?view=detailV2&id=DE9F4FCD0B4FCEDC86C4FB25437AE82D6AAA34B5&thid=OIP.QmOoeHDXM80oGDBSGS0SHQHaEn&mediaurl=https%3A%2F%2Fi.pinimg.com%2F736x%2F4f%2F32%2F16%2F4f32169be852d0416cf4ff76068e6a06.jpg&exph=459&expw=736&q=8-Bit+Adder+Logic+Gates&selectedindex=3&ajaxhist=0&vt=0&eim=1,6

Submission Checklist

1. The cover page is appropriately complete. ☒
2. The six sections in the body of the report are complete. ☒
3. The constructive feedback from a collaborator is addressed. ☒
4. A final spell-check is completed. ☒
5. A backup copy of the report is online. ☒