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DUBLIN
TECHNOLOGICAL UNIVERSITY DUBLIN

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

Programme: DT008 / 2
ELEK2108 Electronics 1
Laboratory Technical Report

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Collaborator 2:		
Collaborator 3:		

Laboratory Number:	**F**
Semester Week Number:	**12**
Date:	**11/04/2019**

Submission Checklist and Declaration

To ensure that the focus of the assessment of your laboratory report can include the development of higher order skills and competences associated with a Level 7 qualification, please complete the checklist and declaration below.

I declare that the report that I am submitting:	**Confirm**
• is my original work, with secondary sources acknowledged;	☒
• was proofread thoroughly for typographical errors;	☒
• contains citations with references formatted in the IEEE citation style.	☒
I understand that my work can be returned uncorrected if the criteria are unfulfilled.	

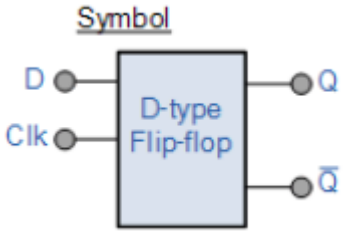
Signature:

(Insert an image of your signature)

1.0 Laboratory Aim

- Describe the purpose of the laboratory or the research.

The purpose of the laboratory is to make a memory data type flip flop in Vivado.



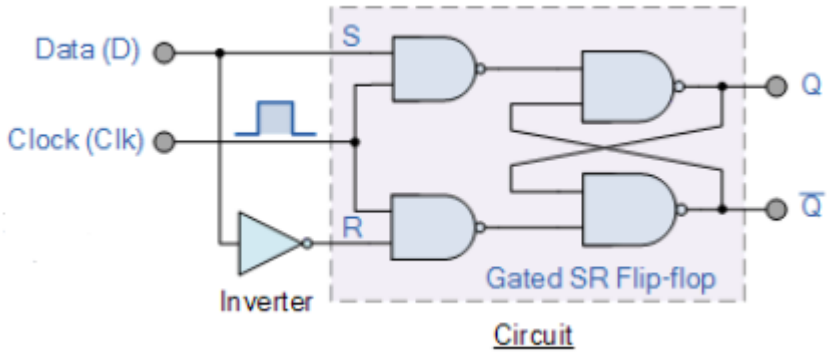
This is a symbol for memory D type flip flop.

The D-type flip-flop is a modified Set-Reset flip-flop with the addition of an inverter to prevent the S and R inputs from being at the same logic level.

One of the disadvantages of the

The D type flip flop is the most important of the clocked flip flops as it ensures that the inputs S and R are never equal to one at the same time.

The D type flip flop are built from a gated SR flip flop with an inverter added between the S and the R inputs to allow for a single for a single data input as the circuit is shown down below.



Memory circuit functions by storing the voltage present on an input signal whenever they are triggered by a control signal whenever they are triggered by a control signal, and they retain that stored voltages until the next assertion of the control signal.

2.0 Laboratory Procedure

- Describe the actions taken during the work.

In order to make data type flip flop in Vivado, new project was created along with a name in Vivado. The Register-Transfer level (RTL) project was selected to able to add sourses, create block diagrams in IP integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

The new sourses file was added from the bright space called “DTypeFlipFlop.vhd” These files will be added to the FlipFlop.xpr project that has just been created. The Basys3 board types were selected to vender: digilentinc.com, Display Name: Basys3, Board Rev: C.0.

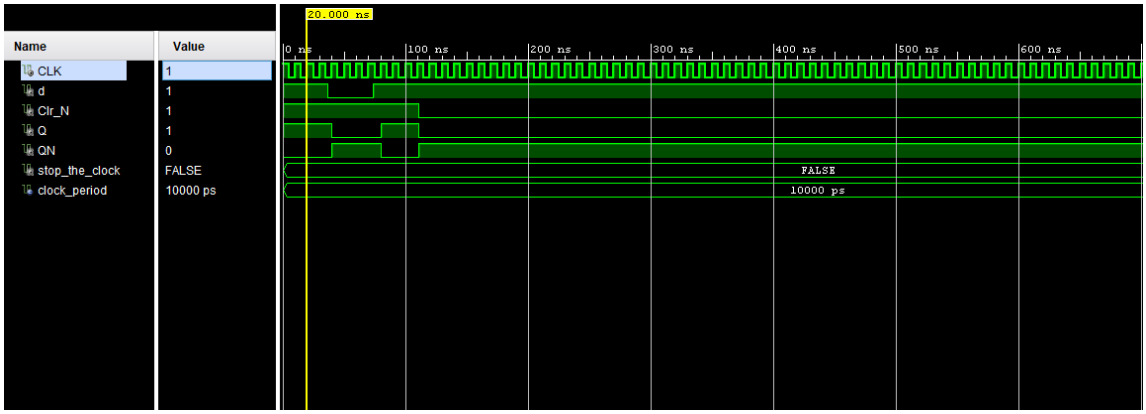
DtypeFlipFlop code that was provided contains the ports which are: clock, data input, active-low asynchronous clear input, data ouput and inverse of 0 for visual confirmation buffer. The next few steps clears the flip-flop if the asynchronous clear input in low otherwise store the value on the d input at the rising clock edge.

The simulation was run after he testbench file was similated and added “DTypeFlipFlop_TB.vhd”. The simulated result can be seen in he result section down below.

3.0 Results

- Present the results recorded from the investigation.

Simulated results.



The flip-flop triggers on the rising edge.

The CLR_N reset signal is active low.

The CLR_S set signal in synchronous with the clock.

The clock frequency in the simulation is 100million hertz because we are given period 10000ps so in order to find frequency we can use this formula

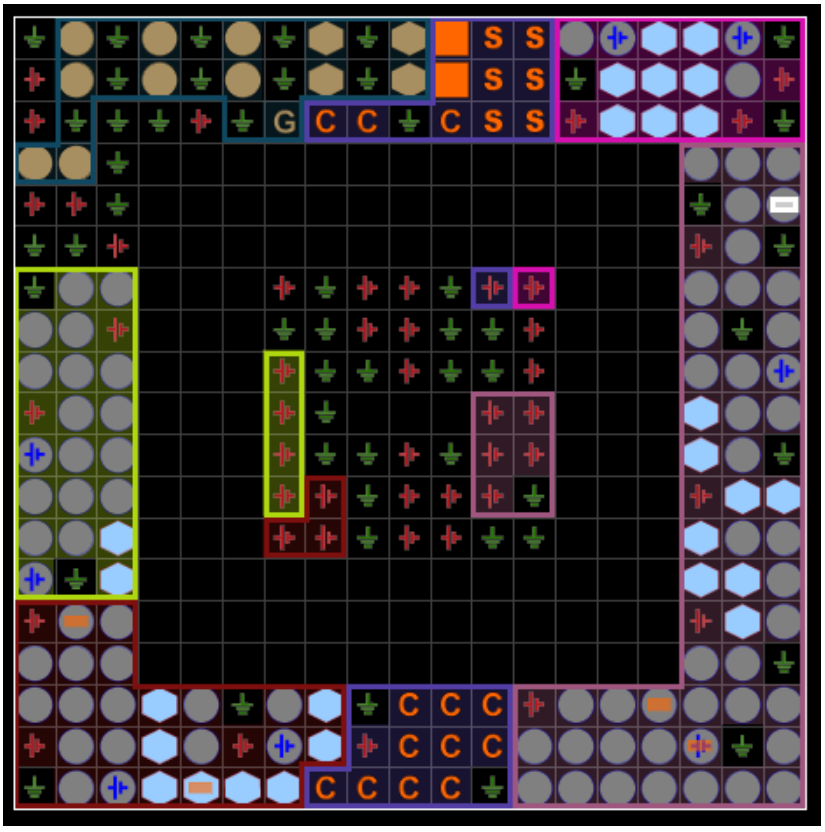
$$f = \frac{1}{p}$$

$$f = \frac{1}{10000 \times 10^{-12}}$$

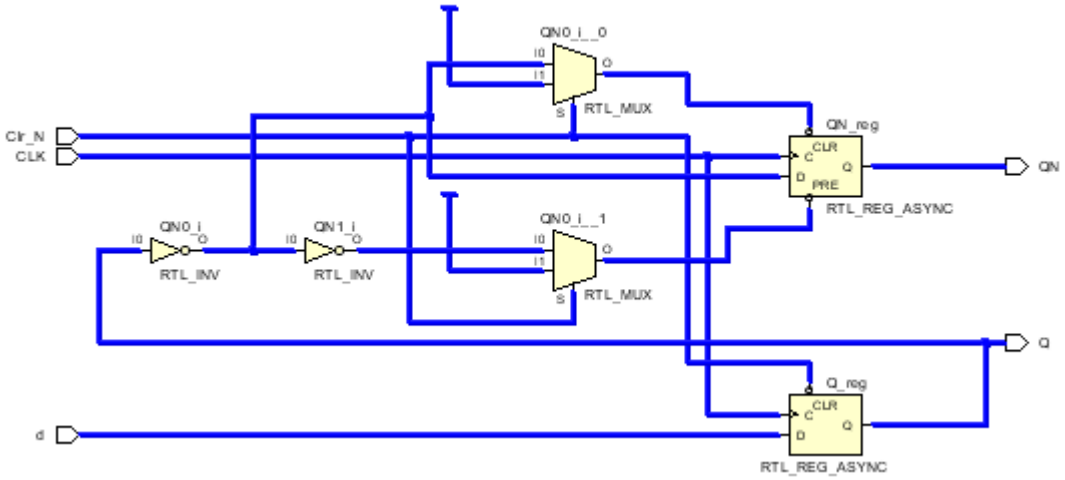
$$f = 100{,}000{,}000$$

Simulation aggress with the truth table and reflects the design code.

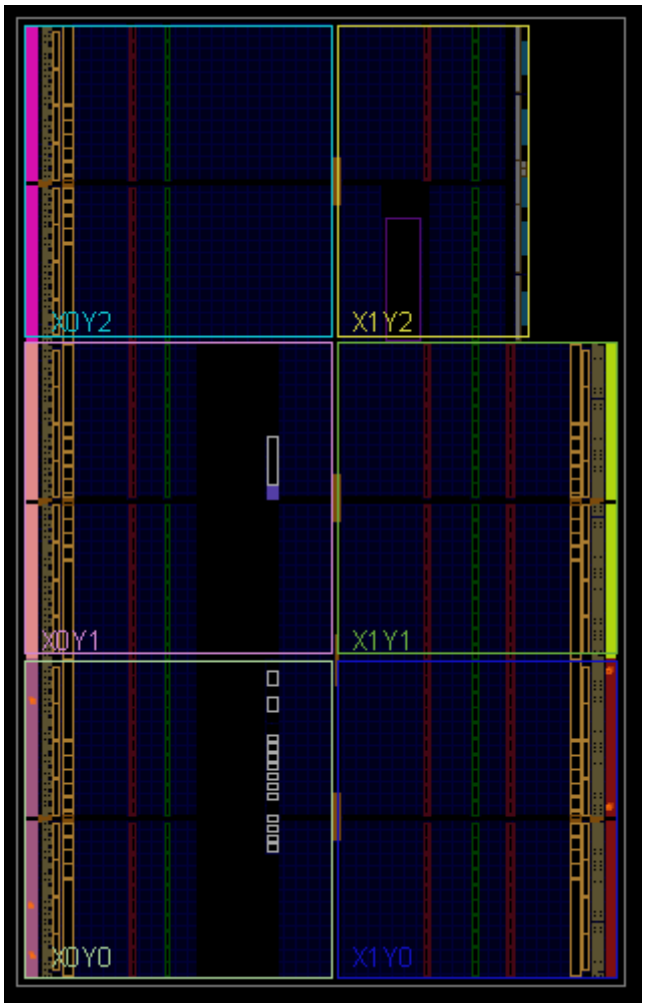
Time				Time + 1	
S	R	D	Clk	Q	⓪
0	0	0	0-1	0	1
0	0	1	0-1	1	0
1	0	0	0	1	0
0	1	1	0	0	1



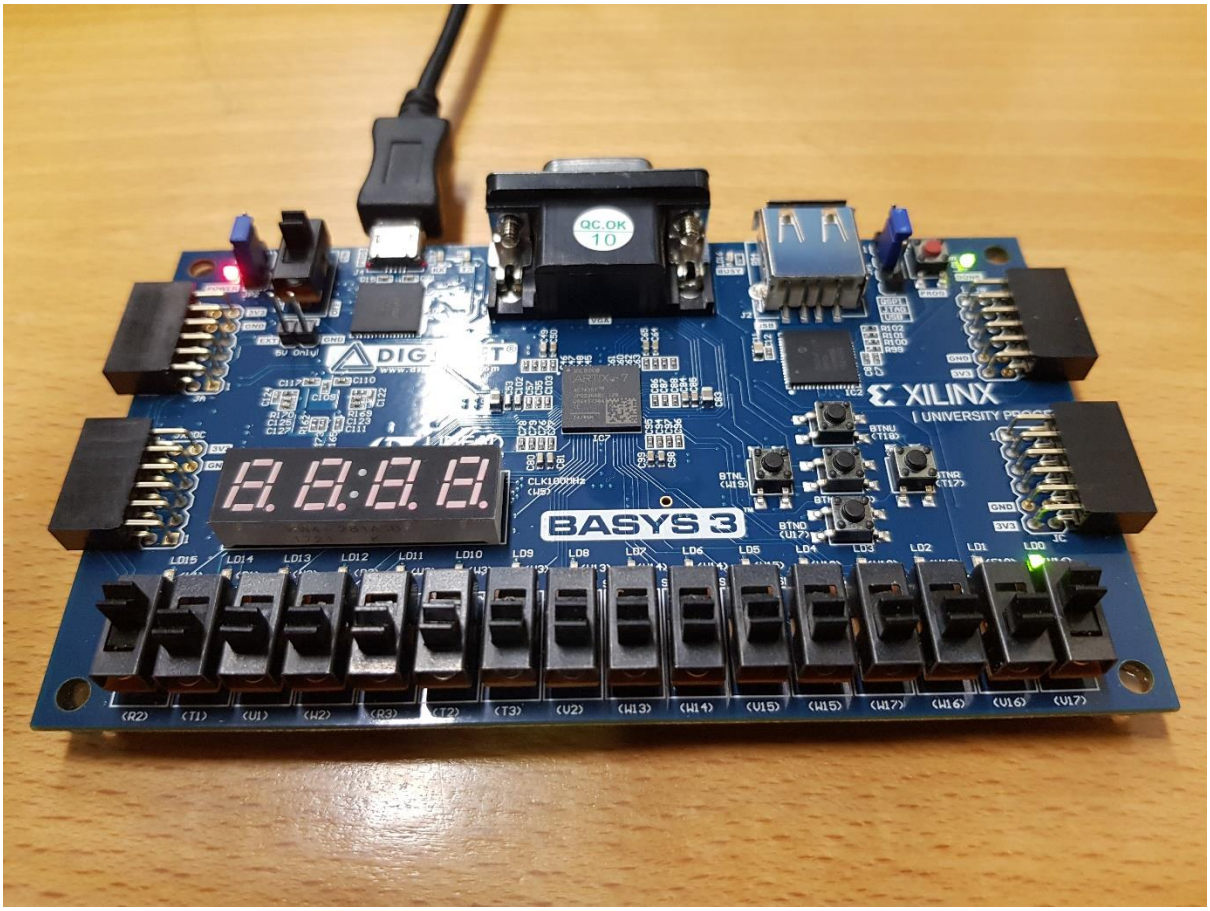
Input and output planning



Elaborated design schematic



Device


BASYS 3
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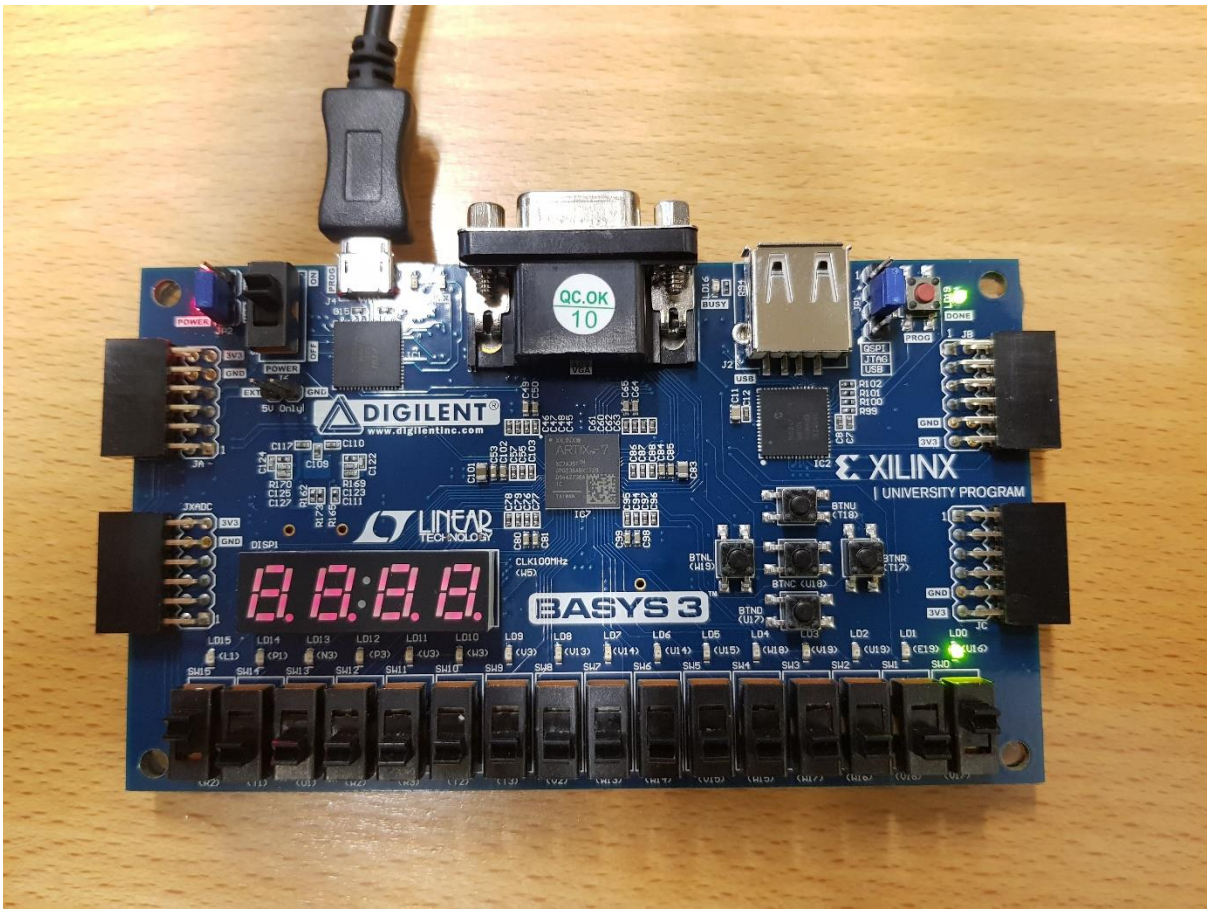
DIGILENT
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BASYS 3
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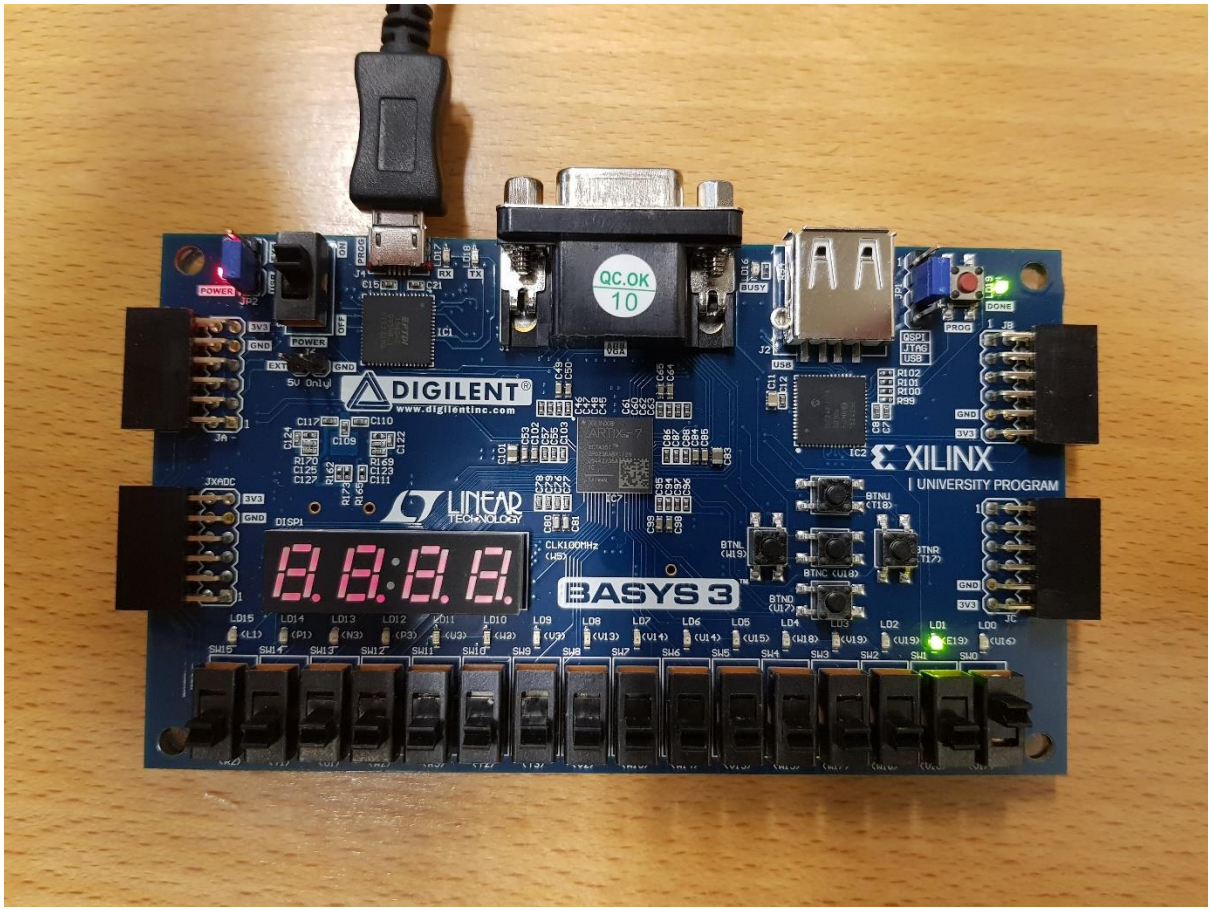
UNIVERSITY PROGRAM
LINEAR TECHNOLOGY


QC.OK
10
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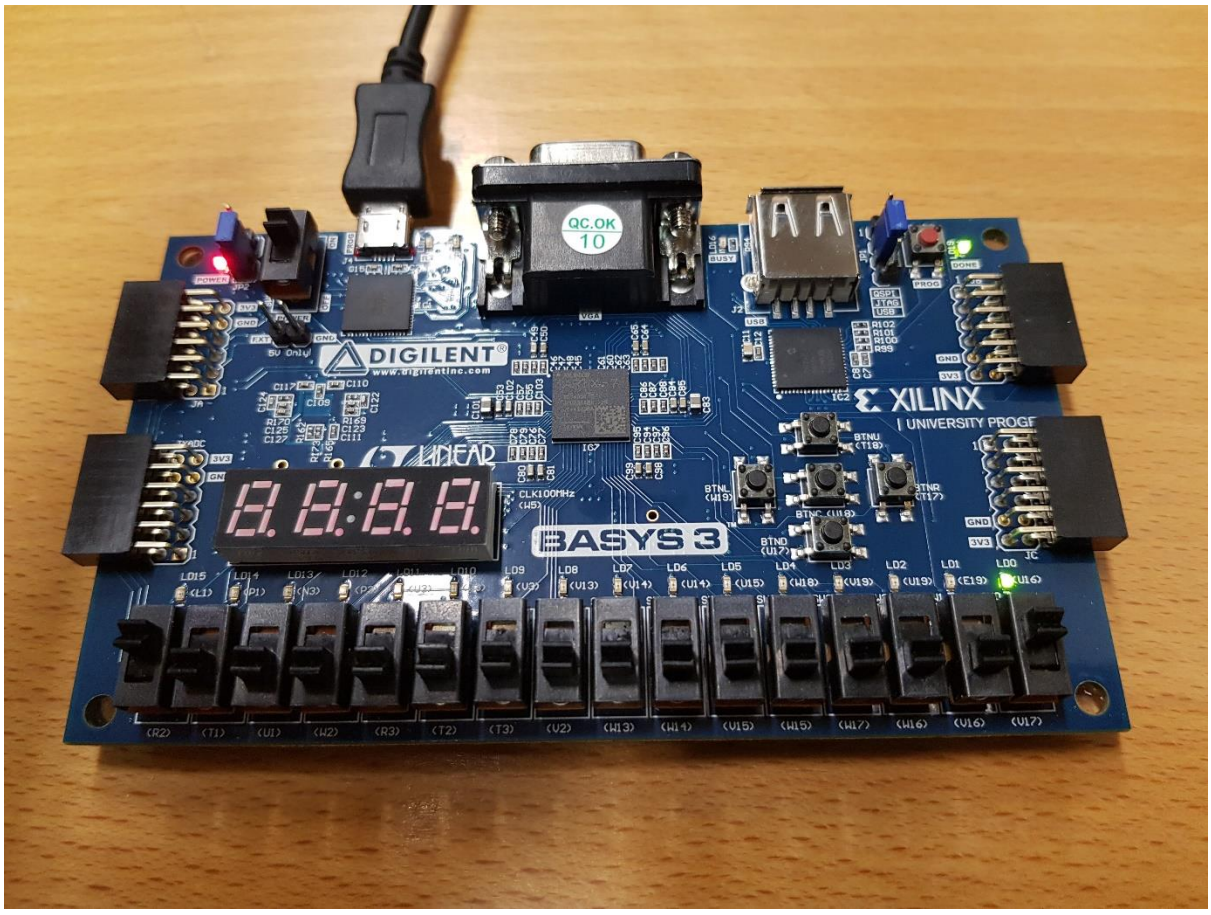
UNIVERSITY PROGRAM
LINEAR TECHNOLOGY
BASYS 3


QC.OK
10
DIGILENT
XILINX
BASYS 3

4.0 Analysis

- Provide some comments that interpret what the results indicate or prove.

5.0 Conclusions

- Develop the conclusion to convincingly state any understanding gained from the results or the research findings.

  The research that was taken while doing the lab work was very useful to learn the topic in the very less time. I can just refer this website in the reference section which helped while working on this lab.

- Typically, the conclusion will indicate a logical pattern that is evident in the results.
  If the results do not meet an expectation, discuss any factors that may have contributed to the unexpected results.

  The result meet all the expectation
  the conclusion is also an opportunity to clarify any knowledge or skill learned during the activity.

  The knowledge was gained while learning Data type Flip Flops.

6.0 References

- Use the IEEE citation style.

  Most of the research was carried from this website:
  https://www.electronics-tutorials.ws/sequential/seq_4.html

Submission Checklist

1. The cover page is appropriately complete. ☒
2. The six sections in the body of the report are complete. ☒
3. The constructive feedback from a collaborator is addressed. ☒
4. A final spell-check is completed. ☒
5. A backup copy of the report is online. ☒