

Computer Architecture Lab

Assignment 4

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Cycle Count for Programs of Assignment-1

Given ASM/OUT Files				
S.No	Name of Program	No of Cycles	Stall in OF Stage	Wrong Instruction taken during Branch
1	even-odd.asm	13	4	0
2	palindrome.asm	94	33	7
3	prime.asm	44	6	5
4	fibonnaci.asm	139	25	16
5	descending.asm	490	99	88

My ASM/OUT Files				
S.No	Name of Program	No of Cycles	Stall in OF Stage	Wrong Instruction taken during Branch
1	even-odd.asm	12	4	0
2	palindrome.asm	79	16	8
3	prime.asm	42	8	5
4	fibonnaci.asm	111	23	9
5	descending.asm	490	99	88

Observation

In this particular Lab assignment, we designed a pipe lined processor which can handle both **DATA** and **CONTROL** hazard. Number of cycle executed for a particular program in this processor is less than that of what we got in our Single Cycle Processor. In this pipelined processor the *Ratio of Number of Cycle Executed to Number of Instruction is less than 5*. For a particular program if number of cycle executed decreases then performance of the processor increases.