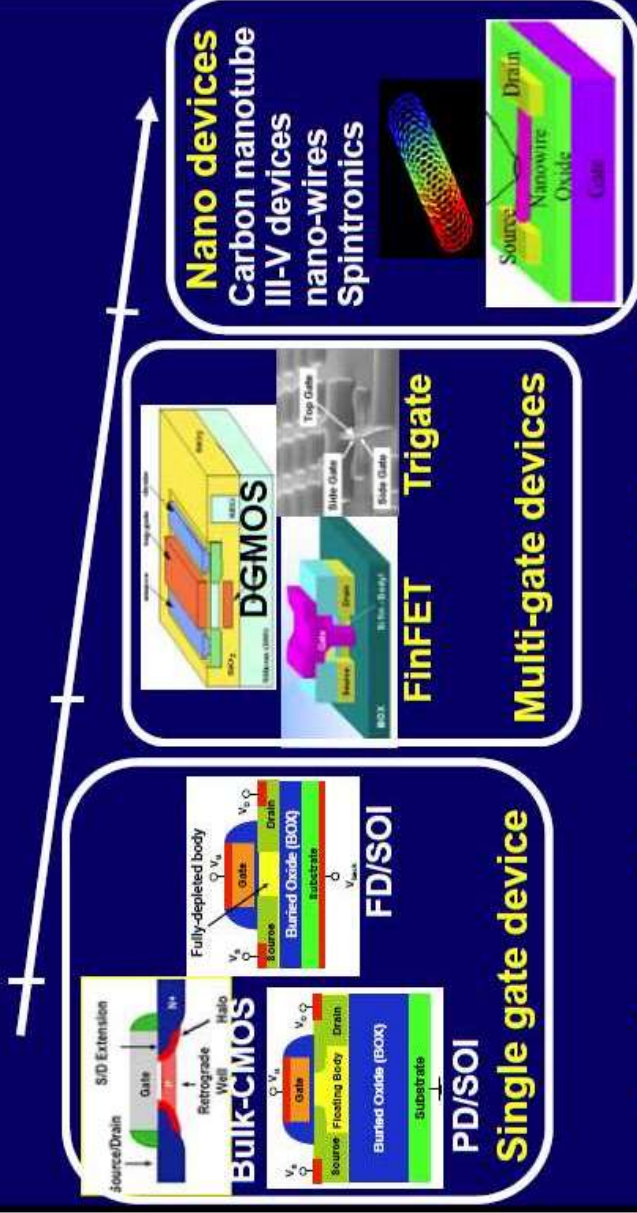


Technology Trend



Design methods to exploit the advantages of technology innovations

Chip	IBM P9™
Technology	14nm FinFET SOI
No. Cores	24
Area	695mm ²
No. of Transistors	8 Billion

VLSI System

- An electronic system composed of VLSI chips
- VLSI Chips
 - Very Large Scale Integration Chips
- Integration Complexity
 - Number of gates in a single chip

Why Integrated Circuits?

- Integration Improves the Design
 - Physically small
- Integration Reduces Manufacturing Costs
 - Automated (Little manual assembly)
 - Less Packaging Cost
 - Less Testing Cost

IC Evolution

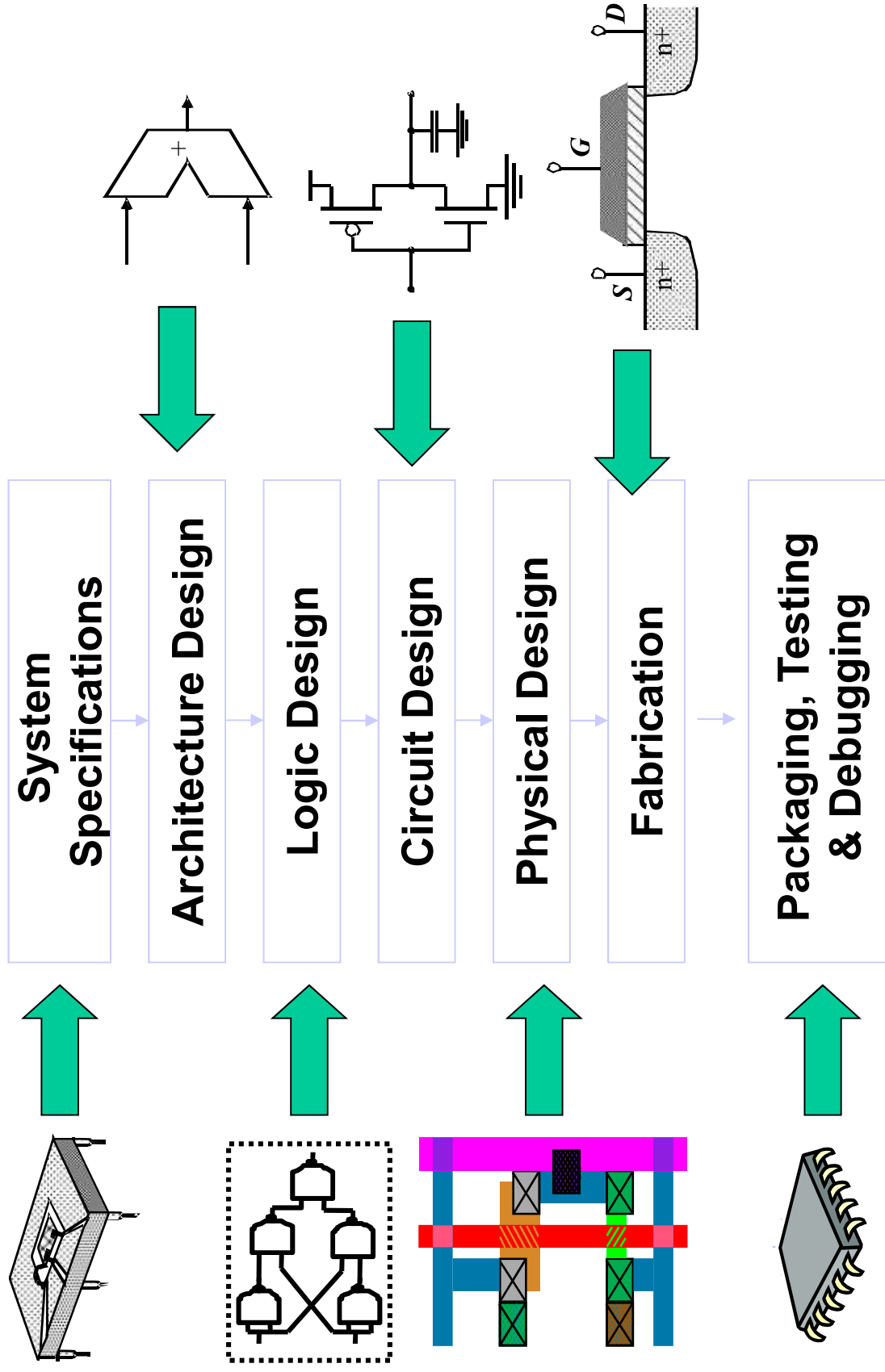
- SSI – Small Scale Integration
 - 10 gates per chip (1960's)
- MSI – Medium Scale Integration
 - 100 gates – 1000 gates per chip (1970's)
- LSI – Large Scale Integration
 - 1000 gates – 10,000 gates per chip (1980's)
- VLSI – Very Large Scale Integration
 - 10,000 gates – 1,00,000 gates per chip (1990's)
- ULSI – Ultra Large Scale Integration
 - 1M gates – 10M gates per chip (late 90's)
- GSI – Giant Scale Integration
 - 10M gates – 100M gates (early 2000's)

Technologies - Evolution

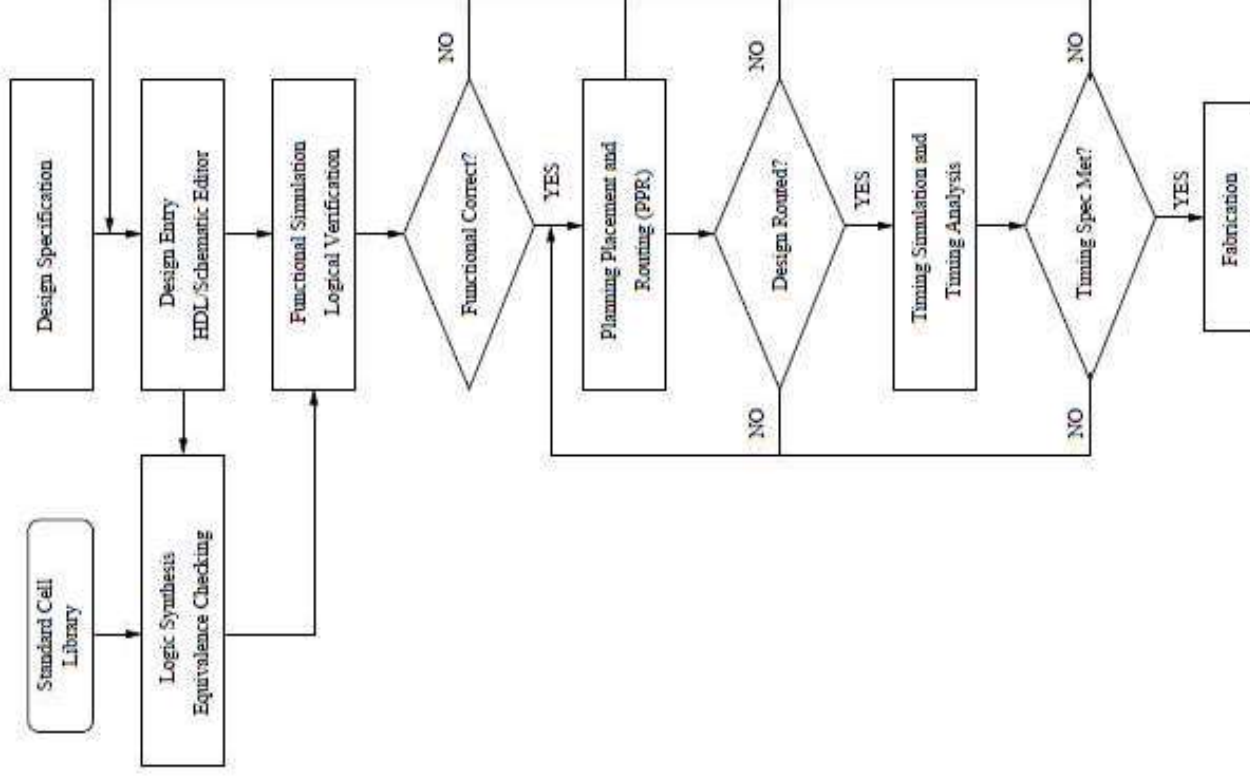
- Bipolar technology
- MOS (Metal-oxide-silicon)
 - Although invented before bipolar transistor, was initially difficult to manufacture
 - nMOS (n-channel MOS) technology developed in 1970s required fewer masking steps, was denser, and consumed less power than equivalent bipolar ICs .
 - CMOS (Complementary MOS): n-channel and p-channel MOS transistors with lower power consumption, simplified fabrication process
- BiCMOS - hybrid Bipolar, CMOS

VLSI Design Cycle

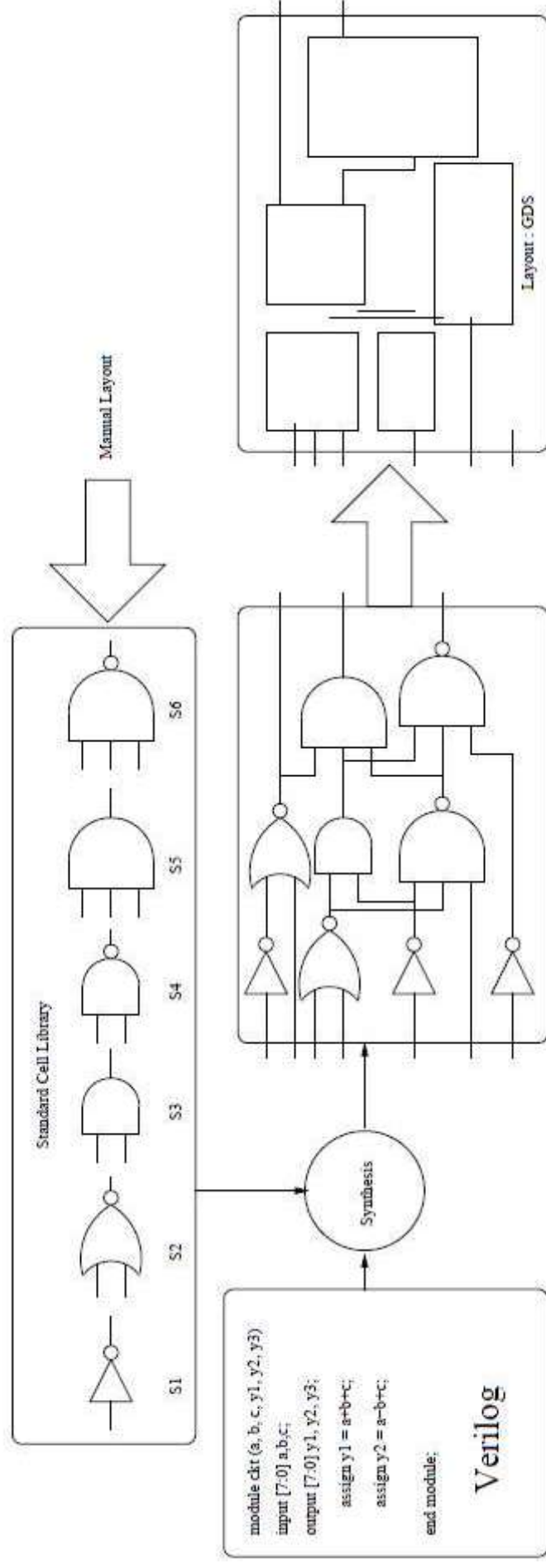
VLSI Design Cycle



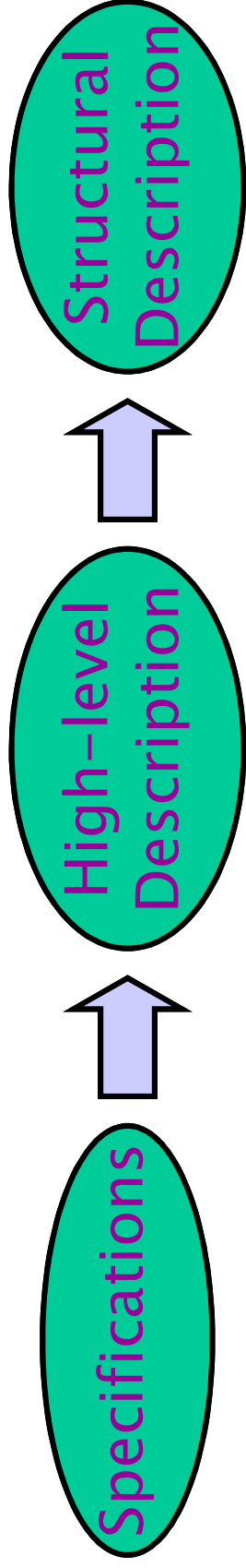
VLSI Design Cycle



VLSI Design Cycle

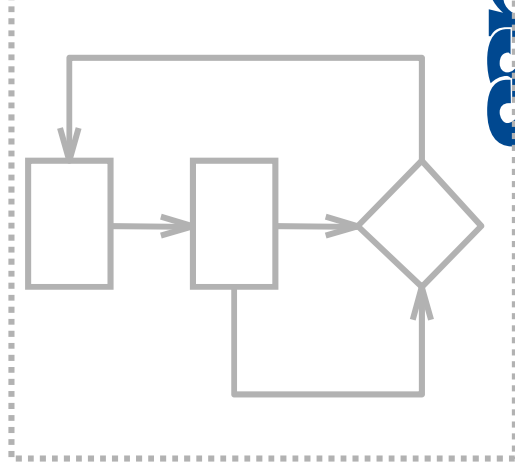


Digital IC Design

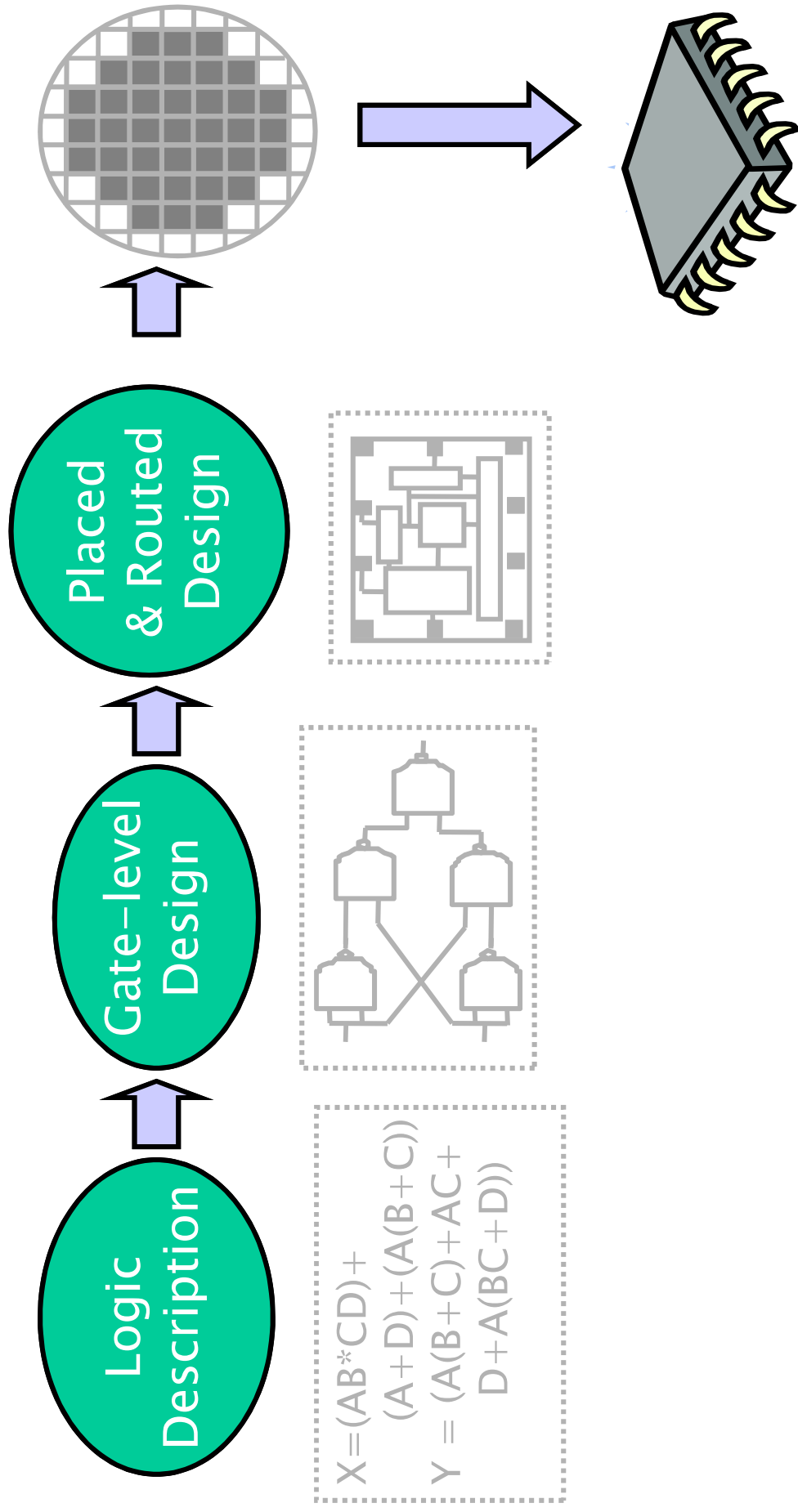


Behavioral
VHDL, C

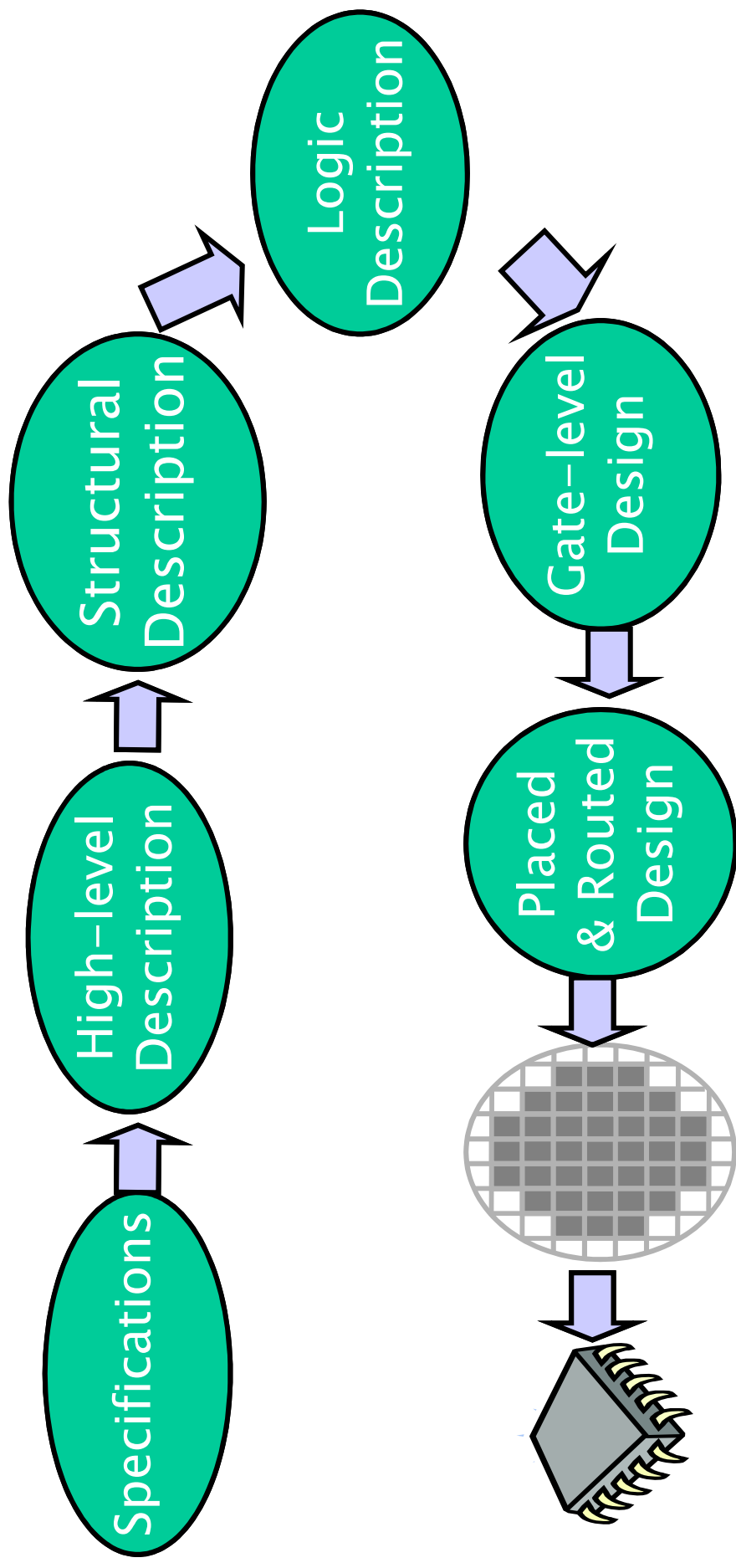
Structural
VHDL



Digital IC Design

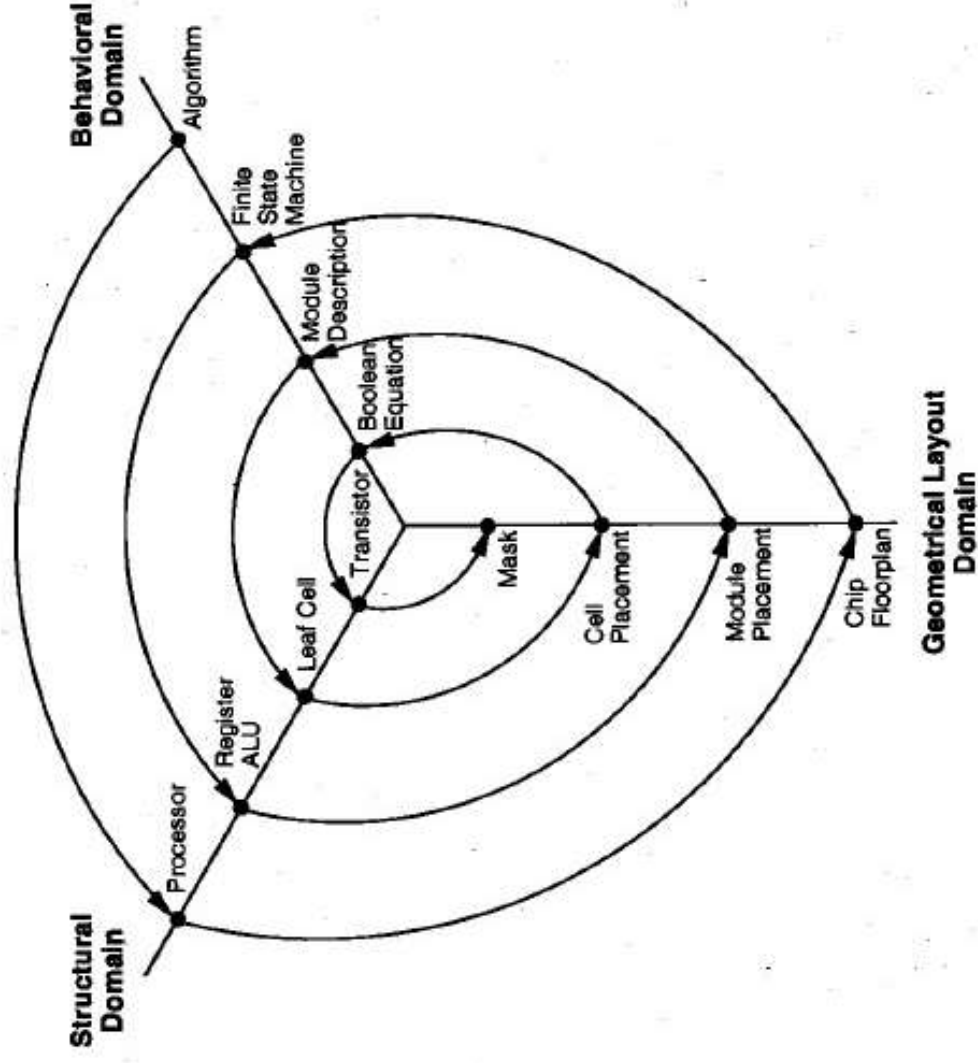


Digital IC Design



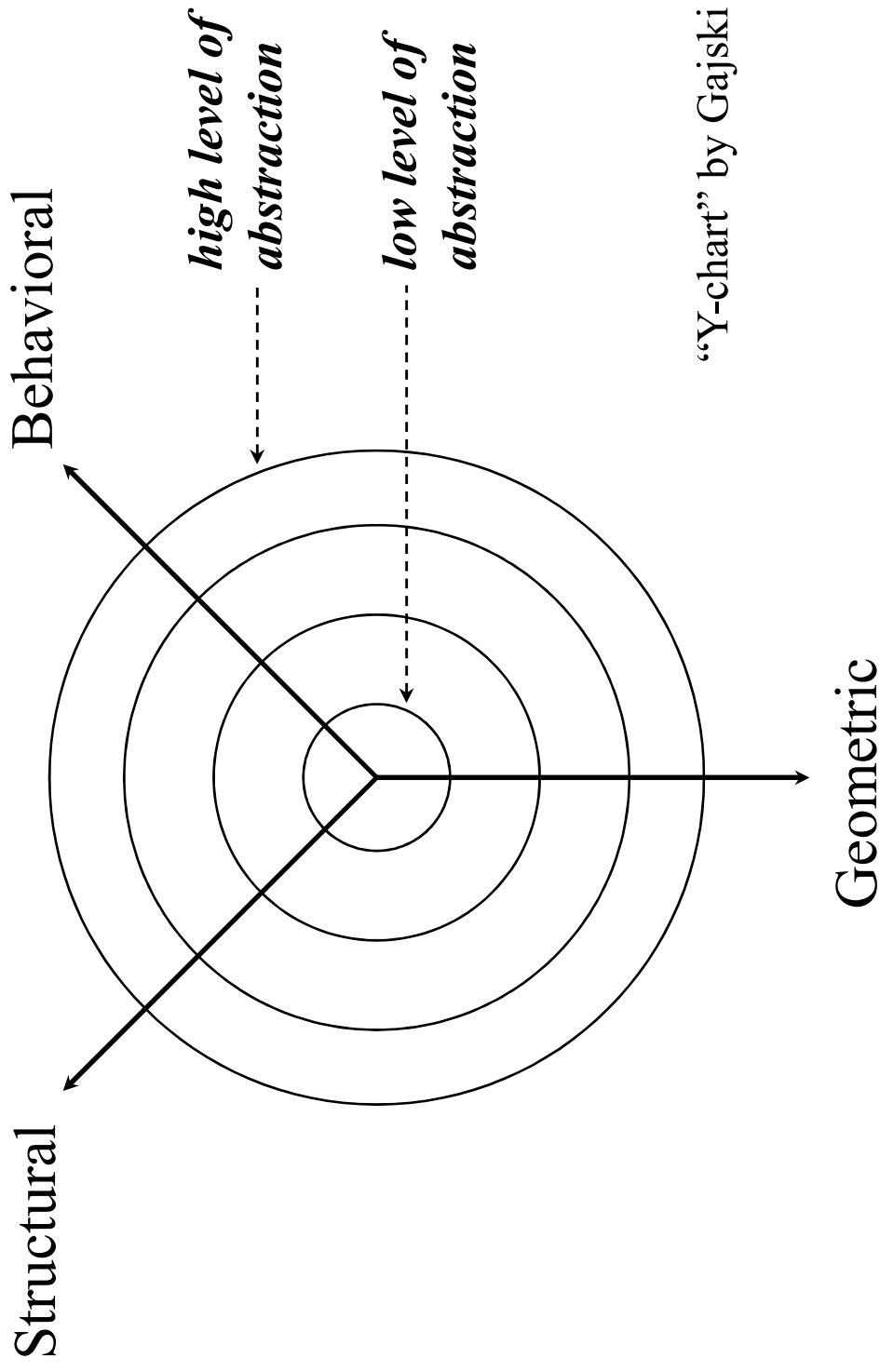
Domains and Levels of Modeling

The Y-Chart



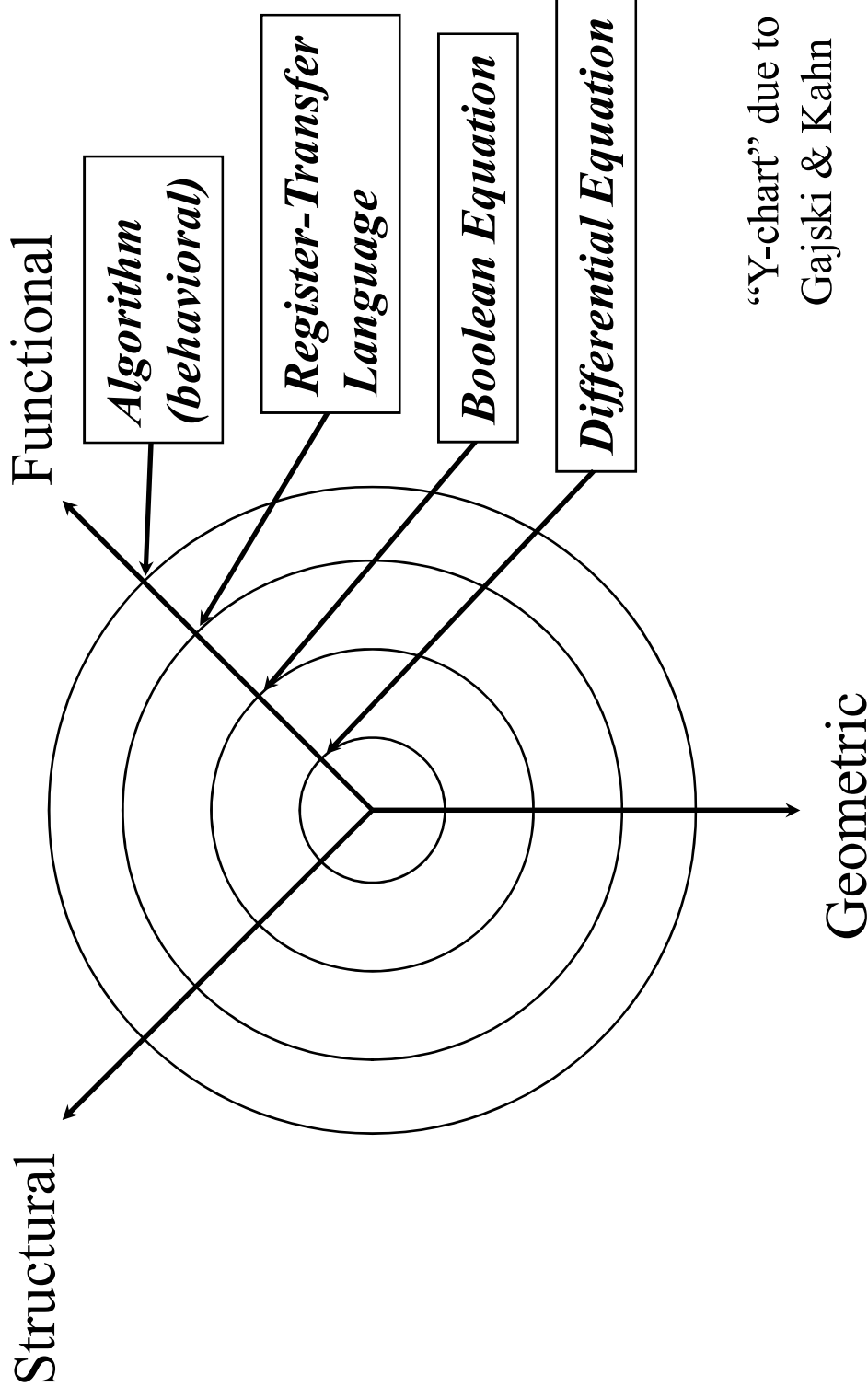
“Y-chart” by Gajski

Domains and Levels of Modeling



Gajski - “Y- Chart”

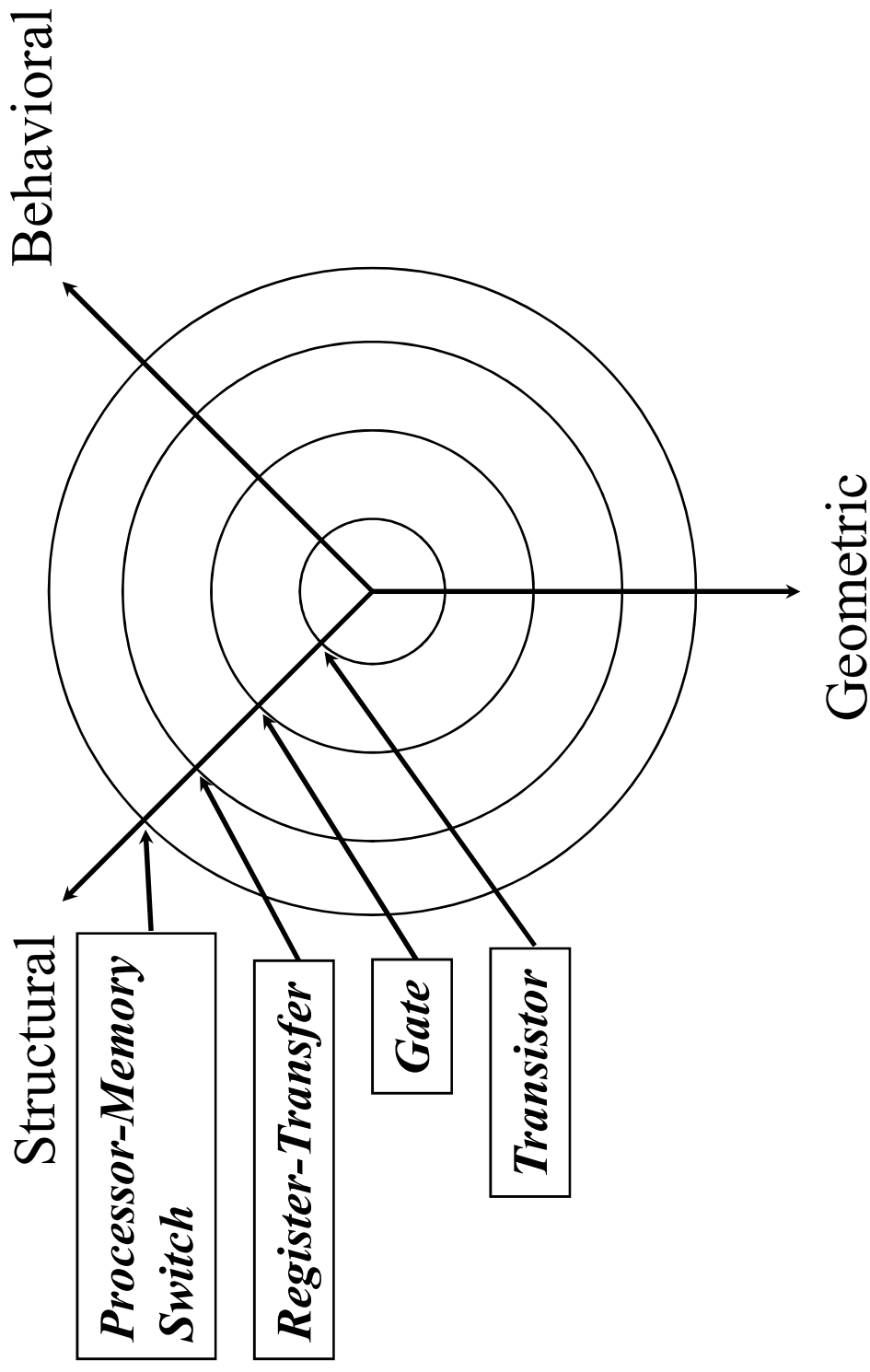
Domains and Levels of Modeling



“Y-chart” due to
Gajski & Kahn

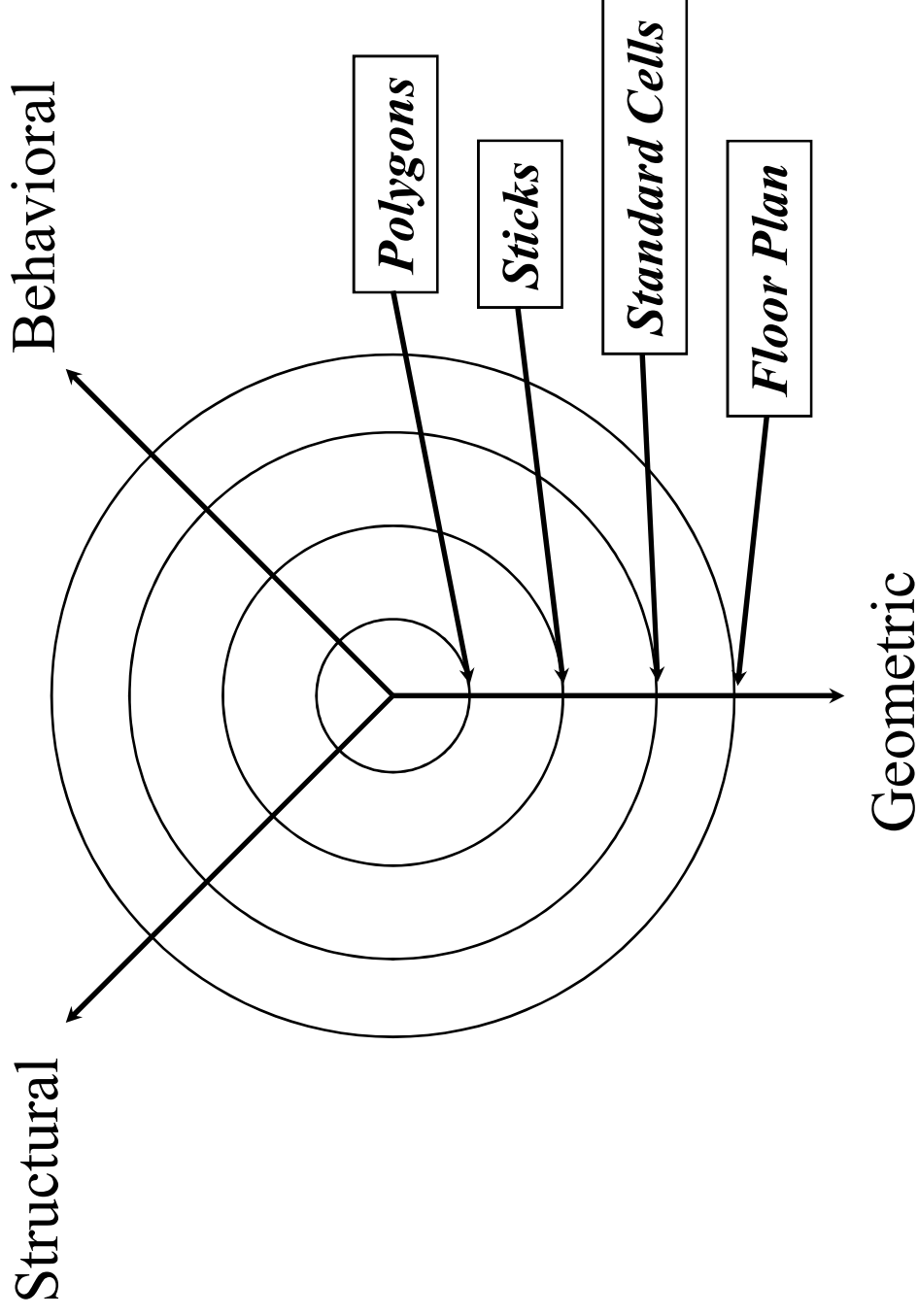
Gajski - “Y-Chart”

Domains and Levels of Modeling



Gajski - “Y- Chart”

Domains and Levels of Modeling



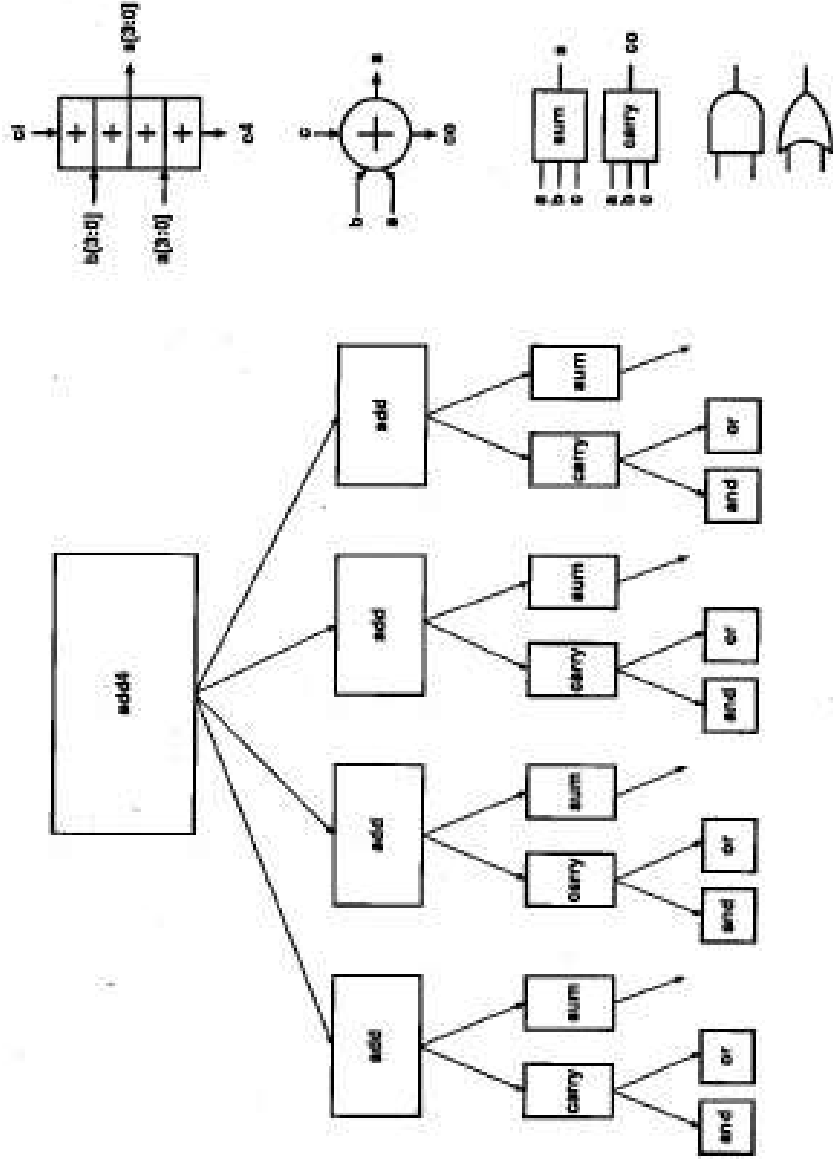
Gajski - “Y- Chart”

VLSI Design Process

- Move from higher to lower levels of abstraction
- Use CAD tools to automate parts of the process
- Use hierarchy to manage complexity

VLSI Design Hierarchy

- Hierarchy – Divide and conquer
- Divide a module into sub module and repeat this operation on sub module until the complexity becomes manageable.



Structural
decomposition of 4 bit
adder that shows the
levels of hierarchy

VLSI Design Hierarchy

Hierarchical design

Top-down design

- The initial work is quite abstract and theoretical and there is no direct connection to silicon until many steps have been completed
- Acceptable in modern digital system design
- Similar to *Cell-based Design Flow*

Bottom-up design

- starts at the silicon or circuit level and builds primitive units such as logic gates, adders, and registers as the first steps
- Acceptable for small projects
- Similar to *Full-custom Design Flow*

Regularity, Modularity and Locality

The hierarchical design approach reduces the design complexity by dividing the large system into several sub-modules. Usually, **other design concepts and design approaches are also needed to simplify the process.**

1) Regularity:

Decomposition of a large system in **simple and similar blocks as much as possible.**

2) Modularity:

- Modularity in design means that the various functional blocks which make up the larger system must have well-defined functions and interfaces.
- Modularity allows that each block or module can be designed relatively independently from each other.
- All of the blocks can be combined with ease at the end of the design process, to form the large system.
- The concept of **modularity enables the parallelization of the design process.**

3) Locality:

The concept of **locality also ensures that connections are mostly between neighboring modules**, avoiding long-distance connections as much as possible.

Challenges in VLSI Design

- Increasing integration
 - To reduce cost, size and power dissipation

Trends in VLSI

- Transistor
 - Smaller, faster, use less power
- Interconnect
 - Less delay, faster
- Yield
 - Smaller die size, higher yield

VLSI Design Tradeoffs

- **Performance**
 - Area
 - Speed
 - Power Consumption
 - Time-to-Market