ECE 340 Homework XIV Spring 2003

Due: Friday, April 25, 2003

1. Aluminum and polysilicon are commonly used as gate metals for the MOS structure in silicon. Assume that gold is used as the gate metal. Reconstruct a diagram similar to Figure 6-17 showing the variation of the metal-semiconductor work function potential difference Φ_{ms} with substrate doping concentration. The work function of Pt is 5.1 V and the electron affinity of silicon is 4.0 V. Show your work and draw to scale with accuracy.

2. (a) Find the voltage V_{FB} required to reduce to zero the negative charge induced at the semiconductor surface by a sheet of positive charge Q_{ox} located x' below the metal. (b) In the case of an arbitrary distribution of charge $\rho(x')$ in the oxide, show that

$$V_{FB} = -\frac{1}{C_i}\int_0^d \frac{x'}{d}\, r(x')dx'$$

3. The flat band voltage is shifted to –3V for an n^+-polysilicon-SiO_2-Si capacitor. The SiO_2 thickness is 200Å and the substrate doping is $N_d = 10^{16}/cm^3$. Find the value of interface charge Q_i required to cause this shift in V_{FB}, with Φ_{ms} given by Fig. 6-17.

4. An n^+-polysilicon-gate n-channel MOS structure is made on a p-type Si substrate with $N_a = 5x10^{15}/cm^3$. The SiO_2 thickness is 150Å in the gate region, and the effective interface charge Q_i is $5x10^{10}$ qC/cm^2. Find W_m, V_{FB}, V_T. Also, sketch the C-V curve for this device and give important numbers for the scale.