CrossLink Family

Data Sheet

FPGA-DS-02007 Version 1.5

July 2018

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
AR	Augmented Reality
ASIC	Application-Specific Integrated Circuit
BGA	Ball Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CSI	Camera Serial Interface
DBI	Display Bus Interface
DDR	Double Data Rate
DPI	Display Pixel Interface
DSI	Display Serial Interface
EBR	Embedded Block RAM
ECLK	Edge Clock
FPGA	Field-Programmable Gate Array
FPD	Flat Panel Display
GPIO	General-Purpose Input/Output
HFOSC	High Frequency Oscillator
HMI	Human Machine Interface
I^2C	Inter-Integrated Circuit
ISM	Industrial, Scientific, Medical
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
LVDS	Low-Voltage Differential Signaling
LVTTL	Low Voltage Transistor-Transistor Logic
MIPI	Mobile Industry Processor Interface
NVCM	Non-Volatile Configuration Memory
OTP	One Time Programmable
PCLK	Primary Clock
PFU	Programmable Functional Unit
PLL	Phase Locked Loops
PMU	Power Management Unit
RAM	Random Access Memory
Rx	Receive
SDR	Single Data Rate
SLVS200	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
TransFR	Transparent Field Reconfiguration
Tx	Transmit
UHD	Ultra-High-Definition
VR	Virtual Reality
WLCSP	Wafer Level Chip Scale Packaging

1. General Description

CrossLink™ from Lattice Semiconductor is a programmable video bridging device that supports a variety of protocols and interfaces for mobile image sensors and displays. The device is based on Lattice mobile FPGA 40-nm technology. It combines the extreme flexibility of an FPGA with the low power, low cost and small footprint of an ASIC.

CrossLink supports video interfaces including MIPI® DPI, MIPI DBI, CMOS camera and display interfaces, OpenLDI, FPD-Link, FLATLINK, MIPI D-PHY, MIPI CSI-2, MIPI DSI, SLVS200, SubLVDS, HiSPi and more.

Lattice Semiconductor provides many pre-engineered IP (Intellectual Property) modules for CrossLink. By using these configurable soft core IPs as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

The Lattice Diamond® design software allows large complex designs to be efficiently implemented using CrossLink. Synthesis library support for CrossLink devices is available for popular logic synthesis tools. The Diamond tools use the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the CrossLink device. The tools extract the timing from the routing and back-annotate it into the design for timing verification.

Interfaces on CrossLink provide a variety of bridging solutions for smart phone, tablets, wearables, VR, AR, Drone, Smart Home, HMI as well as adjacent ISM markets. The device is capable of supporting high-resolution, high-bandwidth content for mobile cameras and displays at 4 UHD and beyond.

1.1. Features

- Ultra-low power
  - Sleep Mode Support
  - Normal Operation – From 5 mW to 150 mW
- Ultra small footprint packages
  - 36-ball WLCSP (6 mm^2)
  - 64-ball ucfBGA (12 mm^2)
  - 80-ball ctfBGA (42 mm^2)
  - 80-ball ckfBGA (49 mm^2)
  - 81-ball csfBGA (20 mm^2)
- Programmable architecture
  - 5936 LUTs
  - 180 Kb block RAM
  - 47 Kb distributed RAM
- Two hardened 4-lane MIPI D-PHY interfaces
  - Transmit and receive
  - 6 Gb/s per D-PHY interface
- Programmable source synchronous I/O
  - MIPI D-PHY Rx, LVDS Rx, LVDS Tx, SubLVDS Rx, SLVS200 Rx, HiSPi Rx
  - Up to 1200 Mb/s per I/O
  - Four high-speed clock inputs
- Programmable CMOS I/O
  - LVTTL and LVCMOS
    - 3.3 V, 2.5 V, 1.8 V and 1.2 V (outputs)
  - LVCMOS differential outputs
- Flexible device configuration
  - One Time Programmable (OTP) non-volatile configuration memory
  - Master SPI boot from external flash
    - Dual image booting supported
  - I^2C programming
  - SPI programming
  - TransFR™ I/O for simple field updates
- Enhanced system level support
  - Reveal logic analyzer
  - TraceID for system tracking
  - On-chip hardened I^2C block
- Applications examples
  - Dual MIPI CSI-2 to Single MIPI CSI-2 Aggregation
  - Quad MIPI CSI-2 to Single MIPI CSI-2 Aggregation
  - Single MIPI DSI to Single MIPI DSI Repeater
  - Single MIPI CSI-2 to Single MIPI CSI-2 Repeater
  - Single MIPI DSI to Dual MIPI DSI Splitter
  - Single MIPI CSI-2 to Dual MIPI CSI-2 Splitter
  - MIPI DSI to OpenLDI/FPD-Link/LVDS Translator
  - OpenLDI/FPD-Link/LVDS to MIPI DSI Translator
  - MIPI DSI/CSI-2 to CMOS Translator
  - CMOS to MIPI DSI/CSI-2 Translator
  - SubLVDS to MIPI CSI-2 Translator

2. Product Feature Summary

Table 2.1 lists CrossLink device information and packages.

Table 2.1. CrossLink Feature Summary

Device	CrossLink
LUTs	5936
sysMEM Blocks (9 Kb)	20
Embedded Memory (Kb)	180
Distributed RAM Bits (Kb)	47
General Purpose PLL	1
NVCM	Yes
Embedded I^2C	2
Oscillator (10 KHz)	1
Oscillator (48 MHz)	1
Hardened MIPI D-PHY	2[1, 2]
Packages (Footprint, Pitch)	**I/O**
36 WLCSP[2] (2.535 × 2.583 mm^2, 0.4 mm)	17
64 ucfBGA (3.5 × 3.5 mm^2, 0.4 mm)	29
80 ctfBGA (6.5 x 6.5 mm^2, 0.65 mm)	37
80 ckfBGA (7.0 x 7.0 mm^2, 0.65 mm)	37
81 csfBGA (4.5 × 4.5 mm^2, 0.5 mm)	37

Notes:

1. Additional D-PHY Rx interfaces are available using programmable I/O.
2. Only one Hardened D-PHY is available in 36 WLCSP package.

3. Architecture Overview

CrossLink is designed as a flexible, chip-to-chip bridging solution which supports a wide variety of applications. The device provides three key building blocks for these bridging applications:

- Up to two embedded Hard D-PHY blocks
- Two banks of flexible programmable I/O supporting a variety of standards including D-PHY Rx, subLVDS, SLVS200, LVDS, and CMOS
- A programmable logic core providing the LUTs, memory, and system resources to implement a wide range of bridging operations

In addition to these blocks, CrossLink also provides key system resources including a Power Management Unit, flexible configuration interface, additional CMOS GPIO, and user I^2C blocks.

The block diagram for the device is shown in Figure 3.1.

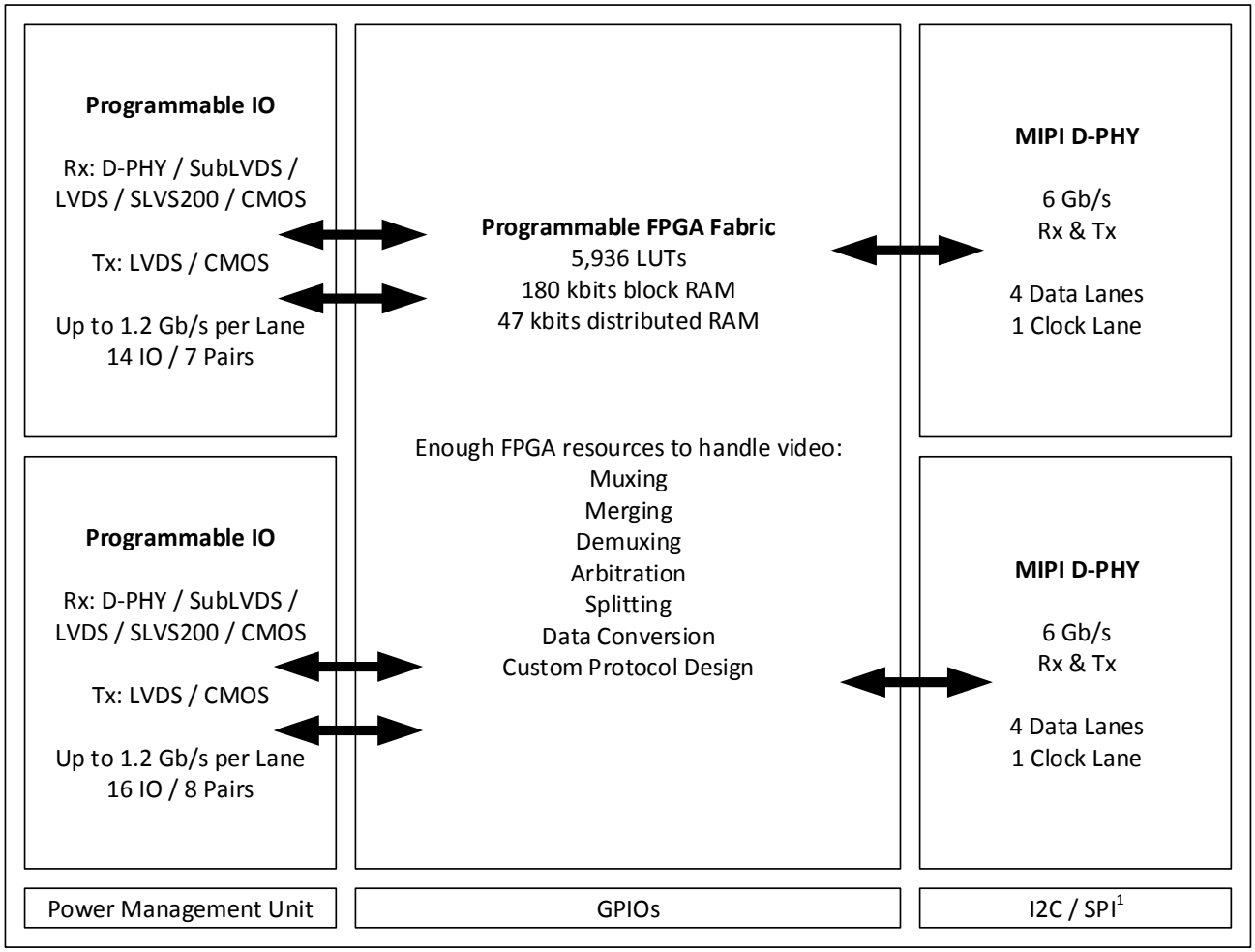


Figure 3.1. CrossLink Device Block Diagram

Note: I^2C and SPI configuration modes are supported. User mode hardened I^2C is also supported.

3.1. MIPI D-PHY Blocks

The top side of the device (Figure 3.2) includes two hard MIPI D-PHY quads. The D-PHY can be configured to support both camera interface (CSI-2) and display interface (DSI) applications. Below is a summary of the features supported by the hard D-PHY quads.

- Transmit and Receive compliant to MIPI Alliance Specification for D-PHY Revision 1.1
- High-Speed (HS) and Low-Power (LP) mode support (including built-in contention detect)
- Supports continuous clock mode or low power clock mode
- Up to 6 Gb/s per quad (1500 Mb/s data rate per lane)
- Dedicated PLL for Transmit Frequency Synthesis

Dedicated Serializer and De-Serializer blocks for fabric interfacingLattice Semiconductor provides a set of pre-engineered IP modules which include the full implementation and control of the hard D-PHY blocks to enable designers to focus on unique aspects of their design.

Figure 3.3 to Figure 3.6 show the signals connected to the fabric and the automatic settings when the hardened D-PHY is configured for the DSI/CSI-2 transmit and receive modes. Refer to CrossLink High-Speed I/O Interface (FPGA-TN-02012) for more information on the Hard D-PHY quads.

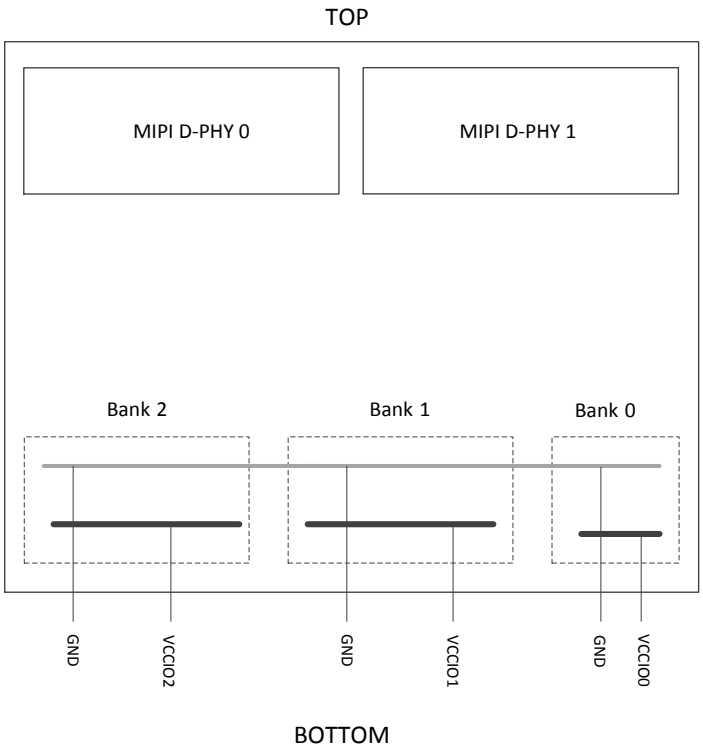


Figure 3.2. CrossLink sysI/O Banking

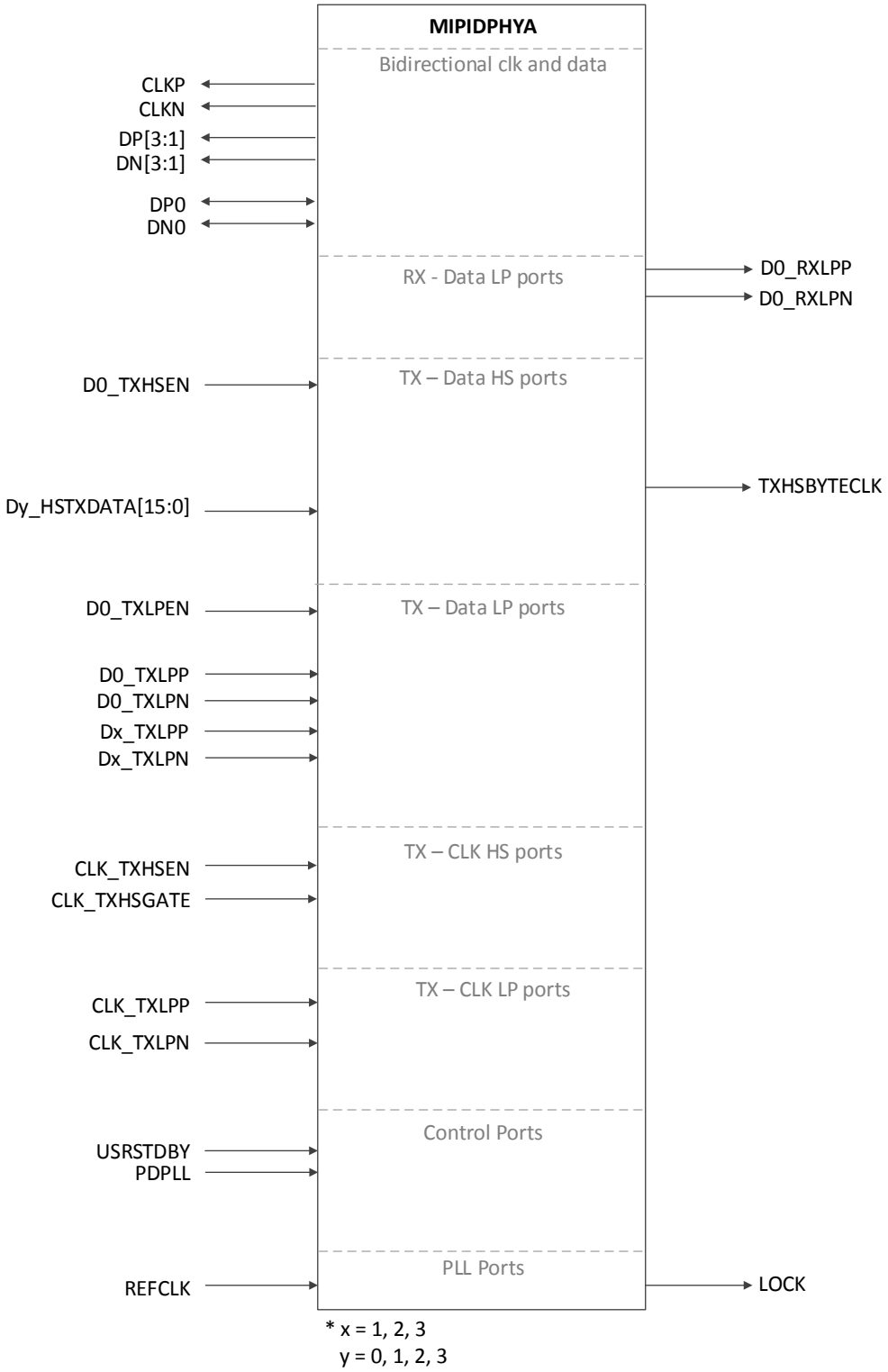


Figure 3.3. MIPI DSI Transmit Interface with Hard D-PHY Module

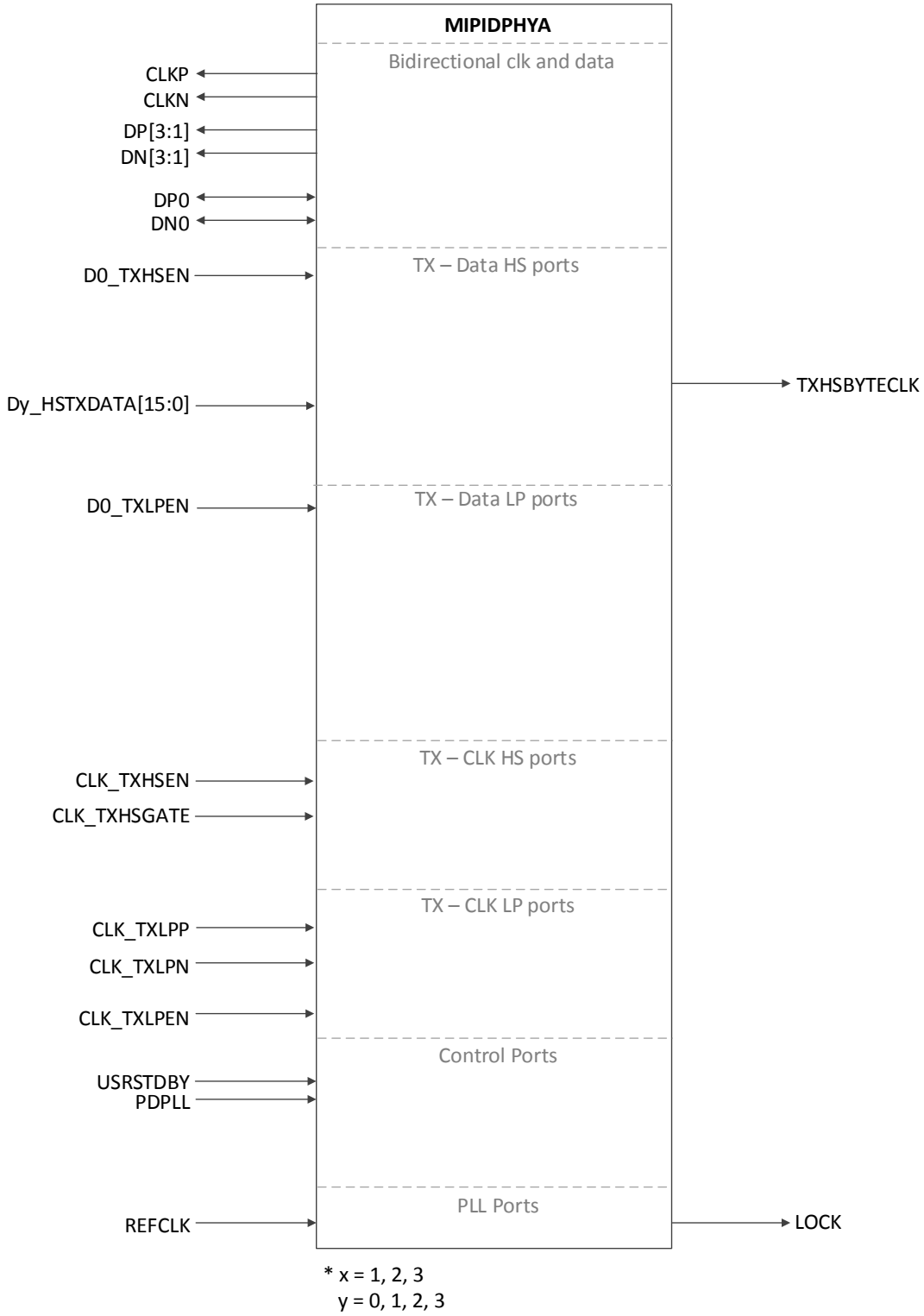


Figure 3.4. MIPI CSI-2 Transmit Interface with Hard D-PHY Module

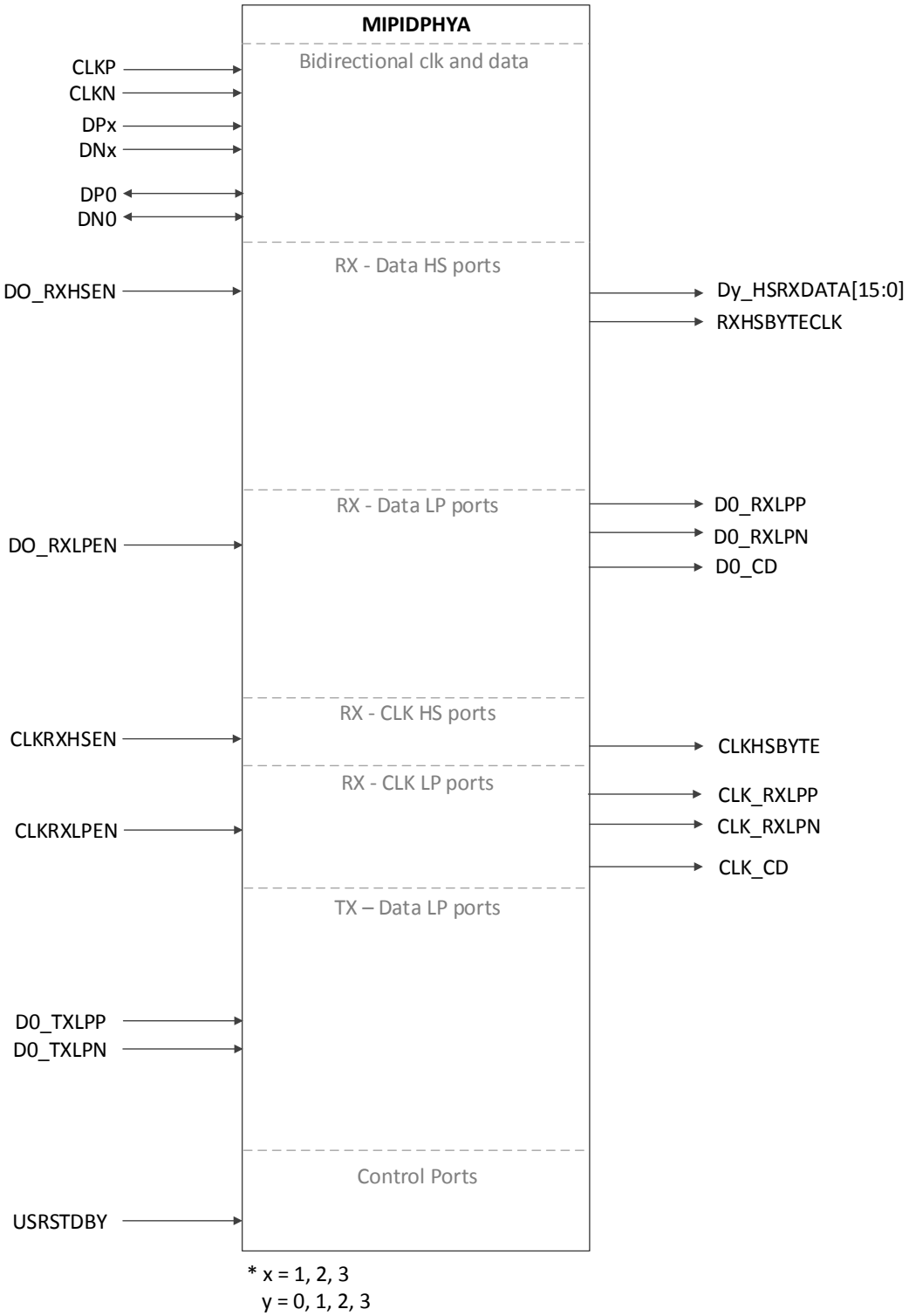


Figure 3.5. MIPI DSI Receive Interface with Hard D-PHY Module

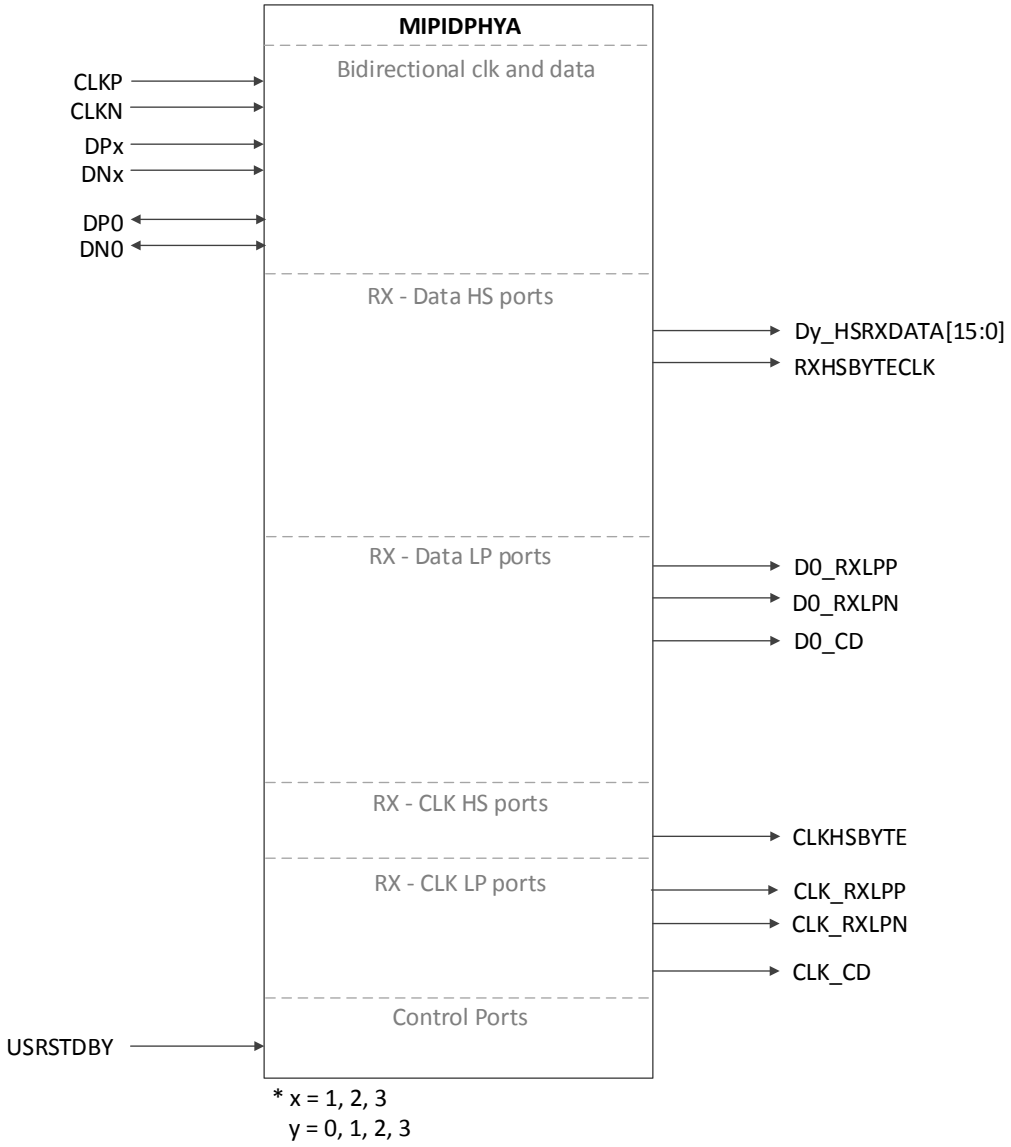


Figure 3.6. MIPI CSI-2 Receive Interface with Hard D-PHY Module

3.2. Programmable I/O Banks

CrossLink devices provide programmable I/O which can be used to interface to a variety of external standards on Banks 1 and 2. CrossLink devices also provide dedicated CMOS GPIOs on Bank 0. Bank 0 GPIOs only support Single Data Rate (SDR) interfaces, while Bank 1 and Bank 2 support both SDR and Double Data Rate (DDR) interfaces. The GPIOs on Bank 0 do not include differential signaling capabilities. The location of the three Banks and their associated supplies are shown in Figure 3.2.

Bank 0 features:

- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVTTL33
- Tri-state control for output
- Input/output register blocks
- Open-drain option and programmable input hysteresis
- Internal pull-up resistors with configurable values of 3.3 kΩ, 6.8 kΩ, and 10 kΩ

Bank 1 and Bank 2 features:

- Built-in support for the following differential standards
  - LVDS – Tx and Rx
  - SLVS200 – Rx
  - SubLVDS – Rx
  - MIPI – Rx (both LP and HS receive on a single differential pair)
- Support for the following single ended standards (ratioed to VCCIO)
  - LVCMOS33
  - LVCMOS25
  - LVCMOS18
  - LVCMOS12 (Outputs Only)
  - LVTTL33
- Independent voltage levels per bank based on VCCIO supply
- Input/output gearboxes per LVDS pair supporting several ratios for video interface applications
  - DDRX1, DDRX2, DDRX4, DDRX8 and DDRX71, DDRX141
  - Programmable delay cells to support edge-aligned and center-aligned interfaces
- Programmable differential termination (~ 100 Ω) with dynamic enable control
- Tri-state control for output
- Input/output register blocks
- Single-ended standards support open-drain and programmable input hysteresis
- Optional weak pull-up resistors

Table 3.1. CrossLink Output Support per Bank Basis

OUTPUT	BANK 0	BANK 1	BANK 2
LVCMOS12	—	✓	✓
LVCMOS18	✓	✓	✓
LVCMOS25	✓	✓	✓
LVCMOS33	✓	✓	✓
LVTTL33	✓	✓	✓
LVDS25	—	✓	✓

Table 3.2. CrossLink Input Support per Bank Basis

INPUT	BANK 0	BANK 1	BANK 2
LVCMOS12	—	—	—
LVCMOS18	✓	✓	✓
LVCMOS25	✓	✓	✓
LVCMOS33	✓	✓	✓
LVTTL33	✓	✓	✓
LVDS25	—	✓	✓
MIPI D-PHY	—	✓	✓
SLVS200	—	✓	✓
subLVDS	—	✓	✓

3.3. sysI/O Buffers

The CrossLink sysI/O buffers are distributed across three banks located at the bottom of the CrossLink device as shown in Figure 3.2. The sysI/O buffers support a wide variety of standards to interface to a range of systems including LVDS, subLVDS, LVCMOS, LVTTL, SLVS200 and MIPI. CrossLink supports single-ended buffers on all three banks. Differential I/O is supported on Bank 1 and Bank 2.

3.3.1. Programmable PULLMODE Settings

The CrossLink sysI/O buffers offer multiple programmable value pull-up resistors on the three banks. The pull-up values are programmable on a “per-pin” basis. The default state of the I/O pins prior to configuration is tri-stated with a weak pull-up to V_{CCIOx}. The I/O pins convert to the software user-defined settings after the configuration bitstream has been successfully downloaded to the device. Each sysIO buffer can be programmed with a 100 kΩ (weak pull-up), 3.3 kΩ, 6.8 kΩ, 10 kΩ or no pull-up. These pull-up options allow an I^2C interface to be place on the majority of the pins on the device. These options are not exclusively for I^2C protocol and may be used for other functions.

3.3.2. Output Drive Strength

Each CrossLink output can have its own individual drive strength setting, but is predefined based on the V_{CCIOx} setting. Table 3.3 lists the drive settings for the corresponding I/O type.

Table 3.3. Drive Strength Values

VCCIOx (V)	I/O Type	Drive Strength (mA)
3.3	LVTTL33	8
3.3	LVCMOS33	8
2.5	LVCMOS25	6
1.8	LVCMOS18	4
1.2	LVCMOS12	2

3.3.3. On-Chip Termination

Bank 1 and bank 2 of CrossLink support LVDS, SLVS200 subLVDS and MIPI D-PHY inputs. These two banks support on-chip 100 Ω input differential termination between LVDS, SLVS200 and subLVDS pairs. For MIPI D-PHY inputs, the on-chip 100 Ω termination is dynamically enabled based on the HSSEL (High Speed Select) signal.

See CrossLink High-Speed I/O Interface (FPGA-TN-02012) and CrossLink sysI/O Usage Guide (FPGA-TN-02016) for details.

3.4. Programmable FPGA Fabric

CrossLink is built around a programmable logic fabric consisting of 5936 four input lookup tables (LUT4) arranged alongside dedicated registers in Programmable Functional Units (PFU). These PFU blocks are the building blocks for logic, arithmetic, RAM and ROM functions. The PFU blocks are connected via a programmable routing network. The Lattice Diamond design software configures the PFU blocks and the programmable routing for each unique design. Interspersed between rows of PFU are rows of sysMEM™ Embedded Block RAM (EBR), with programmable I/O banks, embedded I^2C and embedded MIPI D-PHY arranged on the top and bottom of the device as shown in Figure 3.7.

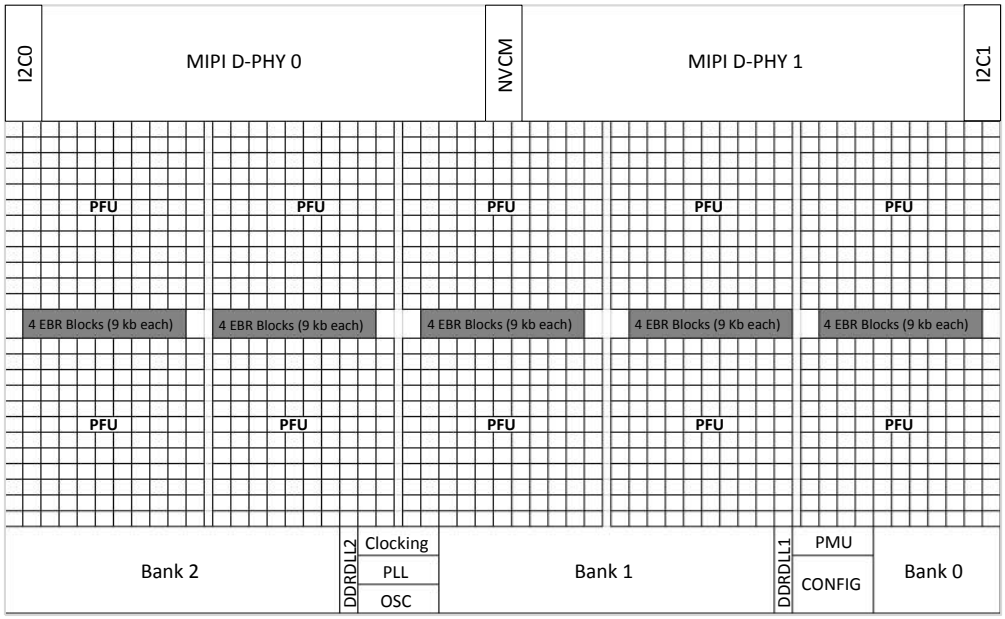


Figure 3.7. CrossLink Device Simplified Block Diagram (Top Level)

3.4.1. PFU Blocks

The core of the CrossLink device consists of PFU blocks. Each PFU block consists of four interconnected slices numbered 0 – 3 as shown in Figure 3.8. Each slice contains two LUTs. All the interconnections to and from PFU blocks are from routing. The PFU block can be used in Distributed RAM or ROM function, or used to perform Logic, Arithmetic or ROM functions.

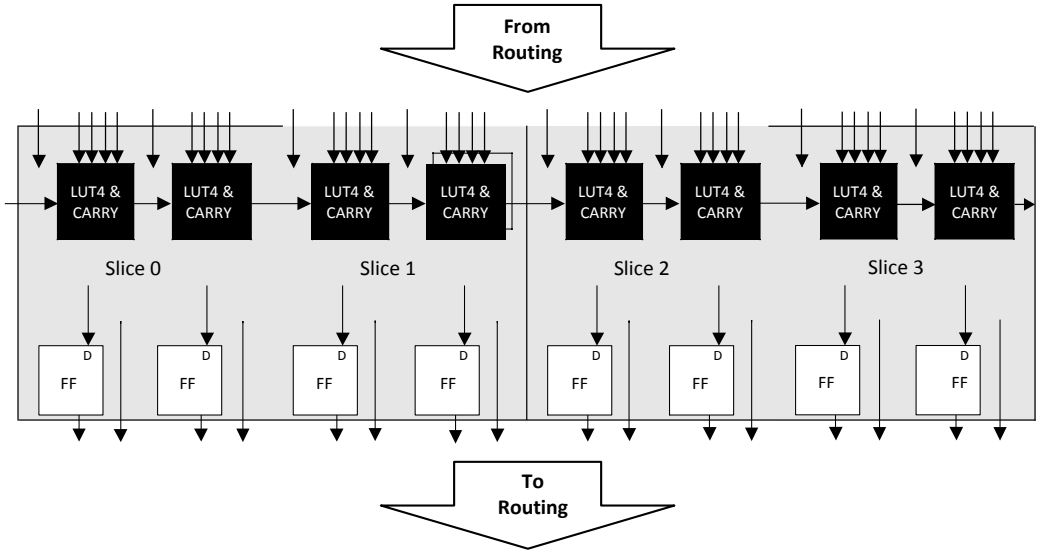
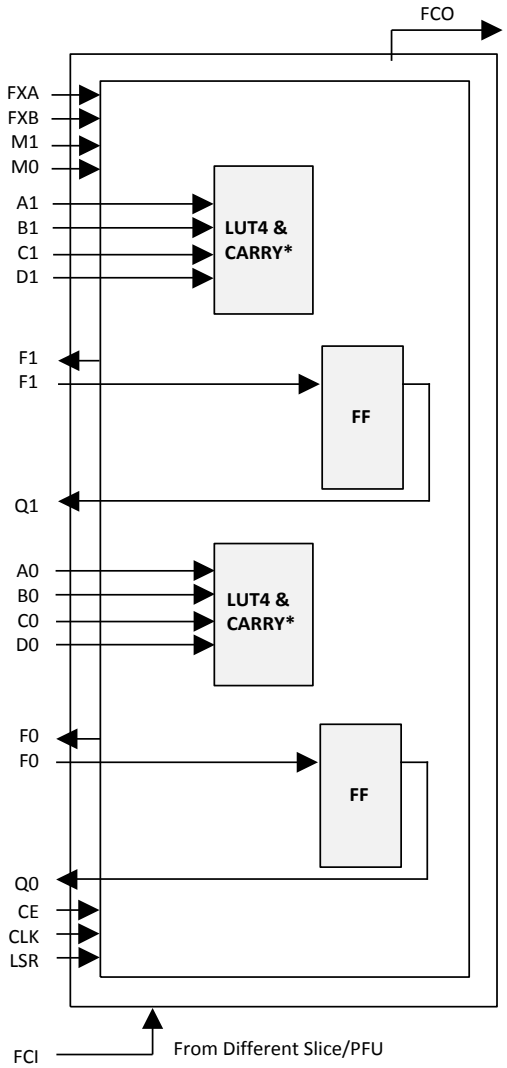


Figure 3.8. CrossLink PFU Diagram

3.4.2. Slice

Each slice contains two LUT4s feeding two registers. Each PFU contains logic that allows the LUTs to be combined to perform functions such as LUT5, LUT6, LUT7 and LUT8. There is control logic to perform set/reset functions (programmable as synchronous/asynchronous), clock select, chip-select and wider RAM/ROM functions. Figure 3.9 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/negative and edge triggered or level sensitive clocks.

Each slice has 14 input signals: 13 signals from routing and 1 signal from the carry-chain routed from the adjacent slice or PFU. There are five outputs: four to routing and one to carry-chain (to the adjacent PFU). There are two inter slice/PFU output signals that are used to support wider LUT functions, such as LUT6, LUT7, and LUT8. Table 3.4 and Figure 3.10 list the signals associated with all the slices. Figure 3.8 shows the connectivity of the inter-slice/PFU signals that support LUT5, LUT6, LUT7, and LUT8.



Notes: For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:
WCK is CLK
WRE is from LSR
DI[3:2] for Slice 1 and DI[1:0] for Slice 0 data from Slice 2
WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 3.9. Slice Diagram

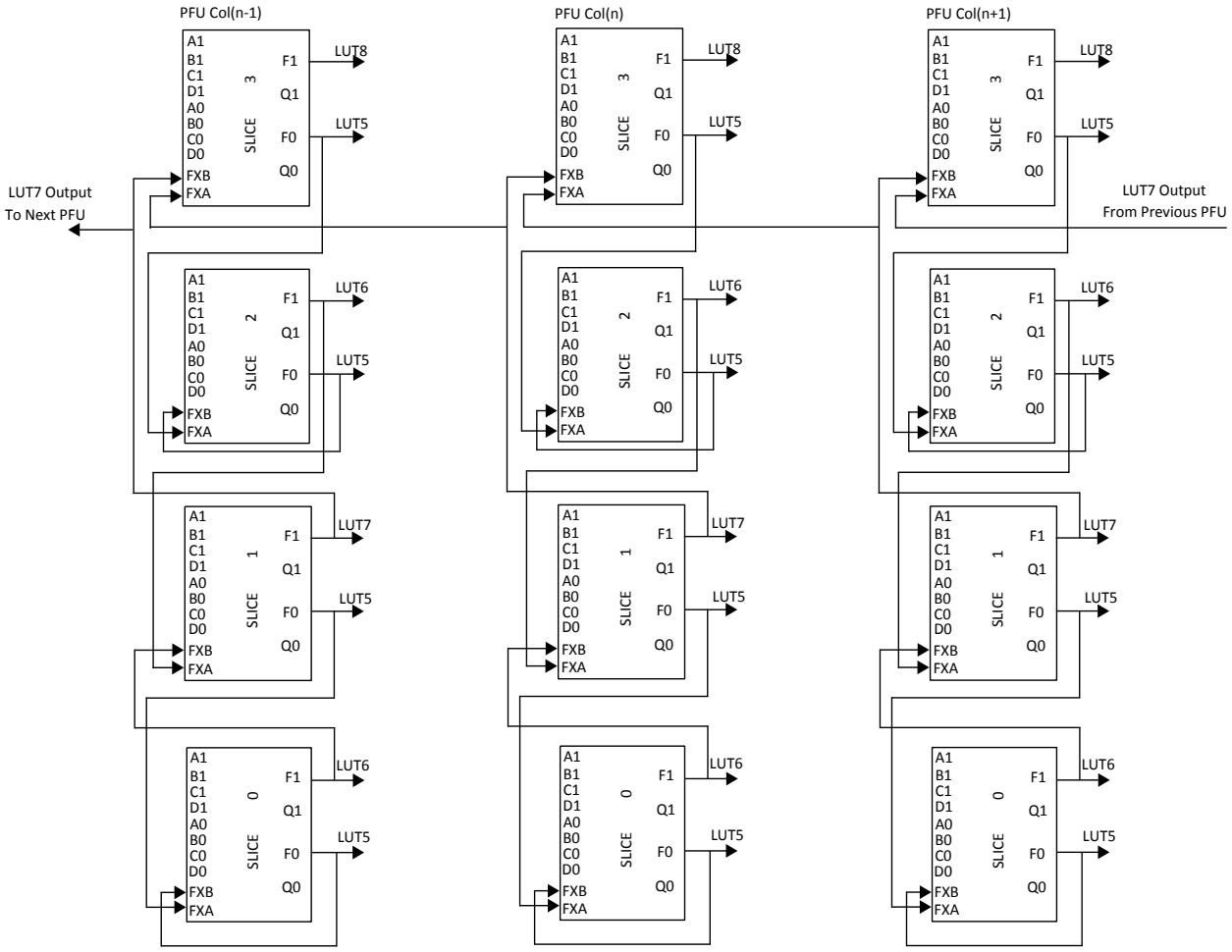


Figure 3.10. Connectivity Supporting LUT5, LUT6, LUT7 and LUT8

Table 3.4. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0	Multipurpose Input
Input	Multi-purpose	M1	Multipurpose Input
Input	Control signal	CE	Clock Enable
Input	Control signal	LSR	Local Set/Reset
Input	Control signal	CLK	System Clock
Input	Inter-PFU signal	FCI	Fast Carry-in[1]
Input	Inter-slice signal	FXA	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Input	Inter-slice signal	FXB	Intermediate signal to generate LUT6, LUT7 and LUT8[2]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Inter-PFU signal	FCO	Fast carry chain output[1]

Notes:

1. See Figure 3.9 for connection details.
2. Requires two adjacent PFUs.

3.5. Clocking Structure

The CrossLink device family provides resources to support a wide range of clocking requirements for programmable video bridging. These resources are described below. For details, refer to CrossLink sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02015).

3.5.1. sysCLK PLL

The CrossLink sysCLK PLL provides the ability to synthesis clock frequencies (See Table 4.14 for input frequency range). The PLL provides features such as dynamic selectable clock input, clock injection delay removal, independent dynamic output enable control, and programmable output phase adjustment. The architecture of the PLL is shown in Figure 3.11 and followed by a description of the PLL blocks.

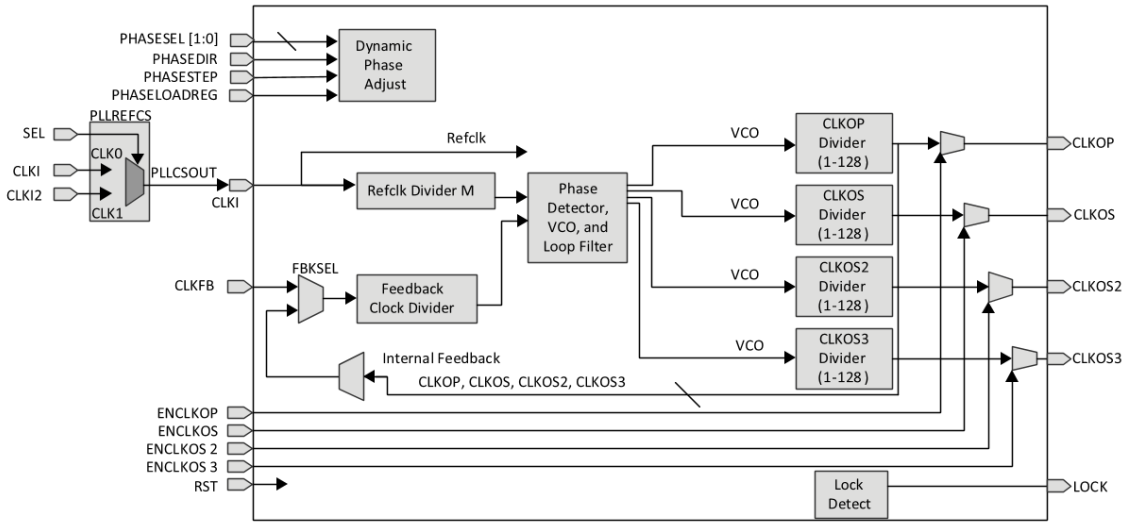


Figure 3.11. CrossLink PLL Block Diagram

Table 3.5 provides a description of the signals in the PLL block.

Table 3.5. CrossLink PLL Port Definition

Signal	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
USRSTDBY	I	User port to put the PLL to sleep mode
PHASESEL[1:0]	I	Select the output affected by Dynamic Phase adjustment
PHASEDIR	I	Dynamic phase adjustment direction
PHASESTEP	I	Dynamic phase adjustment step
PHASELOADREG	I	Load dynamic phase adjustment values into PLL
RST	I	Resets the whole PLL
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS
ENCLKOS2	I	Enable PLL output CLKOS2
ENCLKOS3	I	Enable PLL output CLKOS3
PLLWAKESYNC	I	Enable PLL switching from internal to user feedback path when PLL wake up
CLKOP	O	PLL main output clock
CLKOS	O	PLL output clock
CLKOS2	O	PLL output clock
CLKOS3	O	PLL output clock
LOCK	O	PLL LOCK to CLKI, asynchronous signal. Active high indicates PLL lock

3.5.2. Primary Clocks

The primary clock routing network is made up of low skew clock routing resources with connectivity to every synchronous element of the device. Primary clock sources are selected in the center mux and distributed on the primary clock routing to clock the synchronous elements in the FPGA fabric. CrossLink family of devices provide up to eight unique global primary clocks. Primary clock sources are:

- LVDS PIO pins
- GPIO pins
- PLL outputs
- Clock dividers
- Fabric internally generated clock signal
- Divided down clock from DPHY
- OSCI

The routing clock structure is shown in Figure 3.12.

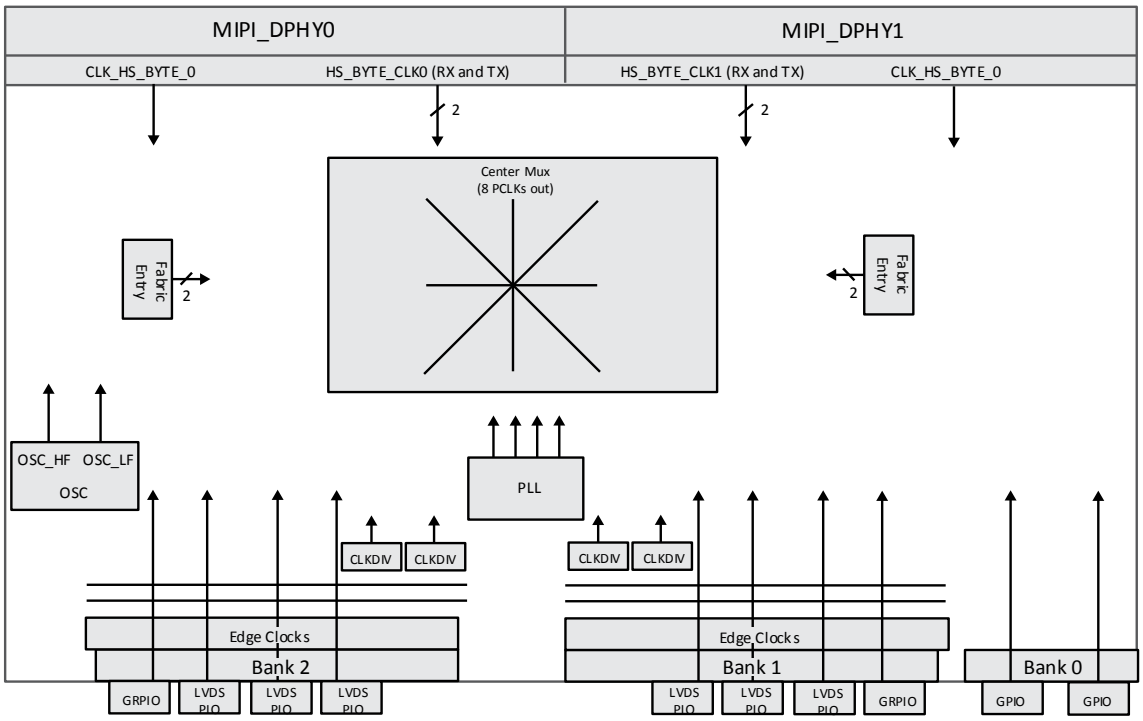


Figure 3.12. CrossLink Clocking Structure

3.5.3. Edge Clocks

The CrossLink device has Edge Clock (ECLK) at the bottom 2 banks (Bank 1 and Bank 2) of the device (Figure 3.3). The CrossLink device has 2 edge clocks per Programmable I/O bank. These clocks, which have low injection time and skew, are used to clock I/O registers. Edge clock resources are designed for high speed I/O interfaces with high fan-out capability. The sources of edge clocks are:

- Dedicated Clock (PCLK) pins muxed with the DLLDEL output
- PLL outputs (CLKOP and CLKOS)
- Internal nodes

ELCK input MUX collects all clock sources as shown in Figure 3.13 below. There are two ECLK Input MUXs, one on each bank. It drives the ECLK SYNC modules and the ECLK Clock Divider through a 2 to 1 MUX.

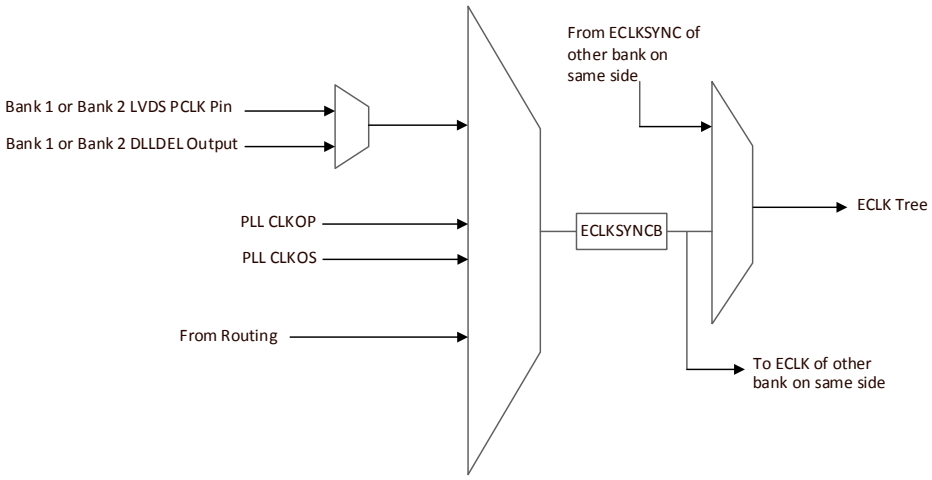


Figure 3.13. CrossLink Edge Clock Sources per Bank

3.5.4. Dynamic Clock Enables

Each PLL output has a user input signal to dynamically enable/disable its output to provide a glitch free clock. Then the clock enable signal is set to logic '0', the corresponding output clock is held to logic '0'. This allows the user to save power by stopping the corresponding output clock when not in use.

3.5.5. Internal Oscillator (OSCI)

The OSCI element performs multiple functions on the CrossLink device. It is used for configuration and available during user mode. OSCI element has the following features in user mode:

- Always-on low frequency clock output (LFCLKOUT) with nominal frequency of 10 kHz
- High-frequency clock output (HFCLKOUT) with nominal frequency of 48 MHz that can be enabled or disabled using HFOUTEN input
- Programmable output dividers (HFCLKDIV) for 48 MHz, 24 MHz, 12 MHz or 6 MHz HFCLKOUT output
- Both output clocks have a direct connection to primary clock routing
- Figure 3.14, Table 3.6 and Table 3.7 below show the OSCI definitions

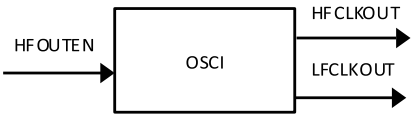


Figure 3.14. CrossLink OSCI Component Symbol

Table 3.6. OSCI Component Port Definition

Port Name	I/O	Description
HFOUTEN	I	High frequency clock output enable
HFCLKOUT	O	High frequency clock output
LFCLKOUT	O	Low Frequency clock output

Table 3.7. OSCI Component Attribute Definition

Defparam Name	Description	Value	Default
HFCLKDIV	Configure HF oscillator output divider	1, 2, 4, 8	1

3.6. Embedded Block RAM Overview

CrossLink devices contain sysMEM Embedded Block RAM (EBR). The EBR consists of a 9-KB RAM with memory core, dedicated input registers and output registers with separate clock and clock enable.

Support for different memory configurations:

- Single Port
- True Dual Port
- Pseudo Dual Port
- ROM
- FIFO (logic wrapper added automatically by design tools)

Flexible customization features:

- Initialization of RAM/ROM
- Memory cascading (handled automatically by design tools)
- Optional parity bit support
- Byte-enable
- Multiple block size options
- RAM modes support optional Write Through or Read-Before-Write modes

For details, refer to CrossLink Memory Usage Guide (FPGA-TN-02017).

Table 3.8. sysMEM Block Configurations

Memory Mode	Memory Size Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
ROM	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

3.7. Power Management Unit

The embedded Power Management Unit (PMU) allows low-power Sleep State of the device. Figure 3.15 shows the block diagram of the PMU IP.

When instantiated in the design, PMU is always on, and uses the low-speed clock from oscillator of the device to perform its operations.

The typical use case for the PMU is through a user implemented state machine that controls the sleep and wake up of the device. The state machine implemented in the FPGA fabric identifies when the device needs to go into sleep mode, issues the command through PMU's FPGA fabric interface, assigns the parameters for sleep (time to wake up and so on) and issues Sleep command.

The device can be woken up externally using the PMU Wake-Up (USRWKUP) pin, or from the PMU Watch Dog Timer expiry or from I2C0 (address decoding detection or FIFO full in one of hardened I^2C).

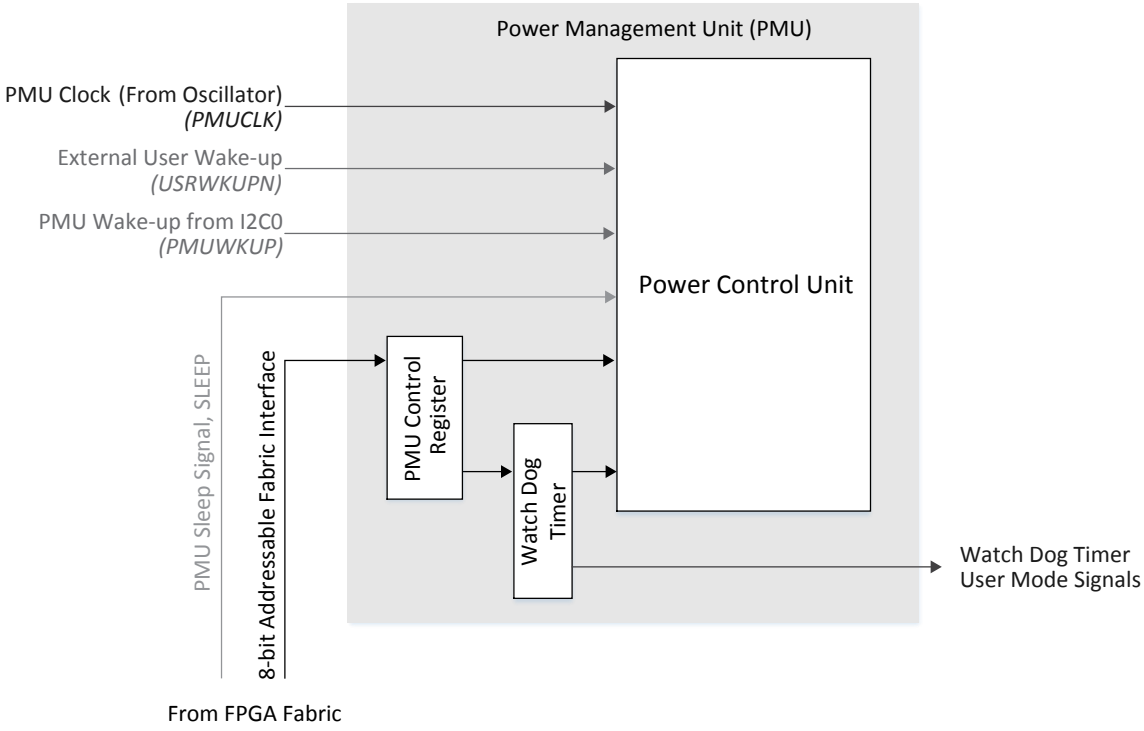


Figure 3.15. CrossLink MIPI D-PHY Block

3.7.1. PMU State Machine

PMU can place the device in two mutually exclusive states – Normal State and Sleep State. Figure 3.16 shows the PMU State Machine triggers for transition from one state to the other.

- Normal state – All elements of the device are active to the extent required by the design. In this state, the device is at fully active and performing as required by the application.
  Note that the power consumption of the device is highest in this state.
- Sleep state – The device is power gated such that the device is not operational. The configuration of the device and the EBR contents are retained; thus in Sleep mode, the device does not lose configuration SRAM and EBR contents. When it transitions to Normal state, device operates with these contents preserved.
  The PMU is active along with the associated GPIOs.
  The power consumption of the device is lowest in this state. This helps reduce the overall power consumption for the device.

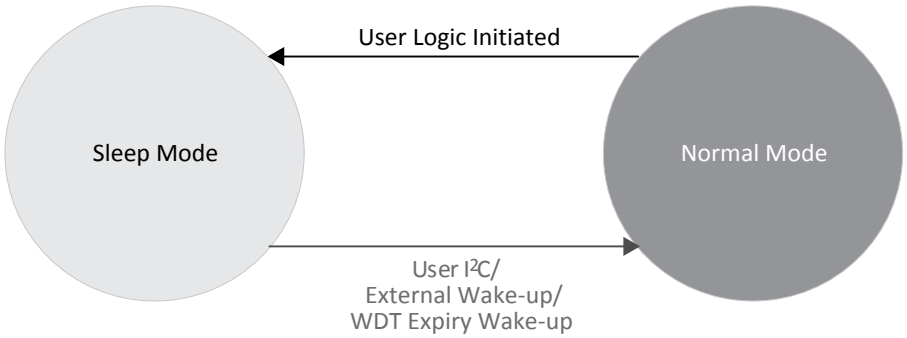


Figure 3.16. CrossLink PMU State Machine

For more details, refer to Power Management and Calculation for CrossLink Devices (FPGA-TN-02018).

3.8. User I²C IP

CrossLink devices have two I²C IP cores that can be configured either as an I²C master or as an I²C slave. The I2C0 core has pre-assigned pins, and supports PMU wakeup over I²C. The pins for the I2C1 interface are not pre-assigned – user can use any General Purpose I/O pins.

The I²C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Clock stretching
- Up to 1 MHz data transfer speed
- General call support
- Optionally delaying input or output data, or both
- Optional FIFO mode
- Transmit FIFO size is 10 bits x 16 bytes, receive FIFO size is 10 bits x 32 bytes

For further information on the User I²C, refer to CrossLink I2C Hardened IP Usage Guide (FPGA-TN-02019).

3.9. Programming and Configuration

CrossLink is a SRAM-based programmable logic device that includes an internal Non-Volatile Configuration Memory (NVCM), as well as flexible SPI and I^2C configuration modes. CrossLink provides four modes for loading the configuration data into the SRAM memory.

- Self-Download (NVCM) mode – CrossLink retrieves bitstream from internal NVCM
- Master SPI mode – CrossLink retrieves bitstream from an external SPI Flash
- Slave SPI mode – System microprocessor writes bitstream to CrossLink through SPI port
- Slave I^2C mode – System microprocessor writes bitstream to CrossLink through I^2C port

CrossLink provides a set of sysCONFIG I/O pins to program and configure the FPGA. The sysCONFIG pins are grouped together to create ports (I^2C, SSPI or MSPI) that are used to interact with the FPGA for programming, configuration, and access of resources inside the FPGA. The sysCONFIG pins (Table 3.9) in a configuration group may be active and used for programming the FPGA or they can be reconfigured to act as general purpose I/Os.

Table 3.9. CrossLink sysCONFIG Pins

Pin Name	Associated sysCONFIG Port
CRESETB	Self Download Mode/SSPI/MSPI/I^2C
CDONE	Self Download Mode/SSPI/MSPI/I^2C
SPI_SCK/MCK/SDA	SSPI/MSPI/I^2C
SPI_SS/CSN/SCL	SSPI/MSPI/I^2C
MOSI	SSPI/MSPI
MISO	SSPI/MSPI

As external power ramps up, a Power On Reset (POR) circuit inside the FPGA becomes active. When POR conditions are met, the POR circuit releases an internal reset strobe, allowing the device to begin its initialization process. After CrossLink drives CDONE low, CrossLink enters the memory initialization phase where it clears all of the SRAM memory inside the FPGA. CrossLink remains in initialization state until the CRESETB pin is deasserted or after SSPI/SI^2C activation code is received.

- After CRESETB goes from low to high, the Configuration Logic puts the device into master auto booting mode where it boots either from the internal NVRAM or an external SPI boot PROM.
- Holding the CRESETB low postpones the master auto booting event and allows the slave configuration ports (Slave SPI or Slave I^2C) to detect a 'Slave Active' condition where the SPI or I^2C Master sends an Activation Key code to CrossLink. An external SPI Master or I^2C Master needs to write the Activation Key to the FPGA while CRESETB is held LOW and within 9.5 ms from V_{CC} min during power up to enter into one of the slave configuration modes.
- Sources should not drive output to CrossLink until configuration has been completed to ensure CrossLink is in a known state.

In addition to the flexible configuration modes, the CrossLink configuration engine supports the following special features:

- TransFR (Transparent Field Reconfiguration) allowing users to update logic in field without interrupting system operation by freezing I/O states during configuration
- Dual-Boot Support for primary and golden bitstreams provides automatic recovery from configuration failures
- Security and One-Time Programmable (OTP) modes protect bitstream integrity and prevent readback
- 64-bit unique TraceID per device

For more information, refer to CrossLink Programming and Configuration Usage Guide (FPGA-TN-02014).

4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings [1, 2, 3]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	–0.5	1.32	V
V_{CCGPLL}	PLL Supply Voltage	–0.5	1.32	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 2.5 V[4]	–0.5	2.75	V
	Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 3.3 V[4]	–0.5	3.63	V
V_{CCIO}	I/O Driver Supply Voltage for Banks 0, 1, 2	–0.5	3.63	V
—	Input or I/O Transient Voltage Applied	–0.5	3.63	V
V_{CCA_DPHYx} V_{CCPLL_DPHY} V_{CCMU_DPHY1}	MIPI D-PHY Supply Voltages	–0.5	1.32	V
—	Voltage Applied on MIPI D-PHY Pins	–0.5	1.32	V
T_A	Storage Temperature (Ambient)	–65	150	°C
T_J	Junction Temperature (TJ)	—	+125	°C

Notes:

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. V_{CCAUX} must be set to 2.5 V when an external I^2C Master or SPI Master is used to program CrossLink’s NVCM. This restriction is not applicable for read access of the NVCM, such as Self-Download Mode, where the NVCM is already programmed and CrossLink retrieves the bitstream from the NVCM and programs it to the SRAM memory.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions [1, 2]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Core Supply Voltage	1.14	1.26	V
V_{CCGPLL}	PLL Supply Voltage	1.14	1.26	V
V_{CCAUX}	Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 2.5 V[3]	2.375	2.625	V
	Auxiliary Supply Voltage for Bank 1, 2 and NVCM - @ 3.3 V[3]	3.135	3.465	V
V_{CCIO0}	I/O Driver Supply Voltage for Bank 0	1.71	3.465	V
$V_{CCIO1/2}$	I/O Driver Supply Voltage for Bank 1, 2	1.14	3.465	V
T_{JIND}	Junction Temperature, Industrial Operation	–40	100	°C
D-PHY External Power Supply				
V_{CCA_DPHYx}	Analog Supply Voltage for D-PHY	1.14	1.26	V
V_{CCPLL_DPHYx}	PLL Supply voltage for D-PHY	1.14	1.26	V
V_{CCMU_DPHY1}	Supply for V_{CCA_DPHY1} and V_{CCPLL_DPHY1} on the WLCSP36 package	1.14	1.26	V

Notes:

1. For Correct Operation, all supplies must be held in their valid operation range.
2. Like power supplies, must be tied together if they are at the same supply voltage. Follow the noise filtering recommendations in CrossLink Hardware Checklist (FPGA-TN-02013).
3. V_{CCAUX} must be set to 2.5 V when an external I^2C Master or SPI Master is used to program CrossLink’s NVCM. This restriction is not applicable for read access of the NVCM, such as Self-Download Mode, where the NVCM is already programmed and CrossLink retrieves the bitstream from the NVCM and programs it to the SRAM memory.

4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates*

Symbol	Parameter	Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	0.6	10	V/ms

***Note**: Assume monotonic ramp rates.

4.4. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels 1, 3, 4

Symbol	Parameter		Min	Max	Unit
V_{PORUP}	Power-On-Reset ramp up trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	0.62	0.93	V
		V_{CCIO0}[2]	0.87	1.50	V
		V_{CCAUX}	0.90	1.53	V
V_{PORDN}	Power-On-Reset ramp down trip point (Monitoring V_{CC}, V_{CCIO0}, and V_{CCAUX})	V_{CC}	—	0.79	V
		V_{CCIO0}[2]	—	1.50	V
		V_{CCAUX}	—	1.53	V

Notes:

1. These POR ramp up trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
2. Only V_{CCIO0} (Config Bank) has a Power-On-Reset ramp up trip point. All other VCCIOs do not have Power-On-Reset ramp up detection.
3. V_{CCIO} supplies should be powered-up before or together with the V_{CC} and V_{CCAUX} supplies.
4. Configuration starts after V_{CC}, V_{CCIO0} and V_{CCAUX} reach V_{PORUP}. For details, see $t_{CONFIGURATION}$ time in Table 4.21 on page 42.

4.5. ESD Performance

Refer to the LIFMD Product Family Qualification Summary for complete qualification data, including ESD performance.

4.6. DC Electrical Characteristics

Over recommended operating conditions.

Table 4.5. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 4, 5]	Input or I/O Leakage	$0 \le V_{IN} \le V_{CCIO}$	–10	—	+10	µA
I_{PU}[4]	Internal Pull-Up Current	V_{CCIO} = 1.8 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	–3	—	–31	µA
		V_{CCIO} = 2.5 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	–8	—	–72	µA
		V_{CCIO} = 3.3 V between $0 \le V_{IN} \le 0.65 * V_{CCIO}$	–11	—	–128	µA
C_1[2]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pF
C_2[2]	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.2 V, V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pF
C_3[2]	MIPI D-PHY High Speed I/O Capacitance	V_{CCIO} = 2.5V,V_{CC} = 1.2V, V_{CC*_DPHY} = 1.2V , V_{IO} = 0 to V_{IH} (MAX)	—	5	—	pF
V_{HYST}[3]	Hysteresis for Single-Ended Inputs	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = 1.2 V, V_{IO} = 0 to V_{IH} (MAX)	—	200	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tristated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A = 25 °C, f = 1.0 MHz.
3. Hysteresis is not available for V_{CCIO} = 1.2 V.
4. Weak pull-up setting. Programmable pull-up resistors on Bank 0 will see higher current. Refer to CrossLink sysI/O Usage Guide (FPGA-TN-02016) for details on programmable pull-up resistors.
5. Input pins are clamped to V_{CCIO} and GND by a diode. When input is higher than V_{CCIO}, or lower than GND, the Input Leakage current will be higher than the I_{IL} and I_{IH}.

4.7. CrossLink Supply Current

Over recommended operating conditions.

Table 4.6. CrossLink Supply Current

Symbol	Parameter	Typ	Unit
Normal Operation [1]			
I_{CC}	Vcc Power Supply Current	7	mA
I_{CCPLL}	PLL Power Supply Current	50	µA
I_{CCAUX}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	3	mA
I_{CCIOx}	Bank x Power Supply Current (per Bank)	60	µA
I_{CCA_DPHYx}	V_{CCA_DPHYx} Power Supply Current	8.5	mA
I_{CCPLL_DPHYx}	V_{CCPLL_DPHYx} Power Supply Current	1.5	mA
I_{CCMLL_DPHYx}	V_{CCA_DPHY1} & V_{CCPLL_DPHY1} Power Supply Operation Current for WLCSP36 Package	10	mA
Standby Current[2]			
I_{CC_STDBY}	Vcc Power Supply Standby Current	4	mA
I_{CCPLL_STDBY}	PLL Power Supply Standby Current	10	µA
I_{CCAUX_STDBY}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Standby Current	0.2	mA
I_{CCIOx_STDBY}	Bank Power Supply Standby Current (per Bank)	6	µA
$I_{CCA\_DPHYx\_STDBY}$	V_{CCA_DPHYx} Power Supply Standby Current	6	µA
$I_{CCPLL\_DPHYx\_STDBY}$	V_{CCPLL_DPHYx} Power Supply Standby Current	4	µA
$I_{CCMLL\_DPHYx\_STDBY}$	V_{CCA_DPHY1} & V_{CCPLL_DPHY1} Power Supply Static Current for WLCSP36 Package	10	µA
Sleep/Power Down Mode Current [3]			
I_{CC_SLEEP}	Vcc Power Supply Sleep Current	0.2	mA
I_{CCPLL_SLEEP}	PLL Power Supply Current	10	µA
I_{CCAUX_SLEEP}	Auxiliary Power Supply Current for Bank 1, 2 and NVCM Programming Supply Current	20	µA
I_{CCIOx_SLEEP}	Bank Power Supply Current (per Bank)	6	µA
$I_{CCA\_DPHY\_SLEEP}$	V_{CCA_DPHYx} Power Supply Sleep Current	6	µA
$I_{CCPLL\_DPHY\_SLEEP}$	V_{CCPLL_DPHYx} Power Supply Sleep Current	4	µA
$I_{CCAMLL\_DPHYx\_SLEEP}$	V_{CCA_DPHY1} & V_{CCPLL_DPHY1} Power Supply Static Current for WLCSP36 Package	10	µA

Notes:

1. **Normal Operation**
   2:1 MIPI CSI-2 Image Sensor Aggregator Bridge design under the following conditions:
   a. T_J = 25 °C, all power supplies at nominal voltages.
   b. Typical processed device in csfBGA81 package.
   c. To determine power for all other applications and operating conditions, use Power Calculator in Lattice Diamond design software
2. **Standby Operation**
   A typically processed device in csfBGA81 package with blank pattern programmed, under the following conditions:
   a. All outputs are tri-stated, all inputs are held at either V_{CCIO}, or GND.
   b. All clock inputs are at 0 MHz.
   c. T_J = 25 °C, all power supplies at nominal voltages.
   d. No pull-ups on I/O.
3. **Sleep/Power Down Mode**
   2:1 MIPI CSI-2 Image Sensor Aggregator Bridge design under the following conditions:
   a. Design is put into Sleep/Power Down Mode with user logic powers down D-PHY, and enters into Sleep Mode in PMU.
   b. T_J = 25 °C, all power supplies at nominal voltages.
   c. Typical processed device in csfBGA81 package.
4. **For ucfBGA64 package**
   a. V_{CCA_DPHY0} and V_{CCA_DPHY1} are tied together as V_{CCA_DPHYx}.
   b. V_{CCPLL_DPHY0} and V_{CCPLL_DPHY1} are tied together as V_{CCPLL_DPHYx}.

5. **For WLCS36 package**
   a. V_{CCGPLL} and V_{CCIO1} (Bank 1) are tied together to V_{CC}.
   b. V_{CCPLL_DPHY1} and V_{CCA_DPHY1} are tied together as V_{CCMU_DPHY1}.
6. To determine the CrossLink start-up peak current, use the Power Calculator tool in the Lattice Diamond design software.

4.8. Power Management Unit (PMU) Timing

Table 4.7. PMU Timing*

Symbol	Parameter	Device	Max	Unit
$t_{PMUWAKE}$	Time for PMU to wake from Sleep mode	All Devices	0.5	ms

***Note**: For details on PMU usage, refer to Power Management and Calculation for CrossLink Devices (FPGA-TN-02018).

4.9. sysI/O Recommended Operating Conditions

Table 4.8. sysI/O Recommended Operating Conditions[1]

Standard	V_{CCIO}		
	Min	Typ	Max
LVCMOS33/LVTTL33	3.135	3.30	3.465
LVCMOS25	2.375	2.50	2.625
LVCMOS18	1.710	1.80	1.890
LVCMOS12 (Output only) [2]	1.140	1.20	1.260
subLVDS (Input only)	1.710	1.80	1.890
	2.375	2.50	2.625
	3.135	3.30	3.465
SLVS200 (Input only) [3]	1.140	1.20	1.260
	1.710	1.80	1.890
	2.375	2.50	2.625
	3.135	3.30	3.465
LVDS (Input only)	1.710	1.80	1.890
	2.375	2.50	2.625
	3.135	3.30	3.465
LVDS (Output only)	2.375	2.50	2.625
MIPI (Input only)	1.140	1.20	1.260

Notes:
1. For input voltage compatibility, refer to CrossLink sysI/O Usage Guide (FPGA-TN-02016).
2. For VCCIO1 and VCCIO2 only.
3. For SLVS200/MIPI interface I/O placement, see the Programmable I/O Banks section.

4.10. sysI/O Single-Ended DC Electrical Characteristics

Table 4.9. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}		V_{OL} Max (V)	V_{OH} Min (V)	I_{OL} (mA)	I_{OH} (mA)
	Min (V)	Max (V)	Min (V)	Max (V)				
LVCMOS33/ LVTTL33	–0.3	0.8	2.0	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	8	–8
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS25	–0.3	0.7	1.7	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	6	–6
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS18	–0.3	0.35 V_{CCIO}	0.65 V_{CCIO}	V_{CCIO}+0.2	0.40	V_{CCIO} – 0.4	4	–4
					0.20	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS12 (Output only)	—	—	—	—	0.40	V_{CCIO} – 0.4	2	–2
					0.20	V_{CCIO} – 0.2	0.1	–0.1

4.11. sysI/O Differential Electrical Characteristics

4.11.1. LVDS/subLVDS/SLVS200

Over recommended operating conditions.

Table 4.10. LVDS/subLVDS1/SLVS200 [1, 2]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{INP}, V_{INN}	Input Voltage	—	0.00	—	2.40	V
V_{CM}	Input Common Mode Voltage	Half the sum of the two inputs	0.05	—	2.35	V
$V_{THD(LVDS)}$	Differential Input Threshold	$\|V_{INP} - V_{INN}\|$	100	—	—	mV
$V_{THD(subLVDS)}$	Differential Input Threshold	$\|V_{INP} - V_{INN}\|$	90	—	—	mV
$V_{THD(SLVS200)}$	Differential Input Threshold	$\|V_{INP} - V_{INN}\|$	70	—	—	mV
I_{IN}	Input Current	Normal Mode	–10	—	10	µA
		Standby Mode	–10	—	10	µA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ω	—	1.43	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ω	0.90	1.08	—	V
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between High and Low	—	—	—	50	mV
V_{OS}	Output Voltage Offset (Common Mode Voltage)	$(V_{OP} + V_{OM})/2$, RT = 100 Ω	1.125	1.250	1.375	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{SAB}	Output Short Circuit Current	V_{OD} = 0 V driver outputs shorted to each other	—	—	12	mA

Notes:

1. Inputs only for subLVDS and SLVS200.
2. For SLVS200/MIPI interface I/O placement, see the Programmable I/O Banks section.

4.11.2. Hardened MIPI D-PHY I/Os

Table 4.11. MIPI D-PHY

Symbol	Description	Min	Typ	Max	Unit
Receiver					
High Speed					
V_{CMRX}	Common-Mode Voltage HS Receive Mode	70	—	330	mV
V_{IDTH}	Differential Input High Threshold	—	—	70	mV
V_{IDTL}	Differential Input Low Threshold	−70	—	—	mV
V_{IHHS}	Single-ended input High Voltage	—	—	460	mV
V_{ILHS}	Single-ended Input Low Voltage	−40	—	—	mV
$V_{TERM-EN}$	Single-ended Threshold for HS Termination Enable	—	—	450	mV
Z_{ID}	Differential Input Impedance	80	100	125	Ω
Low Power					
V_{IH}	Logic 1 Input Voltage	880	—	—	mV
V_{IL}	Logic 0 Input Voltage, not in ULP State	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 Input Voltage, in ULP State	—	—	300	mV
V_{HYST}	Input Hysteresis	25	—	—	mV
Transmitter					
High Speed					
V_{CMTX}	HS Transmit Static Common Mode Voltage	150	200	250	mV
V_{OD}	HS Transmit Differential Voltage	140	200	270	mV
V_{OHHS}	HS Single-ended Output High Voltage	—	—	360	mV
Z_{OS}	Single-ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single-ended Output Impedance Mismatch	—	—	10	%
Low Power					
V_{OH}	Output High Voltage	1.1	1.2	1.3	V
V_{OL}	Output Low Voltage	−50	—	50	mV
Z_{OLP}	Output Impedance in LP Mode	110	—	—	Ω

4.12. CrossLink Maximum General Purpose I/O Buffer Speed

Over recommended operating conditions.

Table 4.12. CrossLink Maximum I/O Buffer Speed

Buffer	Description	Max	Unit
Maximum Input Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages	600	MHz
	LVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
subLVDS	subLVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages	600	MHz
	subLVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
MIPI D-PHY (HS)[6]	MIPI D-PHY, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages	600	MHz
	MIPI D-PHY, WLCSP36 package	500	MHz
MIPI D-PHY (LP)	MIPI D-PHY, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages	5	MHz
	MIPI D-PHY, WLCSP36 package	5	MHz
SLVS200	SLVS200, VCCIO=2.5 V, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages	600	MHz
	SLVS200, VCCIO=2.5 V, WLCSP36 package	500	MHz
LVCMOS33/LVTTL33	LVCMOS/LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVCMOS25D	Differential LVCMOS, V_{CCIO} = 2.5 V	300	MHz
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	300	MHz
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	155	MHz
Maximum Output Frequency			
LVDS25	LVDS, V_{CCIO} = 2.5 V, csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 packages	600	MHz
	LVDS, V_{CCIO} = 2.5 V, WLCSP36 package	500	MHz
LVCMOS33/LVTTL33	LVCMOS/LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVTTL33D	Differential LVTTL, V_{CCIO} = 3.3 V	300	MHz
LVCMOS33D	Differential LVCMOS, 3.3 V	300	MHz
LVCMOS25	LVCMOS, 2.5 V	300	MHz
LVCMOS25D	Differential LVCMOS, 2.5 V	300	MHz
LVCMOS18	LVCMOS, 1.8 V	155	MHz
LVCMOS12	LVCMOS, $V_{CCIO1/2}$ = 1.2 V	70	MHz

Notes:

1. These maximum speeds are characterized but not tested on every device.
2. Maximum I/O speed for differential output standards emulated with resistors depends on the layout.
3. LVCMOS timing is measured with the load specified in Table 4.22.
4. Actual system operation may vary depending on user logic implementation.
5. Maximum data rate equals two times the clock rate when utilizing DDR.
6. This is the maximum MIPI D-PHY input rate on the programmable I/O banks 1 and 2. The hardened MIPI D-PHY input and output rates are described in Hardened MIPI D-PHY Performance section. For SLVS200/MIPI interface I/O placement, see the Programmable I/O Banks section.
7. To ensure the MIPI Rx interface is implemented optimally in the FPGA fabric with the Programmable I/Os, follow the guidelines of assigning I/Os to the bank for the MIPI Rx inputs: When an SLVS200/MIPI Rx interface is placed in Bank 1 or 2, do not place LVCMOS outputs on both Banks 1 and 2.

4.13. CrossLink External Switching Characteristics

Table 4.13. CrossLink External Switching Characteristics [4, 5]

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Clocks					
Primary Clock					
f_{MAX_PRI}	Frequency for Primary Clock Tree	—	—	150	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	—	0.8	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Clock	—	—	450	ps
Edge Clock					
f_{MAX_EDGE}	Frequency for Edge Clock Tree	—	—	600	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	—	0.783	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within a Bank	—	—	120	ps
Generic SDR Interface [1]					
General Purpose I/O Pin Parameters Using Clock Tree Without PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	6.0	ns
t_{SU}	Clock to Data Setup – PIO Input	—	–0.90	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.82	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	With data input delay for hold time = 0	1.25	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	With data input delay for hold time = 0	0	—	ns
General Purpose I/O Pin Parameters Using Clock Tree With PLL					
t_{CO}	Clock to Output – PIO Input Register	—	—	5.2	ns
t_{SU}	Clock to Data Setup – PIO Input	—	0.20	—	ns
t_{HD}	Clock to Data Hold – PIO Input Register	—	1.01	—	ns
t_{SU_DELAY}	Clock to Data Setup – PIO Input Register with Input Delay for zero t_{HD}	With data input delay for hold time = 0	1.70	—	ns
t_{HD_DELAY}	Clock to Data Hold – PIO Input Register with Input Delay for zero t_{HD}	With data input delay for hold time = 0	0	—	ns
Generic DDR Interfaces [2]					
Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Centered at General Purpose Pins (GDDRX8_RX/TX.ECLK.Centered or GDDRX4_RX/TX.ECLK.Centered or GDDRX2_RX/TX.ECLK.Centered)					
$t_{SU\_GDDRX2\_4\_8\_CENTERED}$	Input Data Set-Up Before CLK Rising and Falling edges	—	0.167	—	ns
$t_{HD\_GDDRX2\_4\_8\_CENTERED}$	Input Data Hold After CLK Rising and Falling edges	—	0.167	—	ns
$t_{DVB\_GDDRX2\_4\_8\_CENTERED}$	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s[6]	0.297	—	ns
		Other Data Rates[6]	–0.120	—	ns+1/2UI
$t_{DVA\_GDDRX2\_4\_8\_CENTERED}$	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 1.2 Gb/s[6]	0.297	—	ns
		Other Data Rates[6]	–0.120	—	ns+1/2UI
$f_{MAX\_GDDRX2\_4\_8\_CENTERED}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 GDDRX2	—	300	MHz
		csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 GDDRX4 and GDDRX8	—	600	MHz
		WLCSP36 GDDRX2	—	250	MHz

Table 4.13. CrossLink External Switching Characteristics [4, 5](*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDR Interfaces [2]					
Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Centered at General Purpose Pins (GDDRX8_RX/TX.ECLK.Centered or GDDRX4_RX/TX.ECLK.Centered or GDDRX2_RX/TX.ECLK.Centered)					
		WLCSP36 GDDRX4 and GDDRX8	—	500	MHz
Generic DDRX1 I/O with Clock and Data Centered at General Purpose Pins (GDDRX1_RX/TX.SCLK.Centered)					
$t_{SU\_GDDRX1\_CENTERED}$	Input Data Set-Up Before CLK Rising and Falling edges	—	0.917	—	ns
$t_{HD\_GDDRX1\_CENTERED}$	Input Data Hold After CLK Rising and Falling edges	—	0.917	—	ns
$t_{DVB\_GDDRX1\_CENTERED}$	Output Data Valid Before CLK Output Rising and Falling edges	Data Rate = 300 Mb/s	1.217	—	ns
		Other Data Rates	-0.450	—	ns+1/2UI
$t_{DVA\_GDDRX1\_CENTERED}$	Output Data Valid After CLK Output Rising and Falling edges	Data Rate = 300 Mb/s	1.217	—	ns
		Other Data Rates	-0.450	—	ns+1/2UI
$f_{MAX\_GDDRX1\_CENTERED}$	Frequency for PCLK[3]	—	—	150	MHz
Generic DDRX8 or DDRX4 or DDRX2 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX8_RX/TX.ECLK.Aligned or GDDRX4_RX/TX.ECLK.Aligned or GDDRX2_RX/TX.ECLK.Aligned)					
$t_{SU\_GDDRX2\_4\_8\_ALIGNED}$	Input Data Valid After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s[6]	—	0.188	ns
		Other Data Rates[6]	—	–0.229	ns+1/2UI
$t_{HD\_GDDRX2\_4\_8\_ALIGNED}$	Input Data Hold After CLK Rising and Falling edges	Data Rate = 1.2 Gb/s[6]	0.646	—	ns
		Other Data Rates[6]	0.229	—	ns+1/2UI
$t_{DIA\_GDDRX2\_4\_8\_ALIGNED}$	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.120	ns
$t_{DIB\_GDDRX2\_4\_8\_ALIGNED}$	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.120	ns
$f_{MAX\_GDDRX2\_4\_8\_ALIGNED}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 GDDRX2	—	300	MHz
		csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64 GDDRX4 and GDDRX8	—	600	MHz
		WLCSP36 GDDRX2	—	250	MHz
		WLCSP36 GDDRX4 and GDDRX8	—	500	MHz

Table 4.13. CrossLink External Switching Characteristics [4, 5](*Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDR Interfaces [2]					
Generic DDRX1 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX1_RX/TX.SCLK.Aligned)					
$t_{SU\_GDDRX1\_ALIGNED}$	Input Data Valid After CLK Rising and Falling edges	Data Rate = 300 Mb/s	—	0.750	ns
		Other Data Rates	—	-0.917	ns+1/2UI
$t_{HD\_GDDRX1\_ALIGNED}$	Input Data Hold After CLK Rising and Falling edges	Data Rate = 300 Mb/s	2.583	—	ns
		Other Data Rates	0.916	—	ns+1/2UI
$t_{DIA\_GDDRX1\_ALIGNED}$	Output Data Invalid After CLK Rising and Falling edges Output	—	—	0.450	ns
$t_{DIB\_GDDRX1\_ALIGNED}$	Output Data Invalid Before CLK Output Rising and Falling edges	—	—	0.450	ns
$f_{MAX\_GDDRX1\_ALIGNED}$	Frequency for ECLK[3]	—	—	150	MHz
General Purpose I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing					
$t_{SU\_GDDRX\_MP}$	Input Data Set-Up Before CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	—	UI
		600 Mb/s < Data Rate ≤ 900 Mb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	—	UI
		Data Rate ≤ 600 Mb/s & V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	—	UI
$t_{HD\_GDDRX\_MP}$	Input Data Hold After CLK	900 Mb/s < Data Rate ≤ 1.2 Gb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.200	—	UI
		600 Mb/s < Data Rate ≤ 900 Mb/s & V_{IDTH} = 140 mV V_{IDTL} = -140 mV	0.150	—	UI
		Data Rate ≤ 600 Mb/s & V_{IDTH} = 70 mV V_{IDTL} = -70 mV	0.150	—	UI
$f_{MAX\_GDDRX\_MP}$	Frequency for ECLK[3]	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

Table 4.13. CrossLink External Switching Characteristics [4, 5] *Continued*)

Parameter	Description	Conditions	–6		Unit
			Min	Max	
Generic DDRX71 or DDRX141 Inputs (GDDRX71_RX.ECLK or GDDRX141_RX.ECLK)					
t_{RPBi_DVA}	Input Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.3	UI
		—	—	–0.222	ns+ (i+ 1/2)*UI
t_{RPBi_DVE}	Input Hold Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	0.7	—	UI
		—	0.222	—	ns+ (i+ 1/2)*UI
$f_{MAX\_RX71\_141}$	DDR71/DDR141 ECLK Frequency[3]	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64, WLCSP36	—	450	MHz
Generic DDR Interfaces [2]					
Generic DDRX71 Outputs with Clock and Data Aligned at Pin (GDDRX71_TX.ECLK)					
t_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	—	0.143	ns+i*UI
t_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	—	–0.143	—	ns+i*UI
$t_{TPBi\_skew\_UI}$	Tx skew in UI	—	—	0.15	UI
f_{MAX_TX71}	DDR71 ECLK Frequency[3]	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64	—	525	MHz
		WLCSP36	—	500	MHz
Generic DDRX141 Outputs with Clock and Data Aligned at Pin (GDDRX141_TX.ECLK)					
t_{TPBi_DOV}	Data Output Valid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	—	0.125	ns+i*UI
t_{TPBi_DOI}	Data Output Invalid Bit "i" switching from CLK Rising Edge ("i" = 0 to 6, 0 aligns with CLK)	All Devices	–0.125	—	ns+i*UI
$t_{TPBi\_skew\_UI}$	TX skew in UI	All Devices	—	0.15	UI
f_{MAX_TX141}	DDR141 ECLK Frequency [3]	csfBGA81, ctfBGA80, ckfBGA80, ucfBGA64	—	600	MHz
		WLCSP36	—	500	MHz

Notes:

1. General I/O timing numbers based on LVCMOS 2.5, 0 pF load.
2. Generic DDRX8, DDRX71 and DDRX141 timing numbers based on LVDS I/O.
3. Maximum clock frequencies are tested under best case conditions. System performance may vary upon the user environment.
4. These numbers are generated using best case PLL located.
5. All numbers are generated with the Lattice Diamond design software.
6. Maximum data rate for GDDRX2 mode is 500 Mbps for WLCSP36 package and 600 Mbps for all other packages.

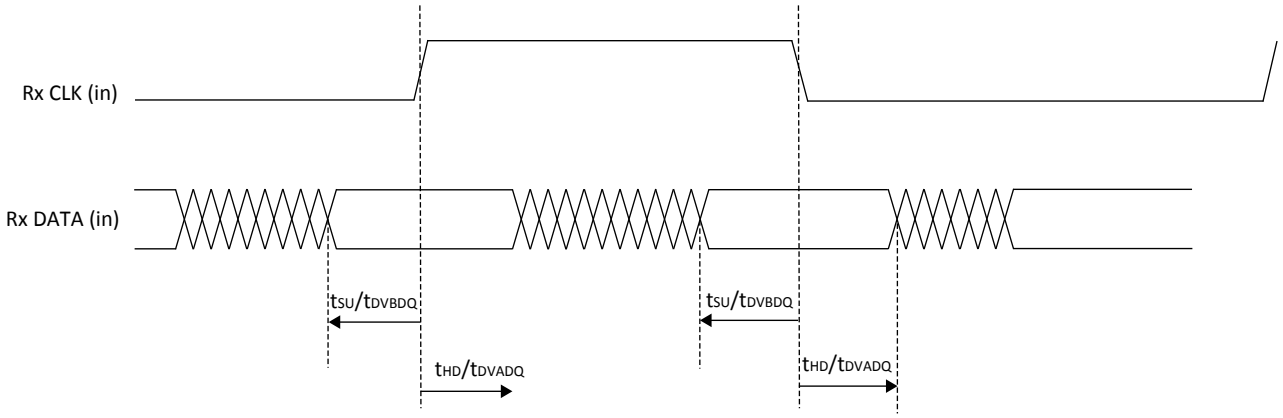


Figure 4.1. Receiver RX.CLK.Centered Waveforms

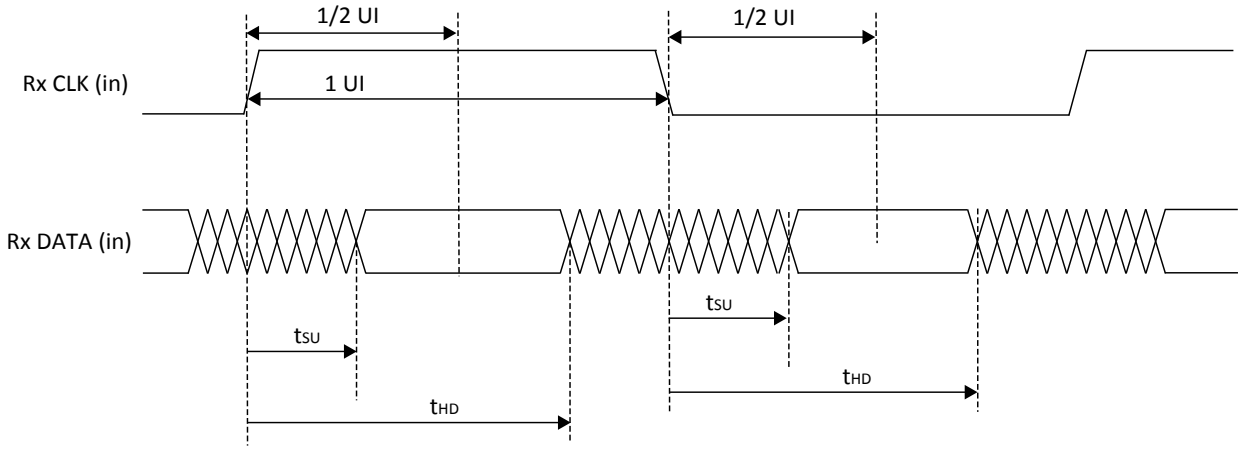


Figure 4.2. Receiver RX.CLK.Aligned Input Waveforms

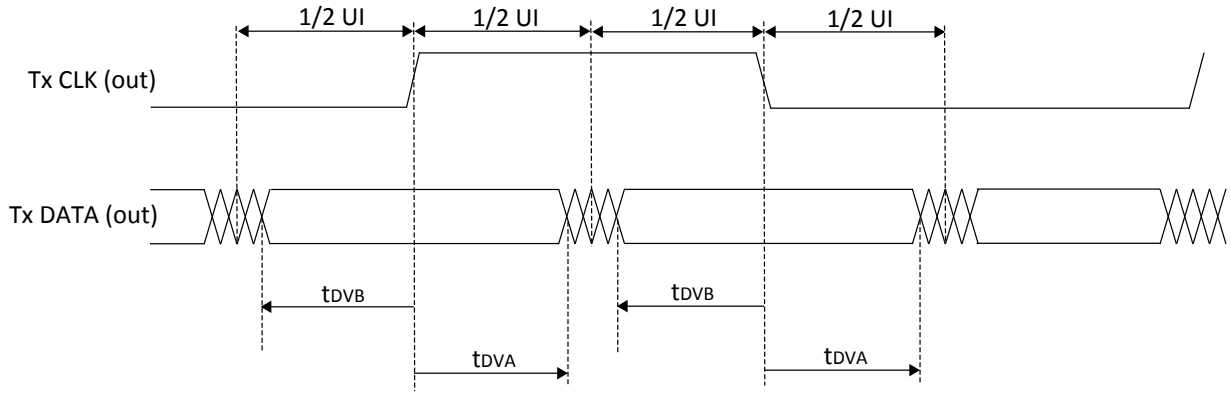


Figure 4.3. Transmit TX.CLK.Centered Output Waveforms

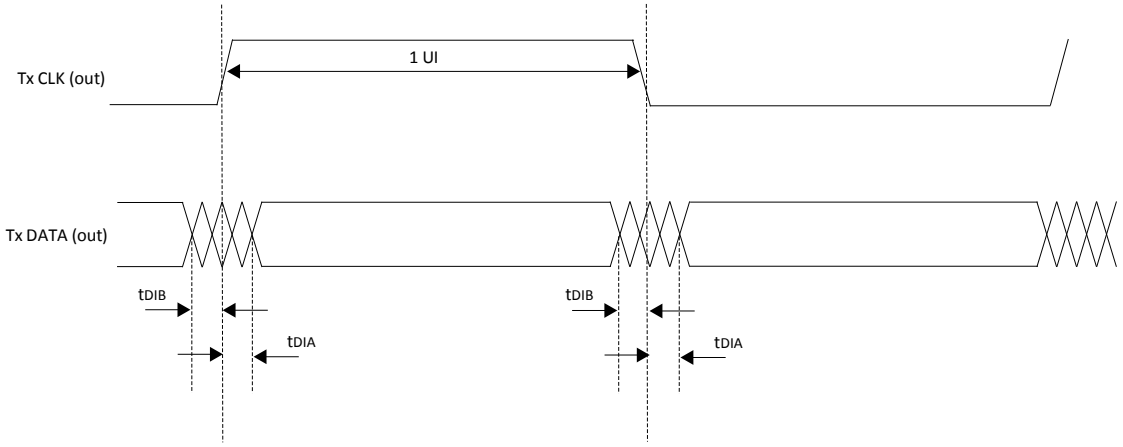


Figure 4.4. Transmit TX.CLK.Aligned Waveforms

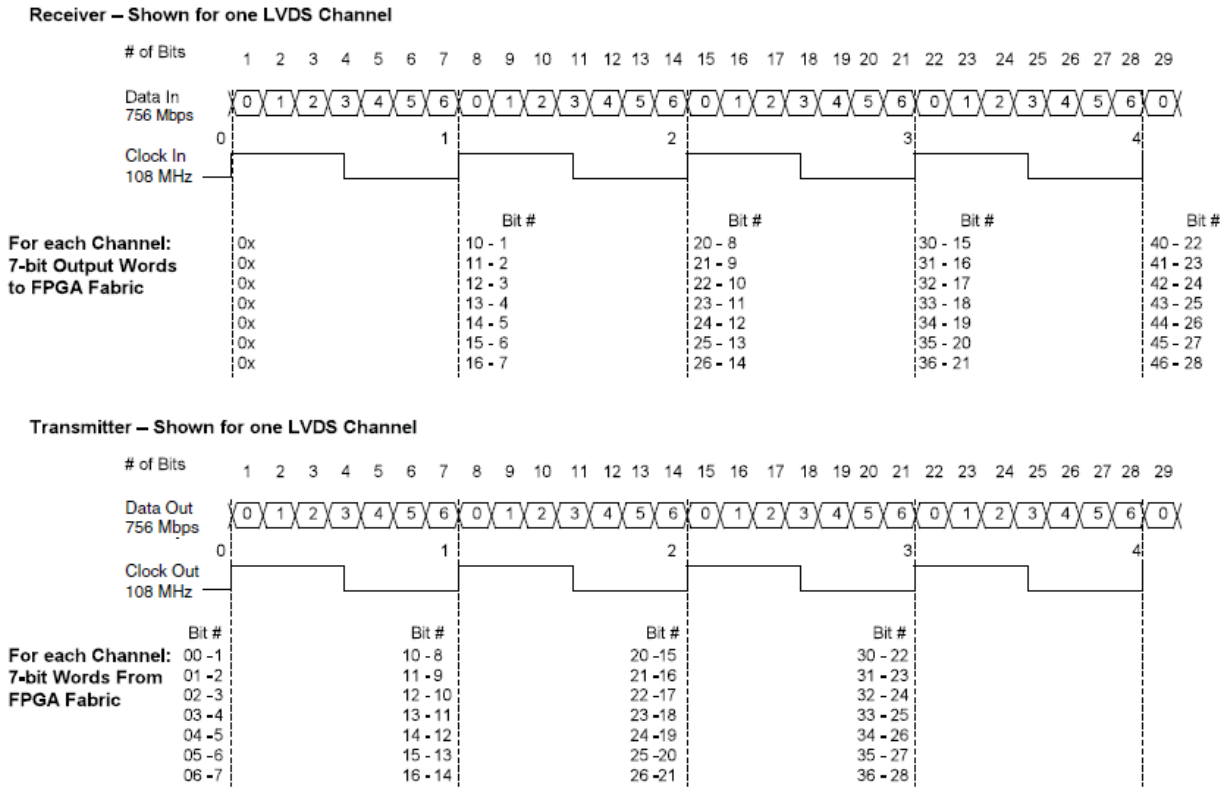


Figure 4.5. DDRX71, DDRX141 Video Timing Waveforms

4.14. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 4.14. sysCLOCK PLL Timing

Parameter	Descriptions	Conditions	Min	Max	Unit
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	10	400	MHz
f_{PD}	Phase Detector Input Clock Frequency	—	10	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS)	—	4.6875	600	MHz
f_{VCO}	PLL VCO Frequency	—	600	1200	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	—	45	55	%
t_{PH}	Output Phase Accuracy	—	–5	5	%
t_{OPJIT}[1]	Output Clock Period Jitter [3]	$f_{OUT} \geq 100$ MHz	—	100	ps p-p
		$f_{OUT} < 100$ MHz	—	0.025	UIPP
	Output Clock Cycle-to-Cycle Jitter [3]	$f_{OUT} \geq 100$ MHz	—	200	ps p-p
		$f_{OUT} < 100$ MHz	—	0.05	UIPP
	Output Clock Phase Jitter	$f_{PD} > 100$ MHz	—	200	ps p-p
		$f_{PD} < 100$ MHz	—	0.05	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	—	400	ps p-p
t_{LOCK}[2]	PLL Lock-in Time	—	—	15	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}	Input Clock Period Jitter	$f_{PD} \geq 20$ MHz	—	500	ps p-p
		$f_{PD} < 20$ MHz	—	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	ns

Notes:

1. Jitter sample is taken over 10,000 samples for Periodic jitter, and 2,000 samples for Cycle-to-Cycle jitter of the primary PLL output with clean reference clock with no additional I/O toggling.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. Period jitter and cycle-to-cycle jitter numbers are guaranteed for $f_{PD} \geq 10$ MHz. For $f_{PD} < 10$ MHz, the jitter numbers may not be met in certain conditions.

4.15. Hardened MIPI D-PHY Performance

Table 4.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s)*

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX8}	Input Data Setup before CLK	0.200	—	UI
t_{HD_MIPIX8}	Input Data Hold after CLK	0.200	—	UI
t_{DVB_MIPIX8}	Output Data Valid before CLK Output	0.300	—	UI
t_{DVA_MIPIX8}	Output Data Valid after CLK Output	0.300	—	UI

***Note**: For WLCSP36 package, the MIPI D-PHY f_{max} is 1200 Mb/s, for other packages, f_{max} is 1500 Mb/s.

Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.200	—	UI
t_{HD_MIPIX4}	Input Data Hold after CLK	0.200	—	UI
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.300	—	UI
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.300	—	UI

Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s)

Parameter	Description	Min	Max	Unit
t_{SU_MIPIX4}	Input Data Setup before CLK	0.150	—	UI
t_{HD_MIPIX4}	Input Data Hold after CLK	0.150	—	UI
t_{DVB_MIPIX4}	Output Data Valid before CLK Output	0.350	—	UI
t_{DVA_MIPIX4}	Output Data Valid after CLK Output	0.350	—	UI

4.16. Internal Oscillators (HFOSC, LFOSC)

Table 4.18. Internal Oscillators

Parameter	Parameter Description	Min	Typ	Max	Unit
f_{CLKHF}	HFOSC CLKK Clock Frequency	43.2	48	52.8	MHz
f_{CLKLF}	LFOSC CLKK Clock Frequency	9	10	11	kHz
DCH_{CLKHF}	HFOSC Duty Cycle (Clock High Period)	45	50	55	%
DCH_{CLKLF}	LFOSC Duty Cycle (Clock High Period)	45	50	55	%

4.17. User I²C

Table 4.19. User I²C [1]

Symbol	Parameter	STD Mode			FAST Mode			FAST Mode Plus[2]			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{scl}	SCL Clock Frequency	—	—	100	—	—	400	—	—	1000[2]	kHz
T_{DELAY}	Optional delay through delay block	—	62	—	—	62	—	—	62	—	ns

Notes:
1. Refer to the I²C Specification for timing requirements.
2. Fast Mode Plus maximum speed may be achieved by using external pull up resistor on I²C bus. Internal pull up may not be sufficient to support the maximum speed.

4.18. CrossLink sysCONFIG Port Timing Specifications

Over recommended operating conditions.

Table 4.20. CrossLink sysCONFIG Port Timing Specifications

Symbol	Parameter	Min	Max	Unit
All Configuration Mode				
t_{PRGM}	Minimum CRESETB LOW pulse width required to restart configuration (from falling edge to rising edge)	145	—	ns
Slave SPI[1]				
f_{CCLK}	SPI_SCK Input Clock Frequency	—	110	MHz
t_{STSU}	MOSI Setup Time	0.5	—	ns
t_{STH}	MOSI Hold Time	2.0	—	ns
t_{STCO}	SPI_SCK Falling Edge to Valid MISO Output	—	13.3	ns
t_{SCS}	Chip Select HIGH Time	25	—	ns
t_{SCSS}	Chip Select Setup Time	0.5	—	ns
t_{SCSH}	Chip Select Hold Time	0.5	—	ns
Master SPI				
f_{CCLK}	MCK Output Clock Frequency	—	52.8	MHz
I²C [2]				
f_{MAX}	Maximum SCL Clock Frequency (Fast-Mode Plus)	—	1	MHz

Notes:

1. Refer to CrossLink Programming and Configuration Usage Guide (FPGA-TN-02014), for timing requirements to enable CrossLink SSPI Mode.
2. Refer to the I2C specification for timing requirements when configuring with I²C port.

4.19. SRAM Configuration Time from NVCM

Over recommended operating conditions.

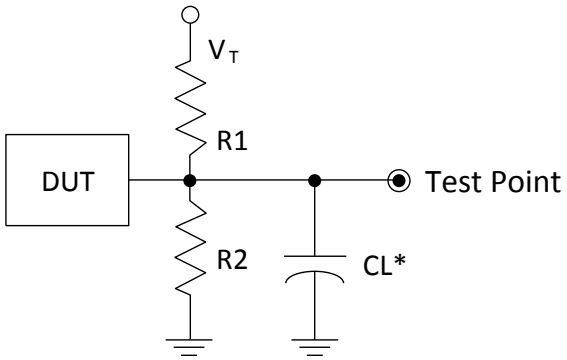
Table 4.21. SRAM Configuration Time from NVCM

Symbol	Parameter	Typ	Unit
$T_{CONFIGURATION}$	POR/CRESET_B to Device I/O Active*	83	ms

***Note**: Before and during configuration, the I/Os are held in tristate with weak internal pullups enabled. I/Os are released to user functionality when the device has finished configuration.

4.20. Switching Test Conditions

Figure 4.6 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.22.



*CL Includes Test Fixture and Probe Capacitance

Figure 4.6. Output Test Load, LVTTL and LVCMOS Standards

Table 4.22. Test Fixture Required Components, Non-Terminated Interfaces*

Test Condition	R_1	R_2	C_L	Timing Ref.	V_T
LVTTL and other LVCMOS settings (L ≥ H, H ≥ L)	∞	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
				LVCMOS 2.5 = $V_{CCIO}/2$	—
				LVCMOS 1.8 = $V_{CCIO}/2$	—
				LVCMOS 1.2 = $V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ H)	∞	1 MΩ	0 pF	$V_{CCIO}/2$	—
LVCMOS 2.5 I/O (Z ≥ L)	1 MΩ	∞	0 pF	$V_{CCIO}/2$	V_{CCIO}
LVCMOS 2.5 I/O (H ≥ Z)	∞	100	0 pF	$V_{OH} - 0.10$	—
LVCMOS 2.5 I/O (L ≥ Z)	100	∞	0 pF	$V_{OL} + 0.10$	V_{CCIO}

***Note**: Output test conditions for all other interfaces are determined by the respective standards.

5. Pinout Information

The pinout tables below correspond to CrossLink LIF-MD6000 Pinout Version 1.4.

GND pins are referenced as V_{SS} in Lattice Diamond Software.

5.1. WLCSP36 Pinout

Table 5.1. WLCSP36 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	GNDMU_DPHY1	GND	—	—
A2	VCCMU_DPHY1	DPHY1	—	—
A3	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
A4	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
A5	VCCAUX	VCCAUX	—	—
A6	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B3	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	PB16D	2	PCLKC2_1	Comp_OF_PB16C
B6	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
C1	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
C2	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
C3	PB52	0	SPI_SS/CSN/SCL	—
C4	VCC	VCC	—	—
C5	PB16C	2	PCLKT2_1	True_OF_PB16D
C6	GND	GND	—	—
D1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
D2	PB48	0	PCLKT0_1/USER_SCL	—
D3	PB47	0	PCLKT0_0/USER_SDA	—
D4	CRESET_B	0	—	—
D5	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D6	PB6B	2	—	Comp_OF_PB6A
E1	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
E2	VCCIO0	0	—	—
E3	GND	GND	—	—
E4	PB50	0	MOSI	—
E5	PB16A	2	PCLKT2_0	True_OF_PB16B
E6	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F1	PB51	0	MISO	—
F2	PB49	0	PMU_WKUPN/CDONE	—
F3	PB53	0	SPI_SCK/MCK/SDA	—
F4	PB12A	2	GPLLT2_0	True_OF_PB12B
F5	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F6	VCCIO2	2	—	—

5.2. ucfBGA64 Pinout

Table 5.2. ucfBGA64 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
A5	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A6	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
A7	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A8	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
B2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
B3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B4	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B5	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B6	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
B7	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
B8	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
C1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
C2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
C3	PB47	0	PCLKT0_0/USER_SDA	—
C4	VCCPLL_DPHYx	DPHY	—	—
C5	VCCA_DPHYx	DPHY	—	—
C6	GNDA_DPHYx	GND	—	—
C7	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
C8	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
D1	PB34B	1	—	Comp_OF_PB34A
D2	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D3	PB52	0	SPI_SS/CSN/SCL	—
D4	GND	GND	—	—
D5	VCC	VCC	—	—
D6	VCCAUX	VCCAUX	—	—
D7	PB16A	2	PCLKT2_0	True_OF_PB16B
D8	PB12A	2	GPLLT2_0	True_OF_PB12B
E1	PB51	0	MISO	—
E2	CRESET_B	0	—	—
E3	PB48	0	PCLKT0_1/USER_SCL	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—
E7	PB16B	2	PCLKC2_0	Comp_OF_PB16A
E8	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F1	PB53	0	SPI_SCK/MCK/SDA	—
F2	PB50	0	MOSI	—

Table 5.2. ucfBGA64 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F3	VCCIO0	0	—	—
F4	VCCIO1	1	—	—
F5	GND	GND	—	—
F6	VCCIO2	2	—	—
F7	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F8	PB6B	2	—	Comp_OF_PB6A
G1	PB38D	1	—	Comp_OF_PB38C
G2	PB38C	1	—	True_OF_PB38D
G3	PB49	0	PMU_WKUPN/CDONE	—
G4	VCCGPLL	VCCGPLL	—	—
G5	PB29B	1	PCLKC1_0	Comp_OF_PB29A
G6	PB29A	1	PCLKT1_0	True_OF_PB29B
G7	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
G8	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
H1	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
H2	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
H3	PB29C	1	PCLKT1_1	True_OF_PB29D
H4	PB29D	1	PCLKC1_1	Comp_OF_PB29C
H5	PB16D	2	PCLKC2_1	Comp_OF_PB16C
H6	PB16C	2	PCLKT2_1	True_OF_PB16D
H7	PB12D	2	—	Comp_OF_PB12C
H8	PB12C	2	—	True_OF_PB12D

5.3. ctfBGA80/cktBGA80 Pinout

Table 5.3. ctfBGA80/cktBGA80 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
A2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
A3	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A4	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
A5	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
A9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
A10	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
B1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
B2	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B3	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
B4	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
B5	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
B9	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B10	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C1	GND	GND	—	—
C2	GNDA_DPHY1	DPHY1	—	—
C9	GNDA_DPHY0	DPHY0	—	—
C10	GND	GND	—	—
D1	PB48	0	PCLKT0_1/USER_SCL	—
D2	VCCPLL_DPHY1	DPHY1	—	—
D4	VCCA_DPHY1	DPHY1	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GNDPLL_DPHYx	GND	—	—
D7	VCCPLL_DPHY0	DPHY0	—	—
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
D10	PB16B	2	PCLKC2_0	Comp_OF_PB16A
E1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
E2	PB34B	1	—	Comp_OF_PB34A
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCC	VCC	—	—
E7	VCCA_DPHY0	DPHY0	—	—
E9	PB12A	2	GPLLT2_0	True_OF_PB12B
E10	PB12B	2	GPLLC2_0	Comp_OF_PB12A
F1	PB38A	1	—	True_OF_PB38B
F2	PB38B	1	—	Comp_OF_PB38A

Table 5.3. ctfBGA80/cktBGA80 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
F4	VCCIO0	0	—	—
F5	VCCIO1	1	—	—
F6	VCCIO2	2	—	—
F7	VCCIO2	2	—	—
F9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F10	PB6B	2	—	Comp_OF_PB6A
G1	PB50	0	MOSI	—
G2	GND	GND	—	—
G4	VCCIO1	1	—	—
G5	GND	GND	—	—
G6	VCCGPLL	VCCGPLL	—	—
G7	GNDGPLL	GND	—	—
G9	PB2A	2	—	True_OF_PB2B
G10	PB2B	2	—	Comp_OF_PB2A
H1	PB52	0	SPI_SS/CSN/SCL	—
H2	CRESET_B	0	—	—
H9	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
H10	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
J1	PB53	0	SPI_SCK/MCK/SDA	—
J2	PB49	0	PMU_WKUPN/CDONE	—
J3	PB43D	1	—	Comp_OF_PB43C
J4	PB38D	1	—	Comp_OF_PB38C
J5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
J6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
J7	PB29A	1	PCLKT1_0	True_OF_PB29B
J8	PB16D	2	PCLKC2_1	Comp_OF_PB16C
J9	PB6D	2	—	Comp_OF_PB6C
J10	PB6C	2	—	True_OF_PB6D
K1	PB51	0	MISO	—
K2	PB47	0	PCLKT0_0/USER_SDA	—
K3	PB43C	1	—	True_OF_PB43D
K4	PB38C	1	—	True_OF_PB38D
K5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
K6	PB29C	1	PCLKT1_1	True_OF_PB29D
K7	PB29B	1	PCLKC1_0	Comp_OF_PB29A
K8	PB16C	2	PCLKT2_1	True_OF_PB16D
K9	PB12D	2	—	Comp_OF_PB12C
K10	PB12C	2	—	True_OF_PB12D

5.4. csfBGA81 Pinout

Table 5.4. csfBGA81 Pinout

Pin Number	Pin Function	Bank	Dual Function	Differential
A1	DPHY1_CKP	DPHY1	—	True_OF_DPHY1_CKN
A2	DPHY1_CKN	DPHY1	—	Comp_OF_DPHY1_CKP
A3	DPHY1_DP1	DPHY1	—	True_OF_DPHY1_DN1
A4	DPHY1_DP3	DPHY1	—	True_OF_DPHY1_DN3
A5	VCCA_DPHY1	DPHY1	—	—
A6	DPHY0_DN2	DPHY0	—	Comp_OF_DPHY0_DP2
A7	DPHY0_DN0	DPHY0	—	Comp_OF_DPHY0_DP0
A8	DPHY0_CKP	DPHY0	—	True_OF_DPHY0_CKN
A9	DPHY0_CKN	DPHY0	—	Comp_OF_DPHY0_CKP
B1	DPHY1_DP0	DPHY1	—	True_OF_DPHY1_DN0
B2	DPHY1_DN0	DPHY1	—	Comp_OF_DPHY1_DP0
B3	DPHY1_DN1	DPHY1	—	Comp_OF_DPHY1_DP1
B4	DPHY1_DN3	DPHY1	—	Comp_OF_DPHY1_DP3
B5	GNDPLL_DPHYx	GND	—	—
B6	DPHY0_DP2	DPHY0	—	True_OF_DPHY0_DN2
B7	DPHY0_DP0	DPHY0	—	True_OF_DPHY0_DN0
B8	DPHY0_DP1	DPHY0	—	True_OF_DPHY0_DN1
B9	DPHY0_DN1	DPHY0	—	Comp_OF_DPHY0_DP1
C1	DPHY1_DP2	DPHY1	—	True_OF_DPHY1_DN2
C2	DPHY1_DN2	DPHY1	—	Comp_OF_DPHY1_DP2
C3	GNDA_DPHY1	DPHY1	—	—
C4	VCCPLL_DPHY1	DPHY1	—	—
C5	GND	GND	—	—
C6	VCCPLL_DPHY0	DPHY0	—	—
C7	GNDA_DPHY0	DPHY0	—	—
C8	DPHY0_DP3	DPHY0	—	True_OF_DPHY0_DN3
C9	DPHY0_DN3	DPHY0	—	Comp_OF_DPHY0_DP3
D1	PB34A	1	GR_PCLK1_0	True_OF_PB34B
D2	PB34B	1	—	Comp_OF_PB34A
D3	VCCA_DPHY1	DPHY1	—	—
D4	GND	GND	—	—
D5	VCCAUX	VCCAUX	—	—
D6	GND	GND	—	—
D7	VCCA_DPHY0	DPHY0	—	—
D8	PB16B	2	PCLKC2_0	Comp_OF_PB16A
D9	PB16A	2	PCLKT2_0	True_OF_PB16B
E1	PB38A	1	—	True_OF_PB38B
E2	PB38B	1	—	Comp_OF_PB38A
E3	VCC	VCC	—	—
E4	VCC	VCC	—	—
E5	GND	GND	—	—
E6	VCCIO2	2	—	—

Table 5.4 csfBGA81 Pinout *(Continued)*

Pin Number	Pin Function	Bank	Dual Function	Differential
E7	PB12B	2	GPLLC2_0	Comp_OF_PB12A
E8	PB6B	2	—	Comp_OF_PB6A
E9	PB6A	2	GR_PCLK2_0	True_OF_PB6B
F1	PB50	0	MOSI	—
F2	PB48	0	PCLKT0_1/USER_SCL	—
F3	VCCIO1	1	—	—
F4	GND	GND	—	—
F5	GNDGPLL	GND	—	—
F6	VCCIO2	2	—	—
F7	PB12A	2	GPLLT2_0	True_OF_PB12B
F8	PB2B	2	—	Comp_OF_PB2A
F9	PB2A	2	—	True_OF_PB2B
G1	PB52	0	SPI_SS/CSN/SCL	—
G2	CRESET_B	0	—	—
G3	VCCIO0	0	—	—
G4	VCCIO1	1	—	—
G5	VCCGPLL	VCCGPLL	—	—
G6	PB29B	1	PCLKC1_0	Comp_OF_PB29A
G7	PB29A	1	PCLKT1_0	True_OF_PB29B
G8	PB2D	2	MIPI_CLKC2_0	Comp_OF_PB2C
G9	PB2C	2	MIPI_CLKT2_0	True_OF_PB2D
H1	PB53	0	SPI_SCK/MCK/SDA	—
H2	PB49	0	PMU_WKUPN/CDONE	—
H3	PB43D	1	—	Comp_OF_PB43C
H4	PB38D	1	—	Comp_OF_PB38C
H5	PB34D	1	MIPI_CLKC1_0	Comp_OF_PB34C
H6	PB29D	1	PCLKC1_1	Comp_OF_PB29C
H7	PB16D	2	PCLKC2_1	Comp_OF_PB16C
H8	PB6D	2	—	Comp_OF_PB6C
H9	PB6C	2	—	True_OF_PB6D
J1	PB51	0	MISO	—
J2	PB47	0	PCLKT0_0/USER_SDA	—
J3	PB43C	1	—	True_OF_PB43D
J4	PB38C	1	—	True_OF_PB38D
J5	PB34C	1	MIPI_CLKT1_0	True_OF_PB34D
J6	PB29C	1	PCLKT1_1	True_OF_PB29D
J7	PB16C	2	PCLKT2_1	True_OF_PB16D
J8	PB12D	2	—	Comp_OF_PB12C
J9	PB12C	2	—	True_OF_PB12D

5.5. Dual Function Pin Descriptions

The following table describes the dual functions available to certain pins on the CrossLink device. These pins may alternatively be used as general purpose I/O when the described dual function is not enabled.

Table 5.5. Dual Function Pin Descriptions

Signal Name	I/O	Description
General Purpose		
USER_SCL	I/O	User Slave I2C0 clock input and Master I²C0 clock output. Enables PMU wake-up via I2C0.
USER_SDA	I/O	User Slave I2C0 data input and Master I²C0 data output. Enables PMU wakeup via I2C0.
PMU_WKUPN	—	This pin wakes the PMU from sleep mode when toggled low.
Clock Functions		
GPLL2_0[T, C]_IN	I	General Purpose PLL (GPLL) input pads: T = true and C = complement. These pins can be used to input a reference clock directly to the General Purpose PLL. These pins do not provide direct access to the primary clock network.
GR_PCLK[Bank]0	I	These pins provide a short General Routing path to the primary clock network. Refer to CrossLink sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02015) for details.
PCLK[T/C][Bank]_[num]	I/O	General Purpose Primary CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins provide direct access to the primary and edge clock networks.
MIPI_CLK[T/C][Bank]_0	I/O	MIPI D-PHY Reference CLK pads: [T/C] = True/Complement, [Bank] = (0, 1 and 2). These pins can be used to input a reference clock directly to the D-PHY PLLs. These pins do not provide direct access to the primary clock network.
Configuration		
CDONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the startup sequence is in progress. Holding CDONE delays configuration.
SPI_SCK	I	Input Configuration Clock for configuring CrossLink in Slave SPI mode (SSPI).
MCK	O	Output Configuration Clock for configuring CrossLink in Master SPI mode (MSPI).
SPI_SS	I	Input Chip Select for configuring CrossLink in Slave SPI mode (SSPI).
CSN	O	Output Chip Select for configuring CrossLink in Master SPI mode (MSPI).
MOSI	I/O	Data Output when configuring CrossLink in Master SPI mode (MSPI), data input when configuring CrossLink in Slave SPI mode (SSPI).
MISO	I/O	Data Input when configuring CrossLink in Master SPI mode (MSPI), data output when configuring CrossLink in Slave SPI mode (SSPI).
SCL	I/O	Slave I²C clock I/O when configuring CrossLink in I²C mode.
SDA	I/O	Slave I²C data I/O when configuring CrossLink in I²C mode.

5.6. Dedicated Function Pin Descriptions

Table 5.6. Dedicated Function Pin Descriptions

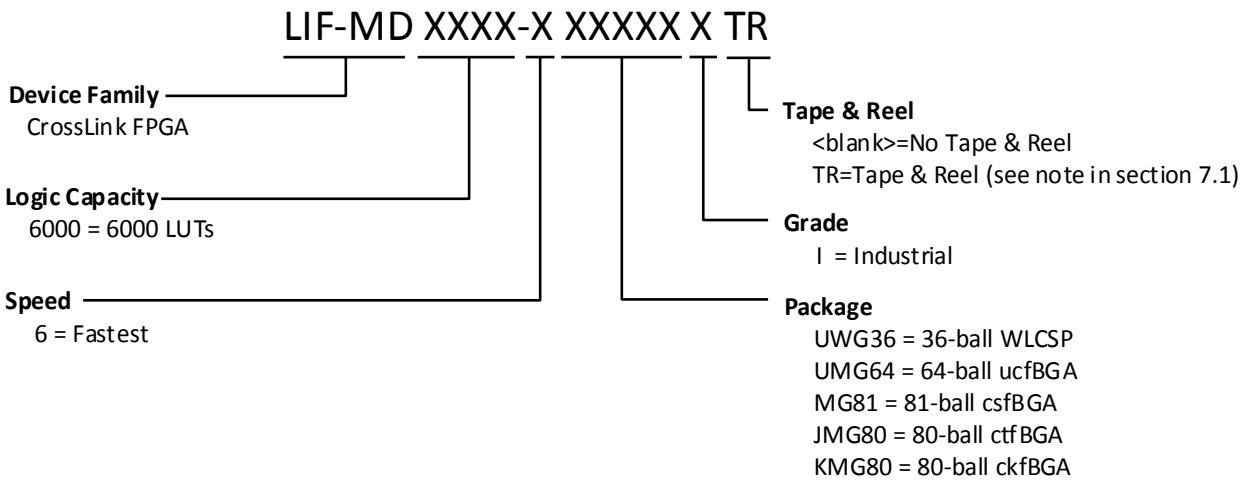
Signal Name	I/O	Description
Configuration		
CRESET_B	I	Configuration Reset, active LOW.
MIPI D-PHY		
DPHY[num]_CK[P/N]	I/O	MIPI D-PHY Clock [num] = D-PHY 0 or 1, P = Positive, N = Negative.
DPHY[num]_D[P/N][lane]	I/O	MIPI D-PHY Data [num] = D-PHY 0 or 1, P = Positive, N = Negative, Lane = data lane in the D-PHY block 0, 1, 2 or 3.

5.7. Pin Information Summary

Table 5.7. Pin Information Summary

Pin Type	CrossLink				
	WLCSP36	ucfBGA64	ctfBGA80	ckfBGA80	csfBGA81
Total General Purpose I/O	17	29	37	37	37
VCC/VCCIOx/VCCAUX/VCCGPLL	4	8	9	9	10
GND	2	3	6	6	6
D-PHY Clock/Data	10	20	20	20	20
D-PHY VCC	1	2	4	4	4
D-PHY GND	1	1	3	3	3
CRESETB	1	1	1	1	1
Total Balls	**36**	**64**	**80**	**80**	**81**
General Purpose I/O per Bank					
Bank 0	7	7	7	7	7
Bank 1	0	10	14	14	14
Bank 2	10	12	16	16	16
Total General Purpose Single Ended I/O	**17**	**29**	**37**	**37**	**37**
Differential I/O Pairs per Bank					
Bank 0	0	0	0	0	0
Bank 1	0	5	7	7	7
Bank 2	5	6	8	8	8
Total General Purpose Differential I/O Pairs	**5**	**11**	**15**	**15**	**15**

6. CrossLink Part Number Description



6.1. Ordering Part Numbers

Industrial*

Part Number	Grade	Package	Pins	Temp.	LUTs (K)
LIF-MD6000-6UWG36ITR	–6	Lead free WLCSP	36	Industrial	5.9
LIF-MD6000-6UMG64I	–6	Lead free ucfBGA	64	Industrial	5.9
LIF-MD6000-6MG81I	–6	Lead free csfBGA	81	Industrial	5.9
LIF-MD6000-6JMG80I	–6	Lead free ctfBGA	80	Industrial	5.9
LIF-MD6000-6KMG80I	-6	Lead free ckfBGA	80	Industrial	5.9

***Note**: UWG36 package is available in shipments of 5000 pieces/reel (TR), 1000 pieces/reel (TR1K), and 50 pieces/reel (TR50 – for samples only).

References

For more information, refer to the following technical notes:

- CrossLink High-Speed I/O Interface (FPGA-TN-02012)
- CrossLink Hardware Checklist (FPGA-TN-02013)
- CrossLink Programming and Configuration Usage Guide (FPGA-TN-02014)
- CrossLink sysCLOCK PLL/DLL Design and Usage Guide (FPGA-TN-02015)
- CrossLink sysI/O Usage Guide (FPGA-TN-02016)
- CrossLink Memory Usage Guide (FPGA-TN-02017)
- Power Management and Calculation for CrossLink Devices (FPGA-TN-02018)
- CrossLink I2C Hardened IP Usage Guide (FPGA-TN-02019)
- Advanced CrossLink I2C Hardened IP Reference Guide (FPGA-TN-02020)

For package information, refer to the following technical notes:

- PCB Layout Recommendations for BGA Packages (TN1074)
- Solder Reflow Guide for Surface Mount Devices (FPGA-TN-12041, previously TN1076)
- Wafer-Level Chip-Scale Package Guide (TN1242)
- Thermal Management
- Package Diagrams

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS): www.jedec.org
- MIPI Standards (D-PHY): www.mipi.org

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
July2018	1.5	• Updated Table 4.1. Absolute Maximum Ratings [1, 2, 3] . Added footnote 4 to V_{CCAUX} parameters. • Updated Table 4.2. Recommended Operating Conditions [1, 2]. Added footnote 3 to V_{CCAUX} parameters. • Updated Table 4.13. CrossLink External Switching Characteristics [4, 5]. Revised $t_{SU\_GDDRX\_MP}$ and $t_{HD\_GDDRX\_MP}$ conditions under I/O MIPI D-PHY Rx with 1:8 or 1:16 Gearing.

February 2018	1.4	• Removed Application Examples section and its associated references throughout the document
		• Updated the Architecture Overview section (general update)
		  • Reordered the list of features supported by the hard D-PHY quads
		  • Added Figure 3.3 to Figure 3.6 to the MIPI D-PHY Blocks section
		  • Updated the Programmable I/O Banks section
		  • Added Bank 0 list of features
		  • Added Table 3.1, Table 3.2, Table 3.3, and Table 3.4
		  • Updated Programmable FPGA Fabric section
		  • Removed FPGA Fabric Overview header
		  • Added PFU Blocks section
		  • Added Slice section
		  • Moved Clocking Overview as a new Clocking Structure (heading 2) section and added contents
		  • Moved Embedded Block RAM Overview as a new (heading 2) section and added contents
		  • Removed System Resources section
		  • Moved Power Management Unit section under Embedded Block RAM Overview
		  • Removed Device Configuration section
		  • Moved User I2C IP as a new (heading 2) section
		  • Added Programming and Configuration section
		• Updated CrossLink Maximum General Purpose I/O Buffer Speed section. Changed LVTTL33/LVCMOS33 to LVCMOS33/LVTTL33
		• Updated CrossLink External Switching Characteristics section (general update)
		• Placed captions to pinout tables

Date	Version	Change Summary

November 2017	1.3	• Added 80-ball ckfBGA (49 mm^2) package in Features section
		• Updated note in Table 2.1, Table 2.2, Table 2.3, Table 2.4, Table 2.5, Table 2.6, Table 2.7, Table 2.8, and Table 2.9 Added 80 ckfBGA (7.0 x 7.0 mm^2, 1 mm) package to Table 2.1. CrossLink Feature Summary
		• Updated System Resources section
		  • Removed LVCMOS12 (Outputs Only) from CMOS GPIO (Bank 0) section
		  • Added information in Device Configuration section
		• Updated Table 4.1. Absolute Maximum Ratings [1, 2, 3]
		  • Changed symbol from VCCPLL to VCCGPLL
		  • Removed VCC_DPHY symbol
		• Updated Table 4.2. Recommended Operating Conditions [1, 2]
		  • Revised symbols to VCCGPLL.and VCCIO0
		  • Added row of VCCIO1/2 symbol
		  • Removed row of VCC_DPHYx symbol
		  • Removed VCC_DPHY1 from V_{CCMU_DPHY1} parameter description
		• Added notes to Table 4.8. sysI/O Recommended Operating Conditions[1] and Table 4.20. CrossLink sysCONFIG Port Timing Specifications
		• Updated link to the LIFMD Product Family Qualification Summary reference in the ESD Performance section
		• Removed V_{CCIO} = 1.2 V between 0 ⩽ V_{IN} ⩽ 0.65 * V_{CCIO} condition from Table 4.5. DC Electrical Characteristics
		• Updated Table 4.6. CrossLink Supply Current
		  • Updated ICCMLL_DPHYx, ICCMLL_DPHYx_STDBY, and ICCPLL_DPHY_SLEEP parameters
		  • Moved ICCA_DPHY_SLEEP and updated parameter
		  • Updated ICCAMLL_DPHYx_SLEEP parameter and unit
		  • Updated footnote 4-a, 4-b, and 5-b
		• Updated Table 4.12. CrossLink Maximum I/O Buffer Speed
		  • Added ckfBGA80 package in descriptions
		  • Changed LVTTL33/LVCMOS to LVTTL33/LVCMOS33
		  • Changed V_{CCIO} to $V_{CCIO1/2}$ in LVCMOS12 description
		• Updated the CrossLink External Switching Characteristics section and Table 4.13. CrossLink External Switching Characteristics [4, 5]
		  • Removed “Over recommended commercial operating conditions.”
		  • General update of information under Generic DDR Interfaces2 including the addition of “Generic DDRX1 I/O with Clock and Data Centered at General Purpose Pins (GDDRX1_RX/TX.ECLK.Centered)” and “Generic DDRX1 I/O with Clock and Data Aligned at General Purpose Pins (GDDRX1_RX/TX.ECLK.Aligned” rows
		  • Added ckfBGA80 package in specific conditions
		• Changed $T_{REFRESH}$ to $T_{CONFIGURATION}$ in Table 4.21. SRAM Configuration Time from NVCM
		• Updated Pinout Information section
		  • Updated section introduction
		  • Updated WLCSP36 Pinout. Changed C4 bank to VCC
		  • Updated section to ctfBGA80/cktBGA80 Pinout and revised pin function of C1, C2, C9, C10, D6, E5, G2, G5, and G7
		  • Updated pin function of B5 in csfBGA81 Pinout
		  • Updated Pin Information Summary section
		• Updated CrossLink Part Number Description section
		• Added LIF-MD6000-6KMG80I part number to Ordering Part Numbers section
		• Update reference to the Solder Reflow Guide for Surface Mount Devices document in References section

Date	Version	Change Summary
June 2017	1.2	• Updated Fabric Resources Used in Table 2.1, Table 2.2, Table 2.3, Table 2.4, Table 2.5, Table 2.6, and Table 2.9 • Updated Figure 3.1. CrossLink Device Block Diagram • Added row of V_{CCAUX} for 3.3 V in Table 4.1. Absolute Maximum Ratings [1, 2, 3] and Table 4.2. Recommended Operating Conditions [1, 2] • Added row of C_3 to Table 4.5. DC Electrical Characteristics • Added rows of I_{CCAMLL_DPHYx}, $I_{CCAMLL\_DPHYx\_STDBY}$, and $I_{CCAMLL\_DPHYx\_SLEEP}$ to Table 4.6. CrossLink Supply Current • Updated Max value in Table 4.7. PMU • Updated values of subLVDS (Input only) and SLVS200 (Input only), and added row of LVDS (Input only) to Table 4.8. sysI/O Recommended Operating Conditions[1] • Updated Table 5.10. LVDS/subLVDS1/SLVS200 • Updated parameter descriptions in Table 4.11. MIPI D-PHY • Added row of MIPI D-PHY (LP Mode), and updated Max values of subLVDS and SLVS200 in Table 4.12. CrossLink Maximum I/O Buffer Speed • Updated conditions in Table 4.13. CrossLink External Switching Characteristics [4, 5] • Added rows of f_{PD} and f_{VCO} to Table 4.14. sysCLOCK PLL Timing • Updated values in Table 4.15. 1500 Mb/s MIPI_DPHY_X8_RX/TX Timing Table (1500 Mb/s > MIPI D-PHY Data Rate > 1200 Mb/s), Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s) and Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s) • Updated Typ values of DCH_{CLKHF} and DCH_{CLKLF} in Table 4.18. Internal Oscillators • Added row of T_{DELAY} to Table 4.19. User I^2C [1] • Updated Min value of t_{SCS} in Table 4.20. CrossLink sysCONFIG Port Timing Specifications • Updated symbol and parameter in Table 4.21. SRAM Configuration Time from NVCM • Included version number in Pinout Information
March 2017	1.1	Updated I/O placements on banks containing MIPI interface in Programmable I/O Banks section. Updated DC and Switching Characteristics section: • Updated Table 4.4. Power-On-Reset Voltage Levels 1, 3, 4, added row of V_{PORDN} • Added Note 5 to Table 4.5. DC Electrical Characteristics • Updated Table 4.6. CrossLink Supply Current, added notes • Updated max values of V_{THD} and $V_{THD(subLVDS)}$ in Table 4.10. LVDS/subLVDS1/SLVS200 [1, 2] • Maximum input frequency values of subLVDS and SLVS200 are TBD in Table 4.12. CrossLink Maximum I/O Buffer Speed • Updated Table 4.13. CrossLink External Switching Characteristics [4, 5] • Updated min values of t_{SU_MIPIX4} and t_{HO_MIPIX4} in Table 4.16. 1200 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1200 Mb/s > MIPI D-PHY Data Rate > 1000 Mb/s) and Table 4.17. 1000 Mb/s MIPI_DPHY_X4_RX/TX Timing Table (1000 Mb/s > MIPI D-PHY Data Rate > 10 Mb/s) • Updated Table 4.20. CrossLink sysCONFIG Port Timing Specifications • Updated Table 4.21. SRAM Configuration Time from NVCM Updated Pinout Information section Updated CrossLink Part Number Description
July 2016	1.0	Updated document numbers.
May 2016	1.0	First preliminary release.

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