Real-Time Clock (RTC) Counter

The Real-Time Clock (RTC) counter is a 16-bit counter that is functional in active mode (AM) and several low-power modes (LPMs). RTC counter accepts multiple clock sources, which are selected by control registers settings, to generate timing from less than 1 µs up to many hours. This chapter describes the operation and use of the RTC counter module.

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15.1 RTC Counter Introduction

The RTC counter is a 16-bit counter that functions in AM and all LPMs except LPM4.5. This module can accept any one of three clock sources:

1. Device specific: SMCLK (maximum operating frequency depends on device configuration) or ACLK (approximately 32 kHz)
2. XT1CLK (approximately 32 kHz)
3. VLOCLK (approximately 10 kHz)

In LPM3.5, RTC counter accepts only XT1CLK or VLOCLK as its clock source to periodically wake up the device. The selected clock source can be predivided before driving the main 16-bit counter. The 16-bit counter supports continuous tick by a 16-bit modulo register that is user accessible and a 16-bit shadow register that is not user accessible. The RTC counter can generate an interrupt when the counter value overflows at the preset shadow register value. RTC counter features include:

- 16-bit modulo counter architecture
  - 16-bit basic counter
  - 16-bit modulo register that is user accessible for read and write
  - 16-bit shadow register that is not user accessible to support continued operation when the modulo value is updated
  - 16-bit compare logic to detect counter overflow at the boundary of the shadow register value
- Three possible clock sources that are selected by setting the RTCSS bits: XT1CLK, VLOCLK, or device specific (SMCLK or ACLK)
  - SMCLK is functional in AM and LPM0 only
  - ACLK is functional in AM to LPM3.
  - XT1CLK and VLOCLK are functional in AM and LPMs, excluding LPM4.5
- Configurable predivider for the source clock input is set by the RTCPS bits
  - Passthrough: ÷1; the input clock source directly drives the 16-bit counter
  - Predivider: ÷10, ÷100, ÷1000, ÷16, ÷64, ÷256, or ÷1024; the input clock source is divided by the selected value before it drives the 16-bit counter
- A hardware interrupt is triggered (if enabled by the RTCIE bit) when the counter value reaches the shadow register value.
- An overflow event can be a trigger in hardware for other modules. See the device-specific data sheet for details on which modules support this trigger.
- Software can reset the counter by setting the RTCSR bit.

Figure 15-1 shows the block diagram of the RTC counter.

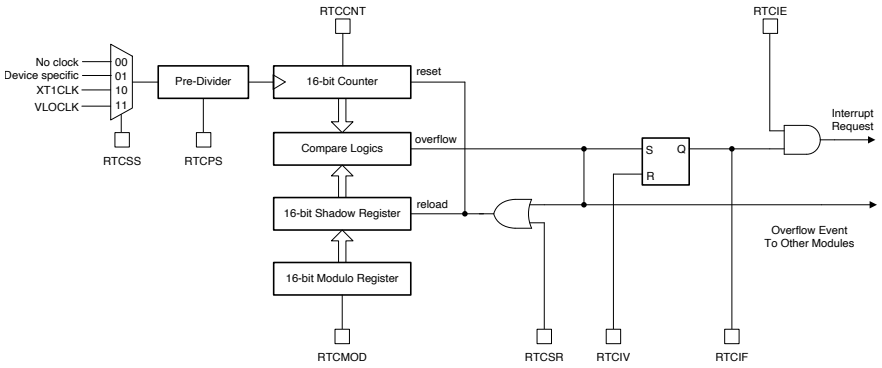

Figure 15-1. RTC Counter Block Diagram

15.2 RTC Counter Operation

The RTC counter module is configured with user software. The setup and operation of RTC counter is described in the following sections.

15.2.1 16-Bit Timer Counter

The 16-bit timer counter register, RTCCNT, increments with each rising edge of the source clock signal. RTCCNT is read only with software. When the counter value reaches the value of the shadow register, the RTC counter generates an overflow signal, the counter value resets to zero, and the counter continues to tick without interruption. As long as the counter clock source that is specified by the RTCSS bit is active, the counter is operational.

RTCCNT is cleared by the overflow event, or it can be reset by software writing logic 1 to the RTCSR bit in the RTCCTL register. If the counter is reset by software, the shadow register is updated by the value in the modulo register at the next cycle of the divided clock, but no overflow event or interrupt is generated.

The maximum input frequency to the counter during LPM3.5 is 40 kHz. Therefore, the predivider must be configured so that the divided clock frequency does not exceed 40 kHz.

15.2.2 Clock Source Select and Divider

In AM and LPM0, the RTC counter clock can be sourced from device-specific (SMCLK or ACLK), XT1CLK, or VLOCLK. In LPM3, ACLK, XT1CLK, or VLOCLK can be selected. In LPM3.5, only XT1CLK or VLOCLK can be selected. The clock source is specified by the RTCSS bits in the RTCCTL register. After reset, RTCSS defaults to 00b (disabled), which means that no clock source is selected.

The selected clock source can be predivided before it is used by the counter. If the passthrough mode (÷1) is selected, the predivider is bypassed and the selected clock source directly sources the counter. The predivider options of ÷16, ÷64, ÷256, and ÷1024 allow simple division of clock source frequencies that are powers of 2, such as from 32768-Hz crystals. The predivider options of ÷10, ÷100, and ÷1000 allow simple division of clock source frequencies that are multiples of 10, such as from 4-MHz or 8-MHz clock inputs.

NOTE: Clock Source Selection

In LPM3.5, the RTC counter is very low power, and the divided clock source that drives the counter can have a maximum frequency of 40 kHz.

TI recommends a software reset by asserting the RTCSR bit after the RTC clock source is switched. An unexpected interrupt may happen during the clock source change, because of the synchronization time. The count setting is resynchronized with the new clock on this software reset.

15.2.3 Modulo Register (RTCMOD) and Shadow Register

The modulo register (RTCMOD) is a 16-bit register that is set by user software. The value in RTCMOD is latched and does not take effect until it is loaded into the shadow register. The shadow register is also a 16-bit register, and it stores the modulo value that the RTC counter logic compares with the counter value. The shadow register acts as a buffer to the RTCMOD register, so that software can set a new modulo value without interrupting the counter. The RTCMOD register is read and write accessible by the user. The shadow register is not directly accessible by the user.

The value in RTCMOD is loaded to the shadow register under two conditions:

1. When the counter reaches the value in the shadow register, which also triggers an overflow signal and clears the counter value.
2. When a software reset is triggered by software writing logic 1 to the RTCSR bit in the RTCCTL register.

Because the shadow register always updates its value from RTCMOD, software must set RTCMOD before the hardware overflow occurs. Using the software reset lets software immediately set the target modulo value into shadow register without waiting for the next overflow. If the value in RTCMOD is not updated when the hardware overflow occurs, the shadow register fetches the previous modulo value stored in RTCMOD. If RTCMOD is changed multiple times before the overflow, only the last value is loaded to the shadow register.

RTC counter always generates an overflow when the RTCMOD is set to either 0x0000 or 0x0001.

Care should be taken when setting RTCMOD so that the overflow events do not happen too quickly to be serviced. When the selected RTC counter source frequency is close to the CPU clock frequency, the modulo value must be long enough that the CPU is able to respond to the RTC counter interrupt service routine (ISR) in time before the next RTC counter interrupt occurs. In addition, frequent writes to the RTCSR bit (software reset) could lead to an overflow event being missed, as the count is reset each time, and the RTCMOD setting overwrites the current shadow register setting.

Figure 15-2 shows a hardware overflow event loading the new value (0x2000) from RTCMOD into the shadow register, replacing the previous value (0x4000).

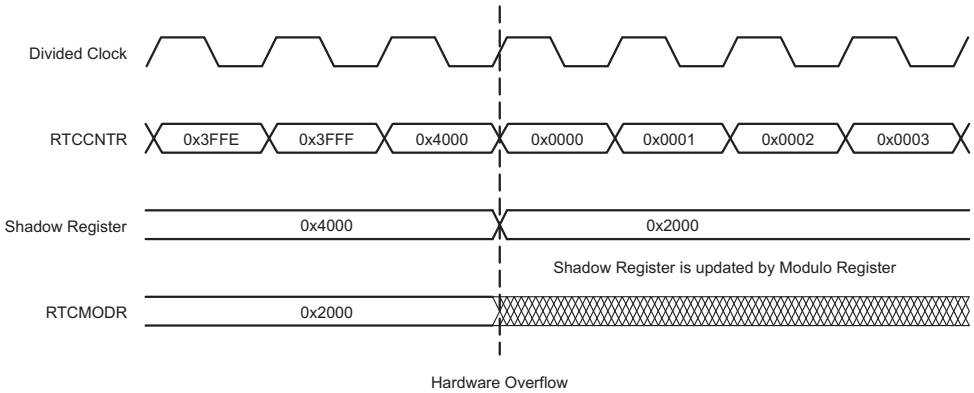

Figure 15-2. Shadow Register Example

15.2.4 RTC Counter Interrupt and External Event/Trigger

There is an interrupt vector (RTCIV) associated with the 16-bit RTC counter module interrupt flag (RTCIFG).

When an overflow occurs, the RTCIFG bit in the RTCCTL register is set until it is cleared by a read of the RTCIV register. At the same time, an interrupt is submitted to the CPU for post-processing, if the RTCIE bit in the RTCCTL register is set. Reading RTCIV register clears the interrupt flag.

TI recommends clearing the RTCIFG bit by reading the RTCIV register before enabling the RTC counter interrupt. Otherwise, an interrupt might be generated if the RTCIFG was already set by a previous overflow.

In addition to the interrupt, the hardware overflow also submits an external trigger to other on-chip modules as a synchronous signal. Refer to the device-specific data sheet for more information on module triggers that are available on particular devices.

15.3 RTC Counter Registers

Table 15-1 lists the RTC counter registers and the address offset for each register. Refer to the device-specific data sheet for the base address of the module.

Table 15-1. RTC Counter Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	RTCCTL	Real-Time Clock Control	Read/write	Word	0000h	Section 15.3.1
00h	RTCCTL_L		Read/write	Byte	00h	
01h	RTCCTL_H		Read/write	Byte	00h	
04h	RTCIV	Real-Time Clock Interrupt Vector	Read/write	Word	0000h	Section 15.3.2
04h	RTCIV_L		Read/write	Byte	00h	
05h	RTCIV_H		Read/write	Byte	00h	
08h	RTCMOD	Real-Timer Clock Modulo	Read/write	Word	BEEFh	Section 15.3.3
08h	RTCMOD_L		Read/write	Byte	EFh	
09h	RTCMOD_H		Read/write	Byte	BEh	
0Ch	RTCCNT	Real-Time Clock Counter	Read	Word	0000h	Section 15.3.4
0Ch	RTCCNT_L		Read	Byte	00h	
0Dh	RTCCNT_H		Read	Byte	00h	

15.3.1 RTCCTL Register

RTC Counter Control Register

Figure 15-3. RTCCTL Register

15	14	13	12	11	10	9	8
Reserved		RTCSS		Reserved	RTCPS		
r0	r0	rw-{0}	rw-{0}	r0	rw-{0}	rw-{0}	rw-{0}
7	6	5	4	3	2	1	0
Reserved	RTCSR	Reserved				RTCIE	RTCIFG
r0	w-{0}	r0	r0	r0	r0	rw-{0}	r-{0}

Table 15-2. RTCCTL Register Description

Bit	Field	Type	Reset	Description
15-14	Reserved	R	0h	Reserved
13-12	RTCSS	RW	0h	Real-time clock source select 00b = No clock (Stop) 01b = Device specific 10b = XT1CLK 11b = VLOCLK
11	Reserved	R	0h	Reserved
10-8	RTCPS	RW	0h	Real-time clock predivider select 000b = /1 001b = /10 010b = /100 011b = /1000 100b = /16 101b = /64 110b = /256 111b = /1024
7	Reserved	R	0h	Reserved
6	RTCSR	W	0h	Real-time software reset. This is a write-only bit and is always read with logic 0. 0b = Write 0 has no effect 1b = Write 1 to this bit clears the counter value and reloads the shadow register value from the modulo register at the next tick of the selected source clock. No overflow event or interrupt is generated.
5-2	Reserved	R	0h	Reserved
1	RTCIE	RW	0h	Real-time interrupt enable 0b = Interrupt disabled 1b = Interrupt enabled
0	RTCIFG	R	0h	Real-time interrupt flag. This bit reports the status of a pending interrupt. This read only bit can be cleared by reading RTCIV register. 0b = No interrupt pending 1b = Interrupt pending

15.3.2 RTCIV Register

RTC Counter Interrupt Vector Register

Figure 15-4. RTCIV Register

15	14	13	12	11	10	9	8
RTCIV							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
RTCIV							
r0	r0	r0	r0	r0	r0	r-{0}	r0

Table 15-3. RTCIV Register Description

Bit	Field	Type	Reset	Description
15-0	RTCIV	R	0h	Low-power-counter interrupt vector. 00h = No interrupt pending 02h = Interrupt Source: RTC Counter Overflow; Interrupt Flag: RTCIFG

15.3.3 RTCMOD Register

RTC Counter Modulo Register

Figure 15-5. RTCMOD Register

15	14	13	12	11	10	9	8
RTCMOD							
rw-{1}	rw-{0}	rw-{1}	rw-{1}	rw-{1}	rw-{1}	rw-{1}	rw-{0}
7	6	5	4	3	2	1	0
RTCMOD							
rw-{1}	rw-{1}	rw-{1}	rw-{0}	rw-{1}	rw-{1}	rw-{1}	rw-{1}

Table 15-4. RTCMOD Register Description

Bit	Field	Type	Reset	Description
15-0	RTCMOD	RW	BEEFh	RTC modulo value

15.3.4 RTCCNT Register

RTC Counter Register

Figure 15-6. RTCCNT Register

15	14	13	12	11	10	9	8
RTCCNT							
r-{0}	r-{0}	r-{0}	r-{0}	r-{0}	r-{0}	r-{0}	r-{0}
7	6	5	4	3	2	1	0
RTCCNT							
r-{0}	r-{0}	r-{0}	r-{0}	r-{0}	r-{0}	r-{0}	r-{0}

Table 15-5. RTCCNT Register Description

Bit	Field	Type	Reset	Description
15-0	RTCCNT	R	0h	RTC counter. This is a read-only register and reflects the current counter value.