# CS 362: Homework 7

Due on April 12, 2024 at 11:59pm

Professor Troy 11:00am

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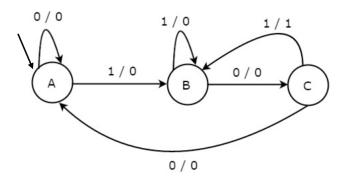
## Problem 1

Consider the following Finite State Machine:

Start State: A

Inputs are listed before the slash on each transition.

Outputs are listed after the slash on each transistion.



#### Solution

1. Is the above FSM a Moore machine or a Mealy machine? Mealy Machine.

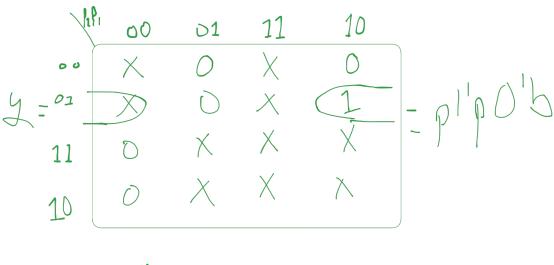
2. What is output by the above FSM for:

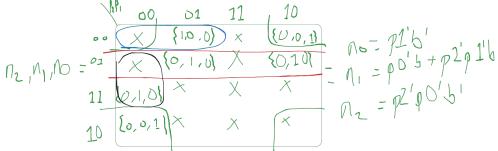
3. Give the truth table for the above Finite State Machine.

Encode the states using "one hot bit" encoding values of:  $A \to 001$ ,  $B \to 010$ ,  $C \to 100$ 

					)	,	
p2	p1	p0	b	y	n2	n1	n0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	0	0
0	1	0	1	0	0	1	0
1	0	0	0	0	0	0	1
1	0	0	1	1	0	1	0

4. Write out the simplified expressions for the next state and output values. You can use K-maps or boolean algebra to determine simplified expressions. Show your work.

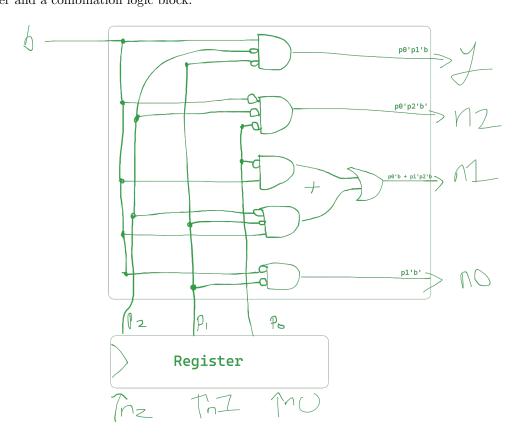




5. Draw the circuit diagram for the Finite State Machine.

Use the format as shown in class and in the zyBooks (and in following programs) that contain a state register and a combination logic block.

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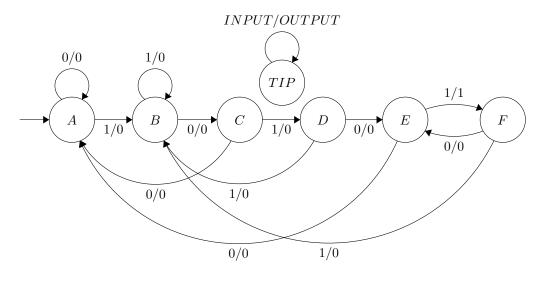
## Problem 2

Suppose we have a machine that takes in an infinite stream of bits, one bit at a time. On every input, the machine will output '0', unless the machine has seen the pattern '10101' in the last four inputs where it will instead output '1'.

Below is an example of this behavior. Input: 01010101010101010111101010... Output: 000001010000001010000010...

### Solution

1. Design/Draw an FSM that exhibits the behavior described above.



2. Give the truth table for the above Finite State Machine. Encode the states using binary encoding.

$$A \to 000$$

$$B \to 001$$

$$C \rightarrow 010$$

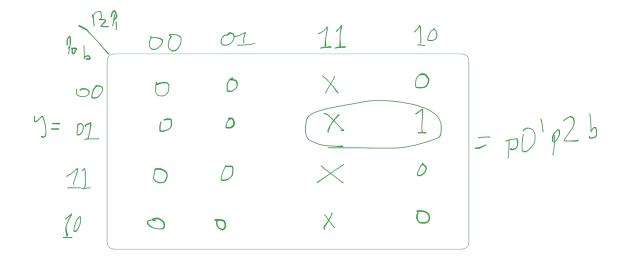
$$D \rightarrow 011$$

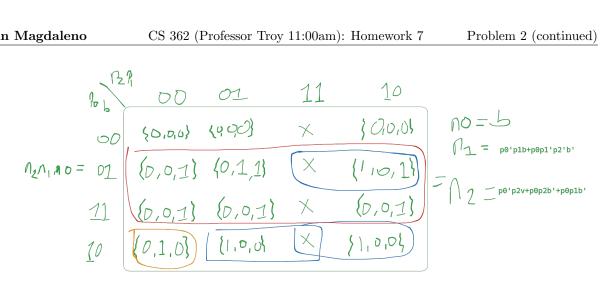
$$E \rightarrow 100$$

$$F \rightarrow 101$$

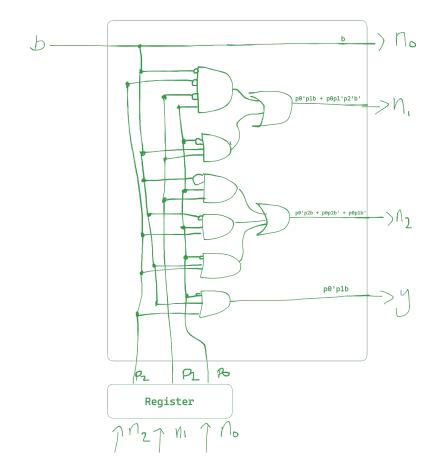
p2	<i>p</i> 1	p0	b	y	n2	n1	n0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	0	1
0	1	0	0	0	0	0	0
0	1	0	1	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	0	0	1
1	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1
1	0	1	0	0	1	0	0
1	0	1	1	0	0	0	1

3. Write out the simplified expressions for the next state and output values. You can use K-maps or boolean algebra to determine simplified expressions. Show your work.



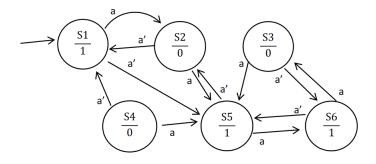


4. Draw the circuit diagram for your Finite State Machine. Use the format as shown in class and in the zyBooks that contain a state register and a combination logic block.



## Problem 3

The following Finite State Machine can be reduced.



### Solution

Identify which states are equivalent and can be combined together
 Include the specifics conditions as to why those states can be reduced.
 Show the State Group Tables from the "Partitioning Method" for your answer.

	State	Inputs	NxState	Group
y=0 G1	\$2 \$3 \$4	0	S6	G2 G2 G2
	S2 S3 S4	1	S5	G2 G2 G2

_	State	Inputs	NxState	Group
/=1 62	S1 S5 S6	0	S2	G2 G1 G2
	S1 S5 S6	1	S6	G1 G2 G1

	State	Inputs	NxState Group
y=0 G1	\$2 \$3 \$4 Equivalent: \$2, \$3, \$4:0	0 0 0	S1 G2 S6 G2 S1 G2
	S2 S3 S4	1 1 1	S5 G3 S5 G3 S5 G3

	State	Inputs	NxState Group
y=0 G1	S1 S6	0	S5 G3 S5 G3
	S1 S6 Equivalent: S1, S6	1	S2 G1 S3 G1

	State	Inputs	NxState Group
y=1 G3	S5	0	S2 G1
	S5	1	S6 G2

 $2.\,$  Draw the reduced FSM that does not have any equivalent states.

