CS 362: Homework 5

Due on March 23, 2024 at 11:59

Professor Troy 11:00am

Ryan Magdaleno
rmagd2@uic.edu

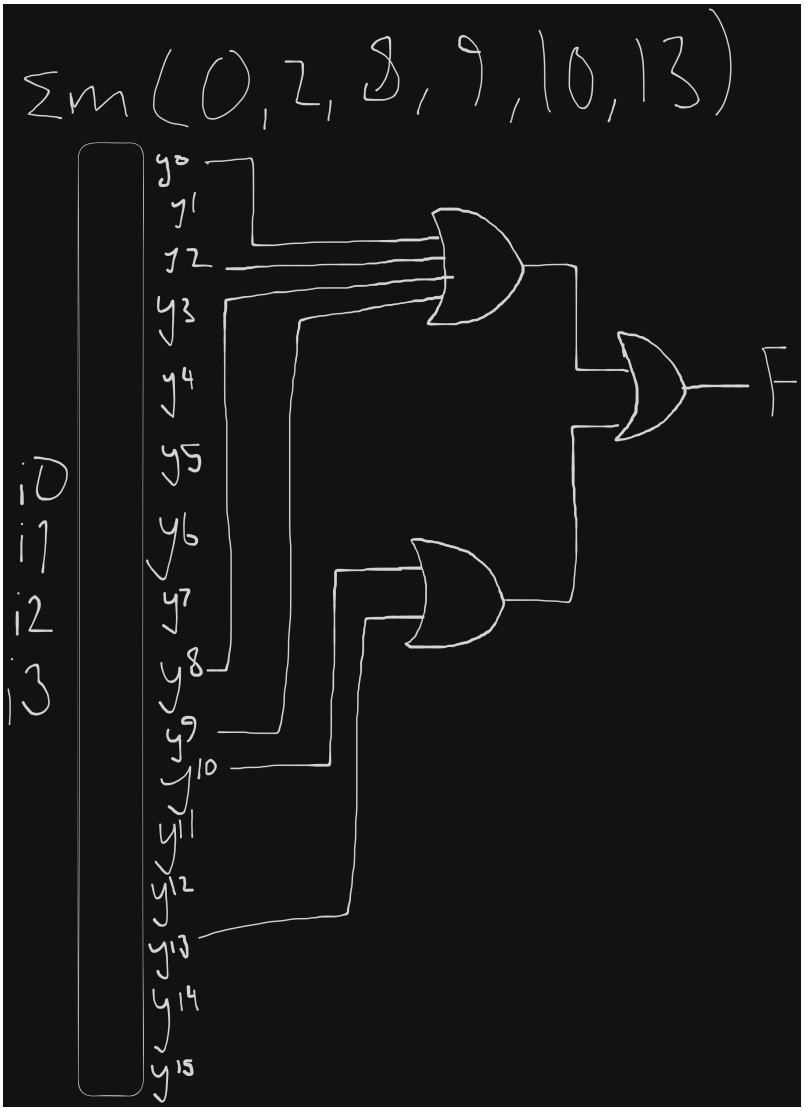
Problem 1

Implement the equations below using a 4-to-16 decoder and minimal other gates.
Hint: only 1 other gate is needed per answer.

Solution

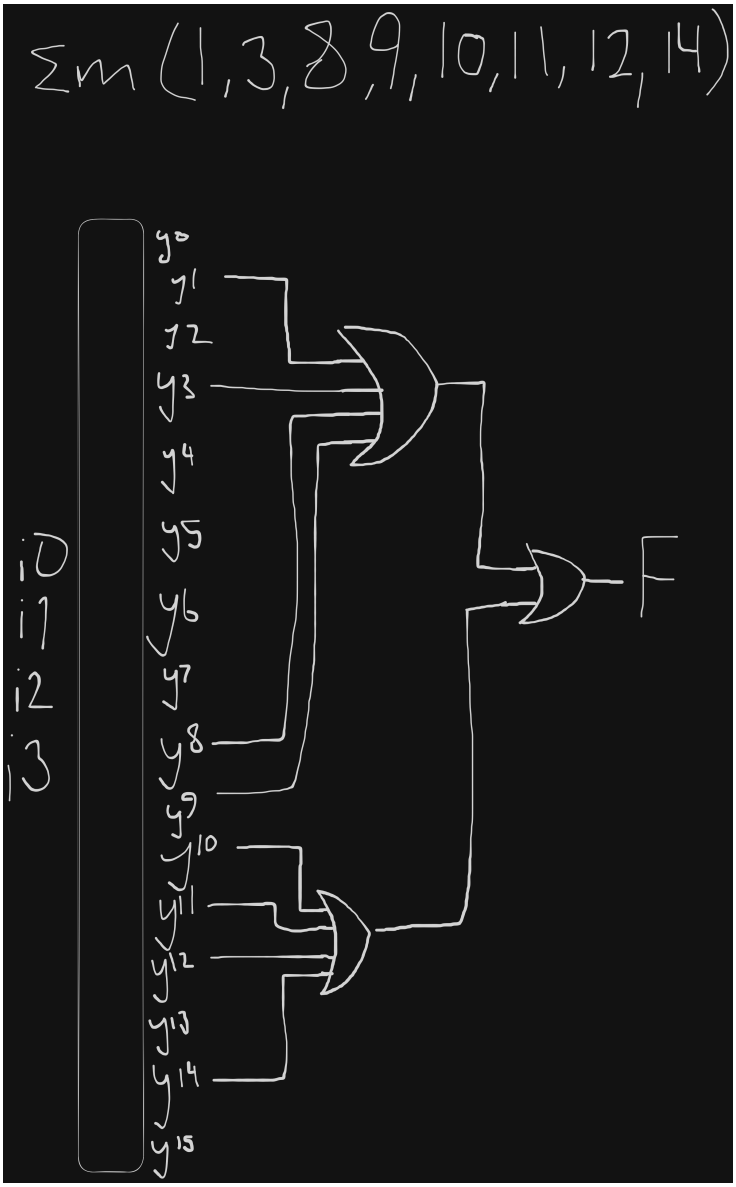
Part A

$$F(A, B, C, D) = \Sigma m(0, 2, 8, 9, 10, 13)$$



Part B

$$F(A, B, C, D) = \Sigma m(1, 3, 8, 9, 10, 11, 12, 14)$$

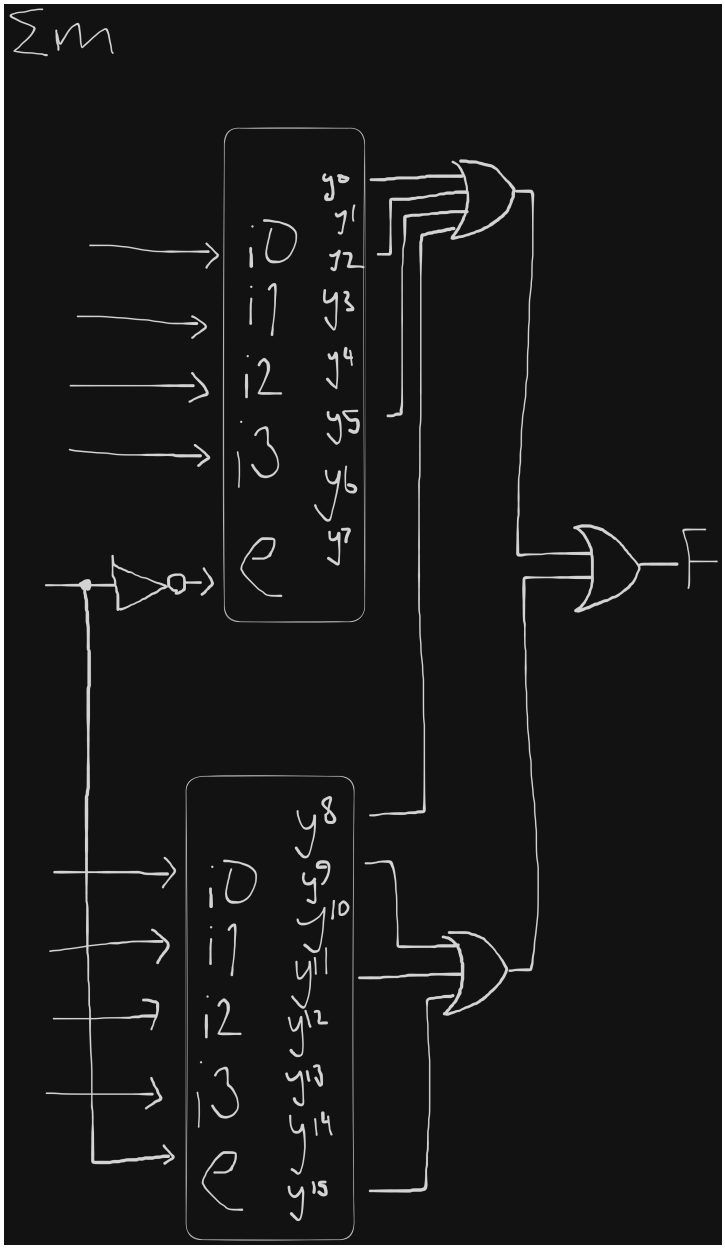


Problem 2

Implement the equations below using two 3-to-18 decoders with enable and minimal other gates.

Solution

$$F(A, B, C, D) = \Sigma m(0, 2, 5, 8, 9, 11, 15)$$



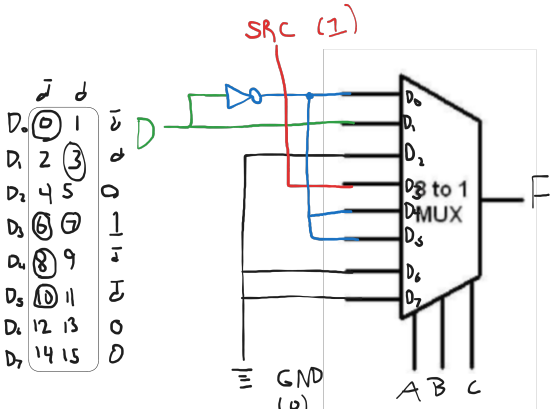
Problem 3

Implement the equations below using an 8-to-1 multiplexor and minimal other gates
Hint: at most only 1 other gate is needed per answer.

Solution

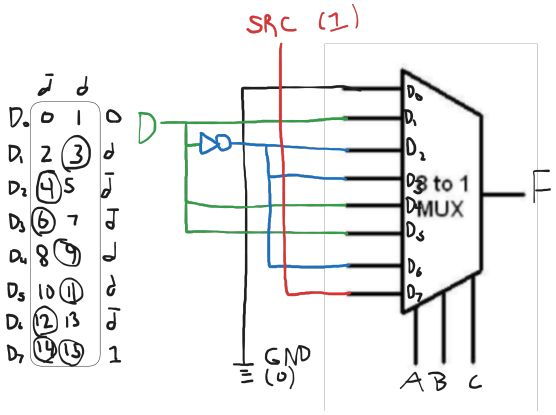
Part A

$$F(A, B, C, D) = \Sigma m(0, 3, 6, 7, 8, 10)$$



Part B

$$F(A, B, C, D) = \Sigma m(3, 4, 6, 9, 11, 12, 14, 15)$$



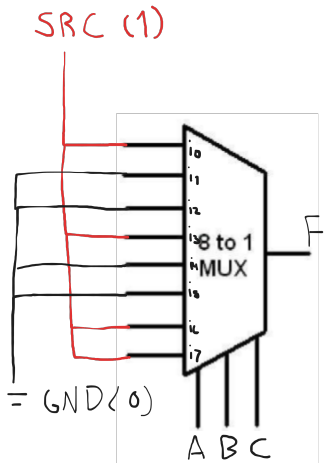
Problem 4

Implement the equations below using the given multiplexor and minimal other gates.

Solution

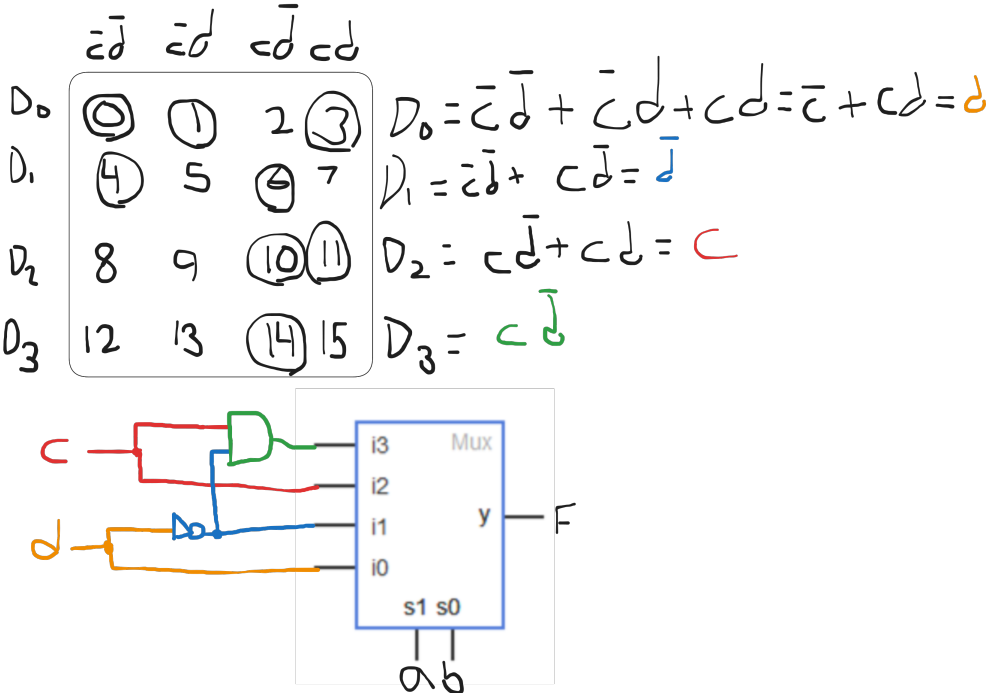
Part A

$$F(A, B, C) = \Sigma m(0, 3, 6, 7)$$



Part B

$$F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 6, 10, 11, 14)$$

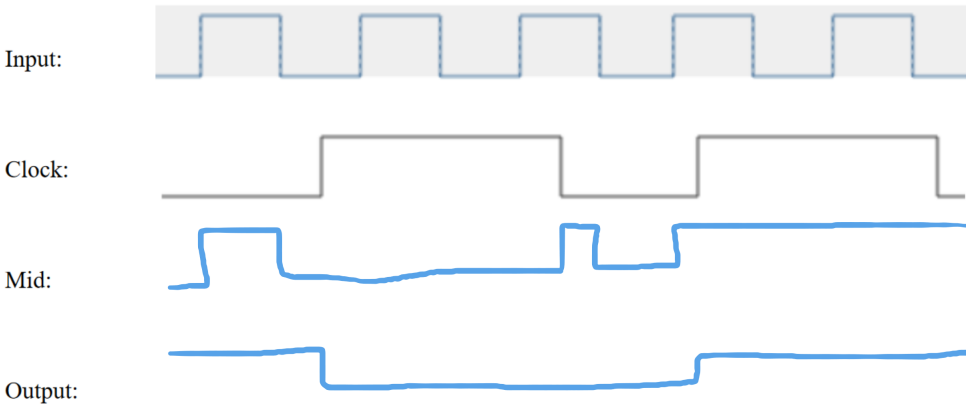


Problem 5

Part A

Fill in the timing diagram below with the values of Mid and Output for the D flip-flip.
Assume the initial value of Output is 1/high.

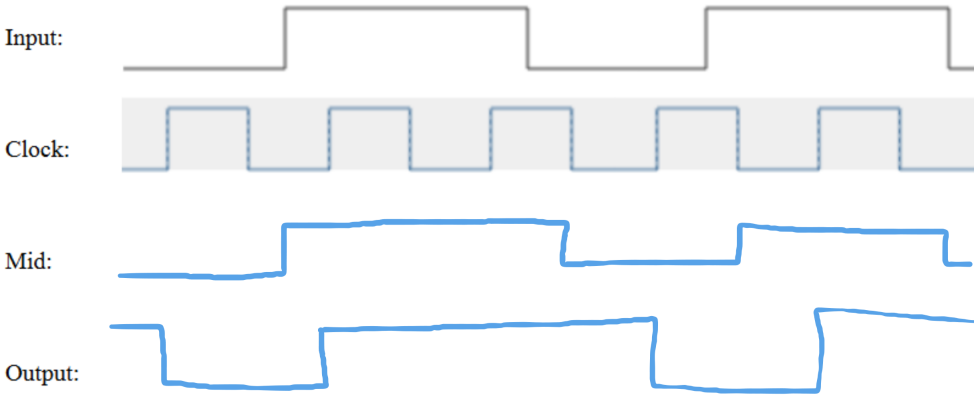
Solution



Part B

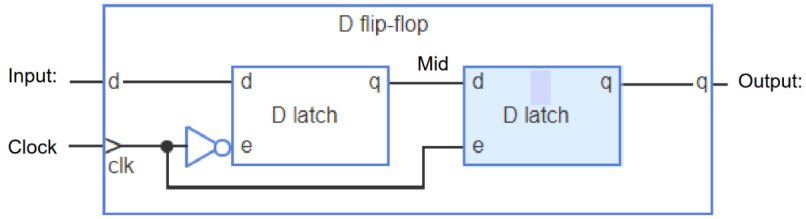
Fill in the timing diagram below with the values of Mid and Output for the D flip-flip as shown above.
Assume the initial value of Output is 1/high.

Solution



Problem 6

The following D flip-flop is a rising-edge-triggered flip-flop.
Redraw it to become a falling-edge-triggered flip-flop.



Solution