MicroBlaze Processor Performance

MicroBlaze™ processor architecture balances execution performance against implementation size. Benchmark performance varies depending on the processor configuration, implementation tool results, targeted FPGA architecture, and device speed grade.

The performance numbers below are best case comparison numbers achieved under industry-standard conditions. The results do not represent typical system performance for general embedded applications. The maximum performance and maximum clock frequency vary from one design to another based on configuration options.

MicroBlaze Processor v7.0 Performance Benchmarks

The Dhrystone 2.1 industry standard benchmark measures the performance of a processor executing a specific distribution of operations. The performance is reported as the number of Dhrystone instructions executed per second (DMIPS).

The following tables represent the maximum Dhrystone performance the MicroBlaze processor v7.00 (in EDK 9.2) can deliver. The targeted system includes a UART and timer necessary for the benchmark. MicroBlaze is configured with a hard multiplier, barrel shifter and one FSL port. Execution is done from on-chip memory.

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MicroBlaze Processor

Overview

Architecture

FPU

MicroBlaze Processor Performance

FPGA	Size	Clock Frequency	Dhrystone 2.1	Performance
Virtex®-5 (XC5VLX50) No MMU 5-stage	1,010 LUTs	210 MHz	240 DMIPS	1.15 DMIPS/MHz
Spartan®-3 (XC3S1600E-5) 5-stage	1,842 LUTs	100 MHz	115 DMIPS	1.15 DMIPS/MHz
Spartan-3 (XC3S1600E-5) 3-stage	1,357 LUTs	100 MHz	92 DMIPS	0.92 DMIPS/MHz

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