Dhrystone Benchmark Results for Products of MIPS Technologies, Inc.

This article reports Dhrystone benchmark results for several popular cores from MIPS Technologies and describes the methodology used to obtain these results.

Results

Two sets of Dhrystone numbers are reported:

- Conforming Dhrystone - generated by in accordance with Reinhold Weiker's guidelines for Dhrystone version 2.1 found in Ref [1] and summarized below.
- Inline Dhrystone - generated as described below.

Dhrystone Benchmark Report					
Core	**DMIPS/MHz**	**Freq. (MHz)**	**DMIPS**	**Inline DMIPS/MHz**	**Inline DMIPS**
4Kc™	1.39	300 WC, 0.13LV	420	1.8	540
4KEc™	1.53	300 WC, 0.13LV	459	2.0	600
24Kc™	1.44	500 WC, 0.13LV	720	1.93	965
24Kf™	1.44	500 WC, 0.13LV	720	1.93	965
5Kc™	1.5	350 WC, 0.13LV	525	2.2	700
5Kf™	1.5	320 WC, 0.13LV	476	2.2	640
20Kc™	1.7	600 typ., 0.13 LV	1020	2.4	1320

Conforming Dhrystone v2.1 Methodology of MIPS Technologies

1. The source code used in the measurement loop is the original unmodified K&R C source code. No source code edits have been made inside the timing loop. Porting Dhrystone to MIPS Technologies' hardware environment required minor edits to the printout functions and timing control, both of which are outside the test loop.
2. Software used to obtain Dhrystone results, like any software, is highly dependent on the compiler and libraries for its performance. The source files are compiled separately using the commercially available version 4.0 of the Green Hills MIPS compiler. Compilation uses the Ospeed optimization. Ospeed enables optimizations such as loop unrolling, which are specifically allowed by the Dhrystone guidelines. No link-time optimizations are used.
3. Procedure merging such as inlining or macro expansion of procedures is not done.
4. Standard compiler libraries are used inside the measurement loop except for *strcmp(),* which is implemented in general-purpose processor-specific assembler code, as allowed per Ref [2]. This code, which cannot be inlined, has been made available to compiler vendors for inclusion in standard libraries.
5. All figures quoted are relative to the 1757 DMIPS achieved by the VAX 11/780.

6. All DMIPS/MHz numbers were generated using silicon implementations of the MIPS Technologies cores. The 24Kc/f and 4KEc cores are MIPS32™ Release 2 implementations. The 4Kc core is a MIPS32 implementation, the 5Kc/f and 20Kc cores are MIPS64™ implementations.

Inline Dhrystone Methodology of MIPS Technologies

For ease of comparison with other semiconductor vendors, MIPS Technologies provides both conforming and inline Dhrystone numbers. The inline numbers are generated by using the conforming Dhrystone setup, but enabling two-pass inlining capability through the addition of the Green Hills Systems' compiler switch OI. No additional optimizations are made.

References

[1] Dhrystone Benchmark: Rationale for Version 2 and Measurement Rules published in SIGPLAN Notices 23,8 (Aug. 1988), 49-62]

[2] Understanding Variations in Dhrystone Performance, Reinhold P. Weicker, Siemens AG, AUT E 51, Erlangen, April 1989