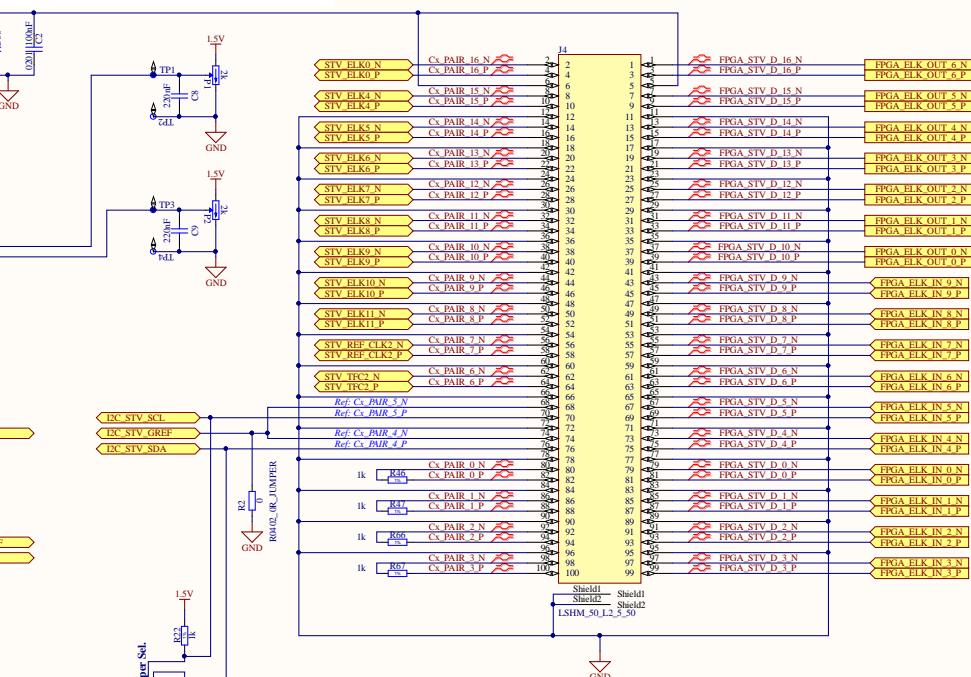
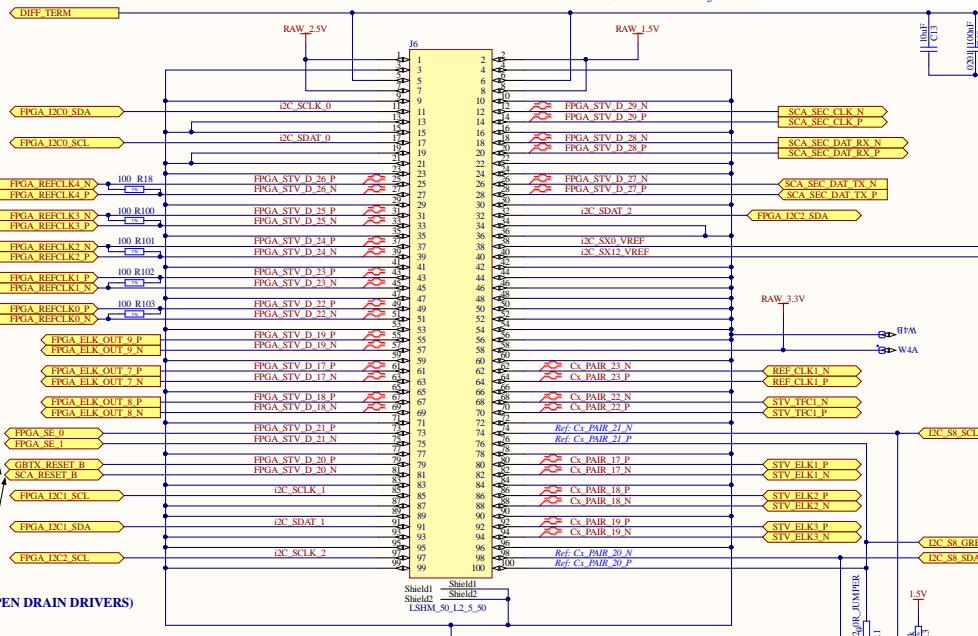


CONN PLACED ADJACENT TO FPGAs 104-53 SIDE  
WHICH IS NOT FACING THE ERBZ CONN.

GBTx Power via Aux Regulator!

These contact assignments are flipped relative to the COMET board per Samtec note 4: WHEN MATING WITH ANOTHER LSHM-DV, PIN 01 WILL MATE WITH CONTACT 02 ON THE MATING CONNECTOR. (These two connector pin assignments were lifted directly from the remapped COMET termination daughter board schematic)



**Note: The i2C\_0 interface is constrained to a max 2.5V**  
**Note: The i2C\_1 and '\_2 interfaces allow a max of 3.3V**

Note 1: The SALT8 test board ER8 connector signal-pins assignments restrict the location to the furthest out STAVE position.

The associated signals specific to SALT8 testing include:

i2C\_ST

TFC\_STAVE

REF\_CLK\_STAVE

ELK11:0]

NOTE 2: The following signals are available at all of the STAVE positions

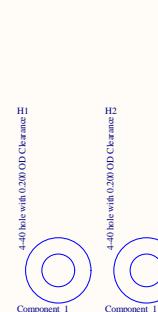
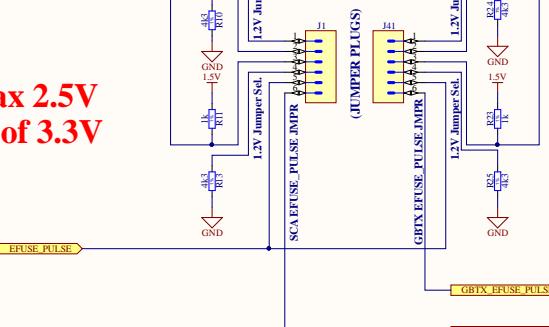
i2C\_ST

TFC\_STAVE

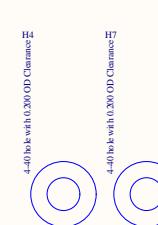
REF\_CLK\_STAVE

ELK11:0]

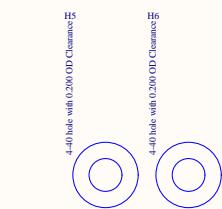
NOTE 3: STV\_DIFF\_PAIR 19, 20, 22, and 23 signal P/N pairs were inadvertently swapped (ie inverted) on the original passive termination daughterboard relative to the COMET Base board. The swaps have been corrected for this GBTx daughter board.



These holes are for pot access on host board.



These holes are for interface with the PWB retention stand-offs.



These holes are for spacers to the heat sink

University of Maryland

COMET GBT Daughter Board LSHM_Comms.SchDoc			
Size	Number	Revision	Rev A
Date:	6/17/2019	Sheet 1	4 of
File:	C:\Users\LSHM_Comms.SchDoc	Drawn By:	Tom O'Banion

A

B

C

D

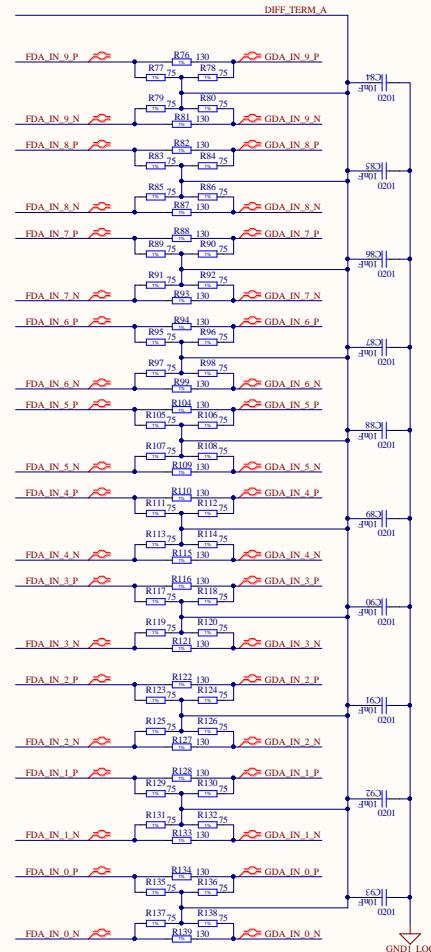
A

B

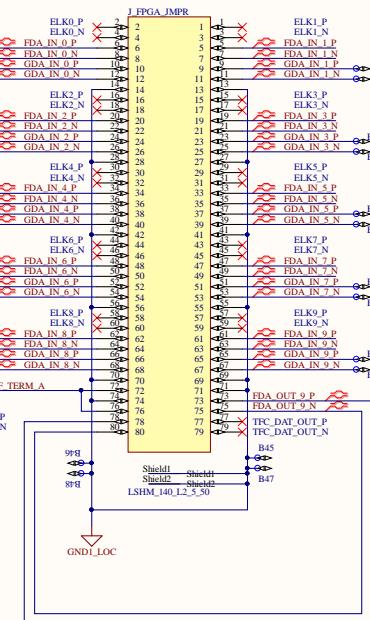
C

D

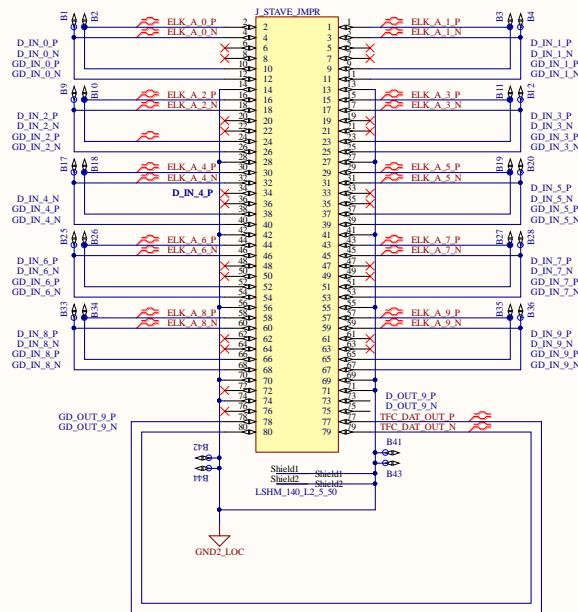
**THE NETS ON THIS PAGE SHOULD COMPLETELY INDEPENDENT OF THE OTHER SCHEMATIC PAGES!!!!**



Wire Jumper for connecting the  
FPFA ELINK outputs to the GBTX inputs via attenuator networks  
(NOTE: THESE ARE MIRRORED PIN ASSIGNMENTS!)

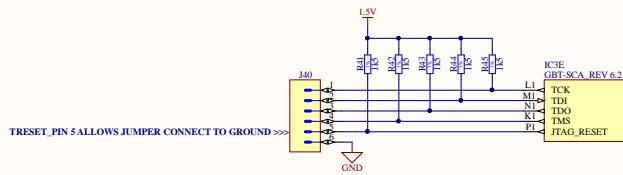


Wire Jumper for connecting the  
Stave ELINKs to the GBTX inputs  
(NOTE: THESE ARE MIRRORED PIN ASSIGNMENTS!)

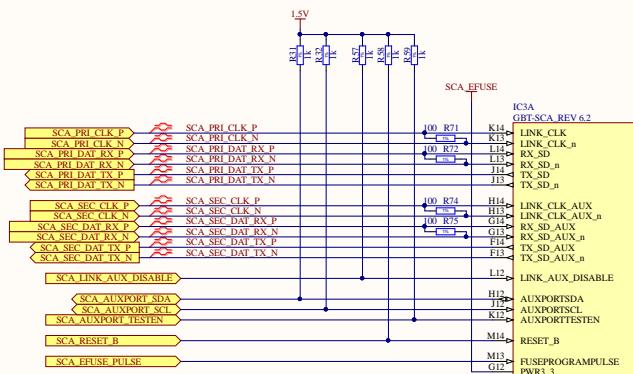


Title		
Size	Number	Revision
Date: 6/17/2019 File: C:\Users\1\Documents\Select Jumpers.SchDoc	Sheet of	1

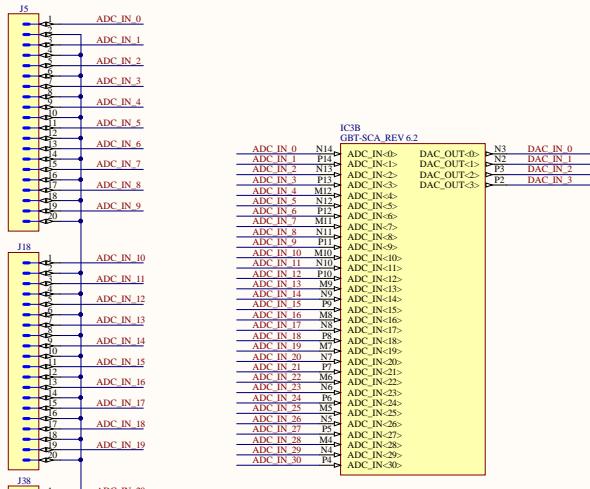
A



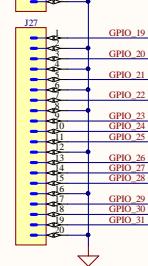
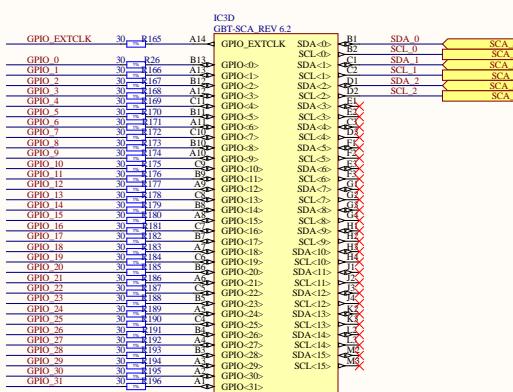
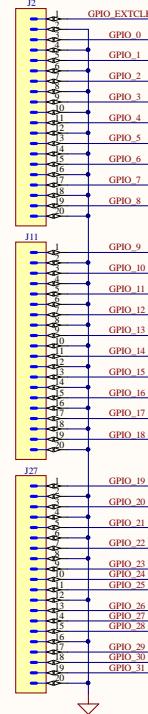
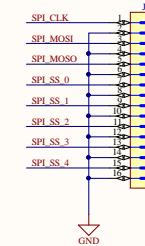
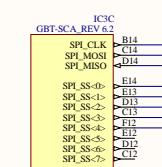
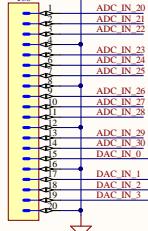
B



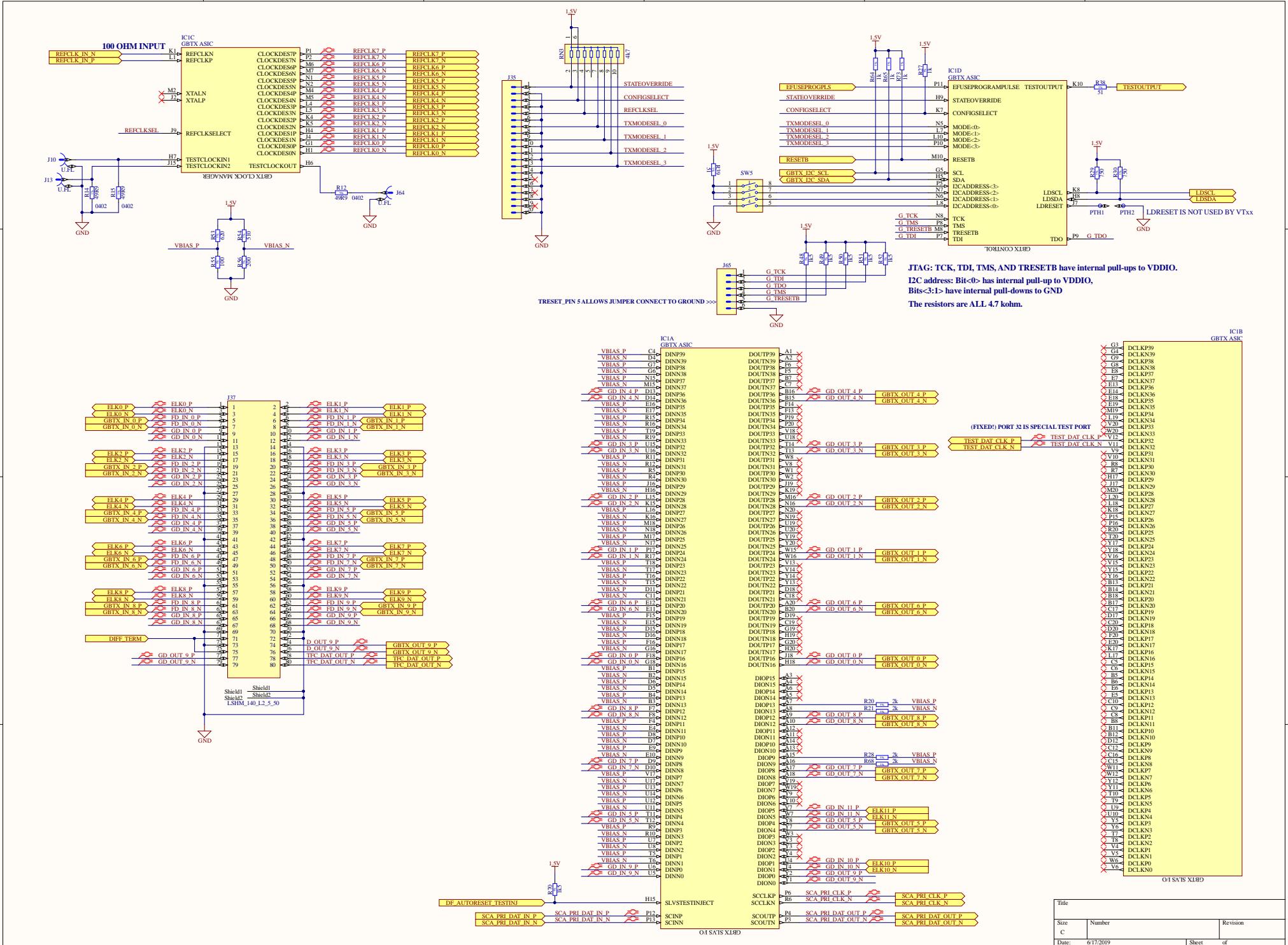
C



D

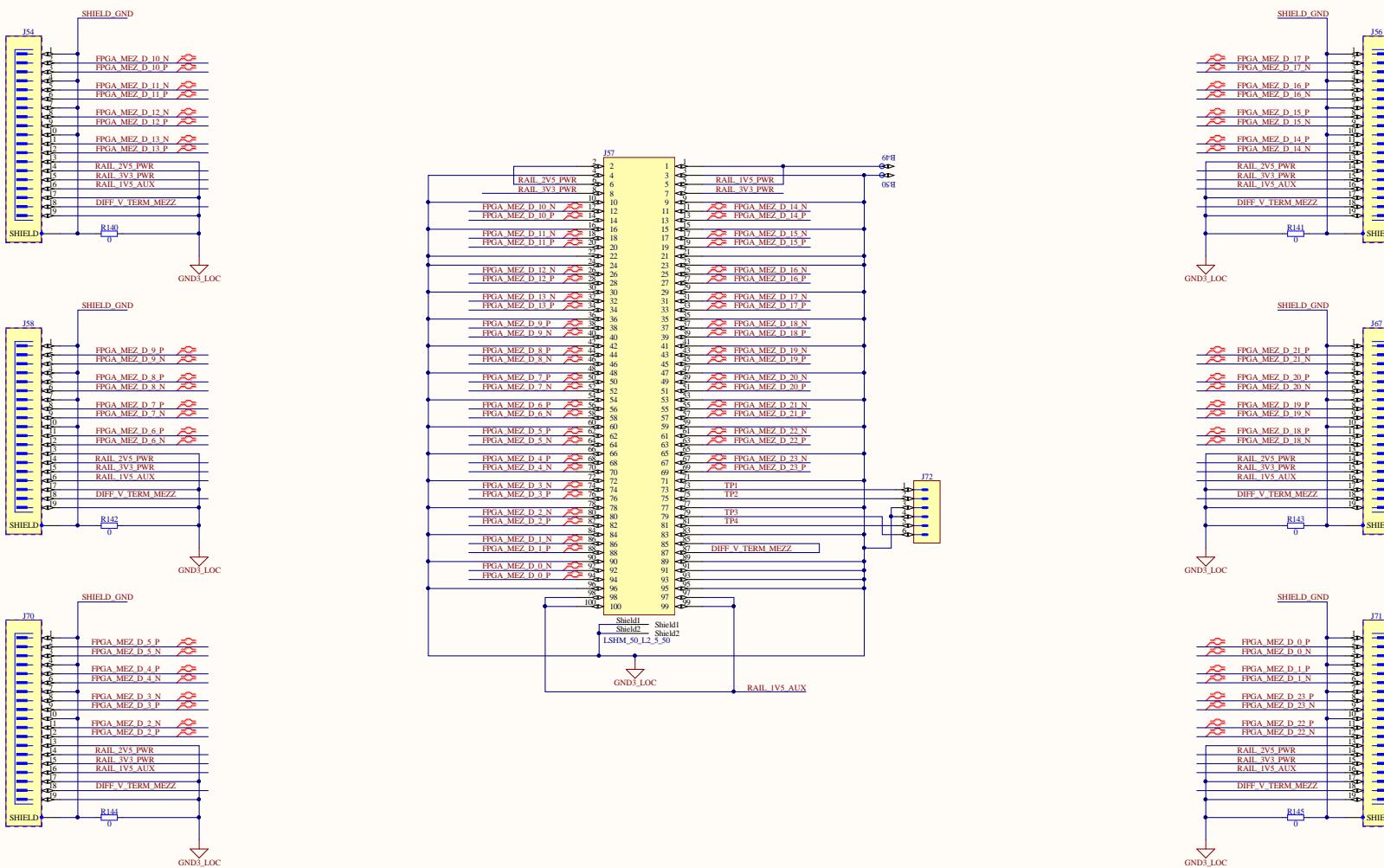


Title		
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C		
Date: 6/17/2019	Sheet of	
File: C:\Users\...\GBT-SCA.SchDoc		Drawn By:

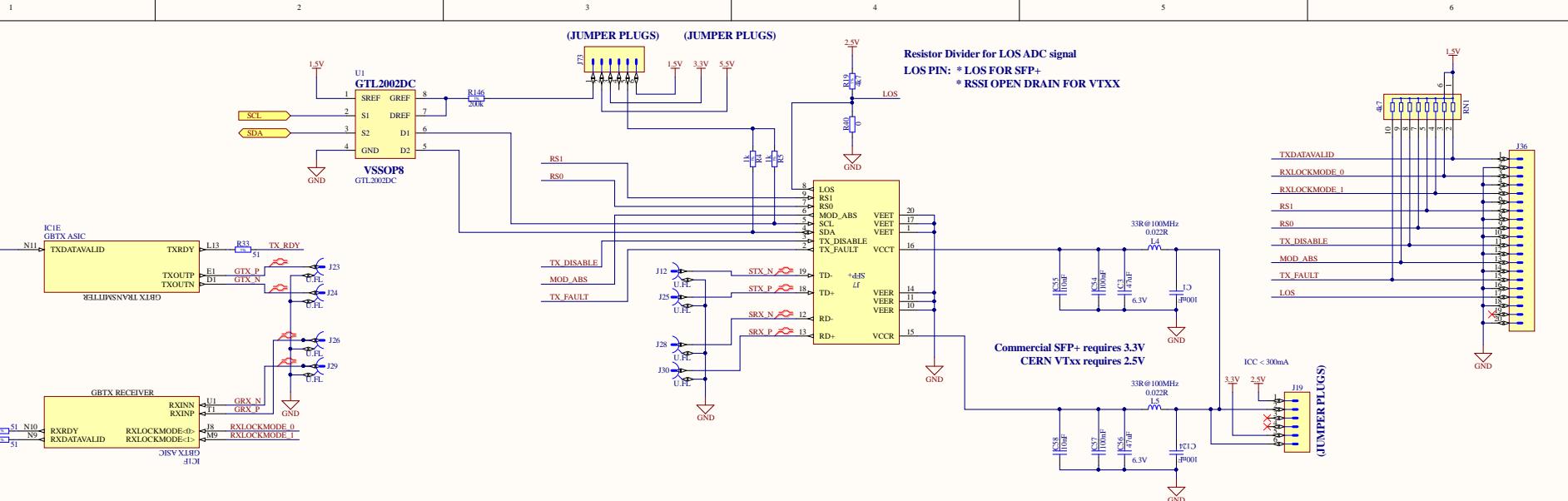


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Date: 6/17/2019	Sheet of	
File: C:\Users...\GBTx_ALL_PORTS.SchDoc	Drawn By:	

O.I SATS XLRD



Title		
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Date: 6/17/2019	Sheet of	
File: C:\Users...\HDMI_Breakout.SchDoc	Drawn By:	



#### 4 Pin assignment and function

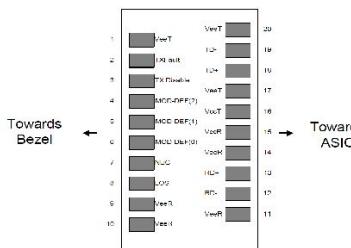


Figure 3. Pin assignment

Pin number	Name	Function	Plug sequence*	Note
1	VeeT	Transmitter ground	1	
2	TXFault	Transmitter fault indication	3	
3	TXDisable	Transmitter disable input	3	Module disables on high or open
4	MOD-DEF2	Module definition 2	3	2 wire serial ID and interface
5	MOD-DEF1	Module definition 1	3	2 wire serial ID and interface
6	MOD-DEF0	Module definition 0	3	Grounded internally via 100ohm
7	NUC	No user connection	3	Reserved for future use
8	LOS	Loss of signal indication	3	
9	VeeR	Receiver ground	1	
10	VeeR	Receiver ground	1	
11	VeeR	Receiver ground	1	
12	RD-	Negative receiver Data out	3	
13	RD+	Positive receiver Data out	3	
14	VeeR	Receiver ground	1	
15	VccR	Receiver power	2	
16	VccT	Transmitter power	2	
17	VeeT	Transmitter ground	1	
18	TD+	Positive transmitter Data in	3	
19	TD-	Negative transmitter Data in	3	
20	VeeT	Transmitter ground	1	

\*Plug sequence: Pin engagement sequence during hot plugging.

SFP+ Connector can be populated with several options:

- 1) VTTx
- 2) VTRx
- 3) Industry std SFP+ Tx/Rx
- 4) Copper SFP+ interface cable

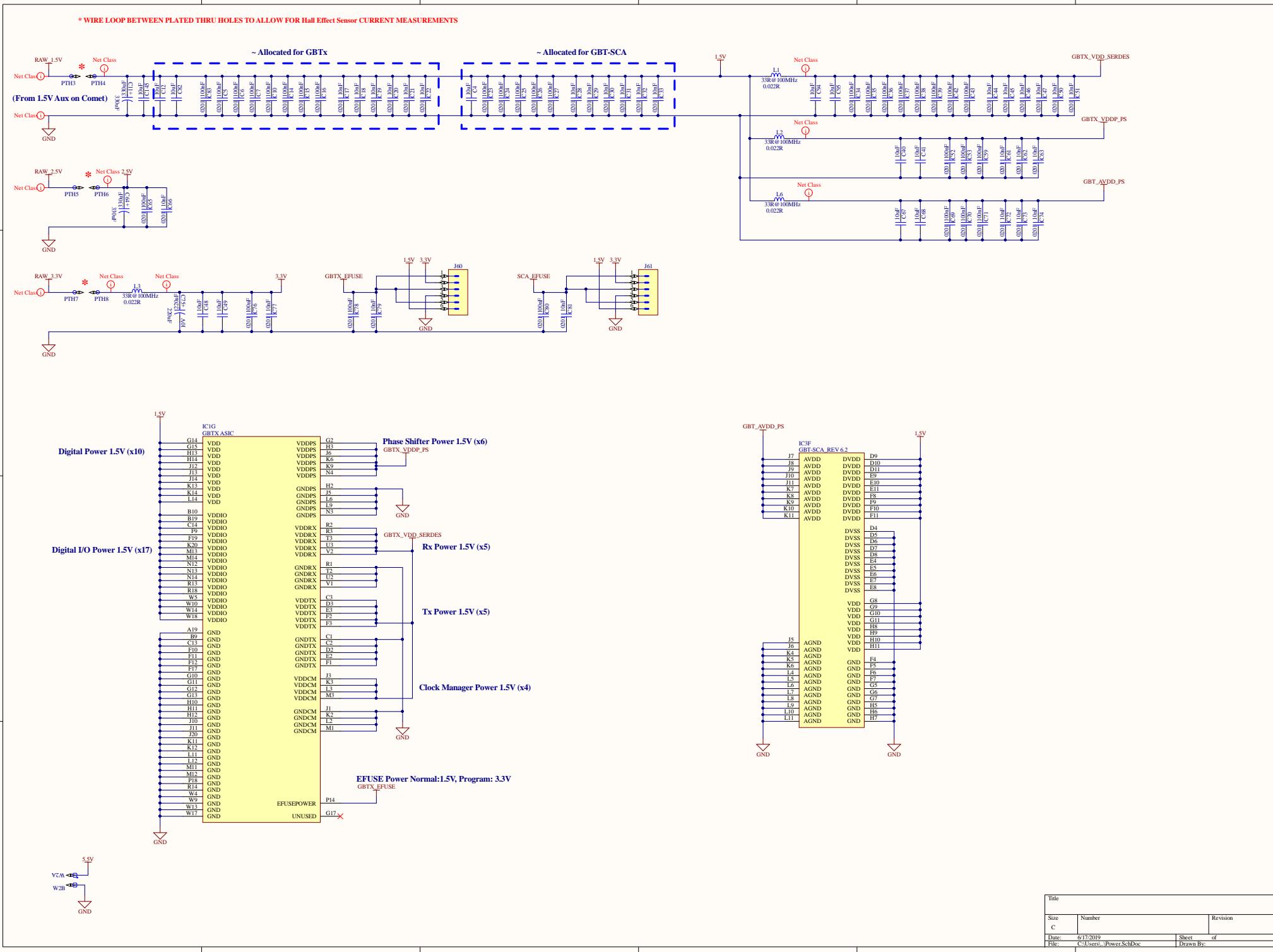
There are only 2 functional applications:

- a) single Tx using either VTTx, VTRx, or SFP+  
Unused Tx channel to be jumper configured with failsafe jumper resistors for DC coupled or 320 MHz clock if module contains internal AC coupling capacitors. This allows thermal evaluation.
- b) Standard Tx/Rx using either VTRx or SFP+  
The I2C of Commercial SFP+ modules must be provided by the COMET FPGA using 3.3V pullups.  
The I2C of CERN VTxx modules must be provided by the GBTx using 1.5V pullups.

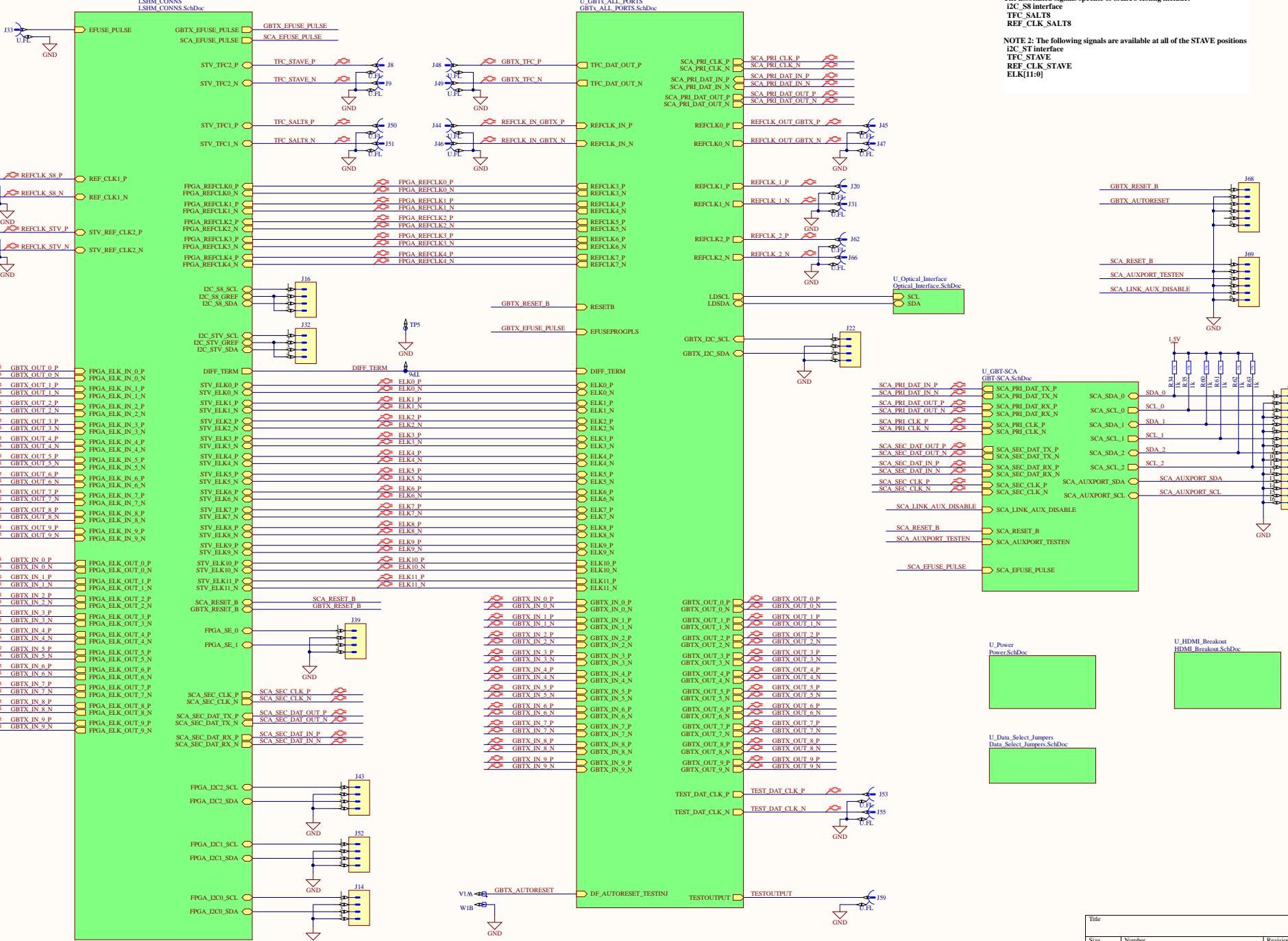
Title		
Size C	Number	Revision
Date: 6/17/2019		Sheet of
File: C:\Users\Optical Interface SchDoc		
Drawn By:		

1 2 3 4 5 6

\* WIRE LOOP BETWEEN PLATED THRU HOLES TO ALLOW FOR Hall Effect Sensor CURRENT MEASUREMENTS

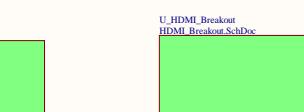
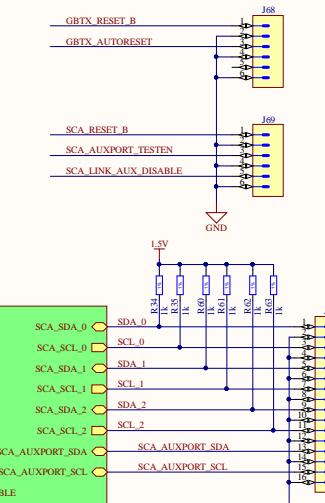


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Date: 6/17/2019 File: C:\Users...\Power.SchDoc	Sheet of	Drawn By:

**U.FL CONNECTORS CONNECTED TO THE STAVE VIA ERX8**


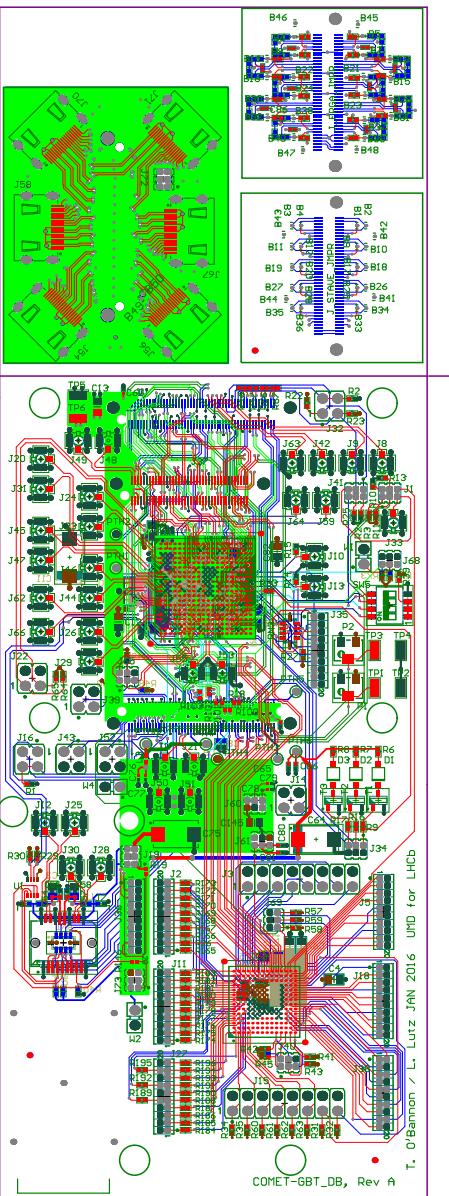
Note 1: The SALTB test board ERX8 connector signal-pins assignments restrict the location to the furthest out STAVE position.  
The associated signals specific to SALTB testing include:  
12C\_SS interface  
TFC\_STAVE  
TFC\_SALTB  
REF\_CLK\_STAVE  
REF\_CLK\_SALTB

Note 2: The following signals are available at all of the STAVE positions  
12C\_SS interface  
TFC\_STAVE  
REF\_CLK\_STAVE  
ELK[11:0]



Title			
Size	Number	Revision	
Date:	6/17/2019	Sheet	of
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NOTE: Upper three board areas outlined in silkscreen need to be separated after assembly. Outer dimensions of these three board outlines are not critical. Upper left corner to be separable for discard.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Assembly Overlay	Overlay				
IPC-A-610E Class 2	Solder Mask/Coverlay	Surface Material	0.8	Solder Resist	3.5
ROHS					
Top Solder	Top Layer 1	Copper	1.7		
Fabrication requirement	Dielectric	Prepreg	3.9	370HR	4.2
Internal plane 2	Internal Plane	Copper	0.7		
0.07 inch Nominal Thickness					
1/2 Dielectric Inner and Outer Layers	Dielectric	Core	6		4.2
ENIG Finish	Signal Layer 3	Copper	0.7		
Electrical testing required	Dielectric	Prepreg	6.8		4.2
Internal plane 4	Internal Plane	Copper	0.7		
Dielectric	Dielectric	Core	6		4.2
NOTE: 5.480 inch dimension is critical at point for outer 0.500 inch extent on both sides to provide additional clearance with components on mating board during assembly. Please avoid placing mouse bites in either those Internal Plane 6 and Internal Plane 7.	Signal Layer 5	Copper	0.7		
Dielectric	Dielectric	Prepreg	6.8		4.2
Internal Plane 6	Internal Plane	Copper	0.7		
Dielectric	Dielectric	Core	6		4.2
Internal Plane 7	Internal Plane	Copper	0.7		
Dielectric	Dielectric	Prepreg	6.8		4.2
Signal Layer 8	Signal	Copper	0.7		
Dielectric	Dielectric	Core	6		4.2
Internal Plane 9	Internal Plane	Copper	0.7		
Dielectric	Dielectric	Prepreg	6.8		4.2
Signal Layer 10	Signal	Copper	0.7		
Dielectric	Dielectric	Core	6		4.2
Internal Plane 11	Internal Plane	Copper	0.7		
Dielectric	Dielectric	Prepreg	3.9		4.2
Bottom Layer 12	Signal	Copper	1.7		
Bottom Solder	Solder Mask/Coverlay	Surface Material	0.8	Solder Resist	3.5
Bottom Overlay (13)	Overlay				