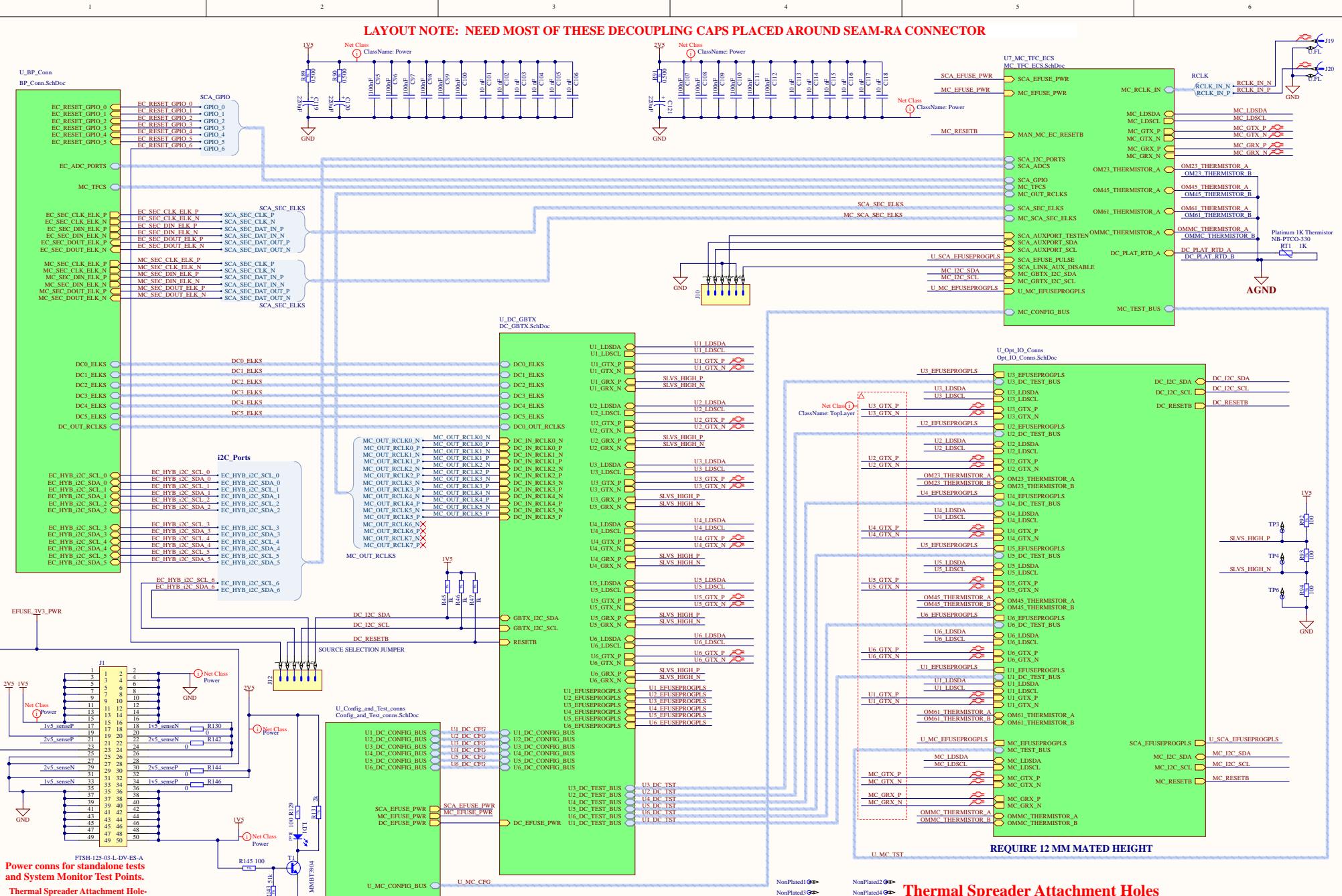


LAYOUT NOTE: NEED MOST OF THESE DECOUPLING CAPS PLACED AROUND SEAM-RA CONNECTOR



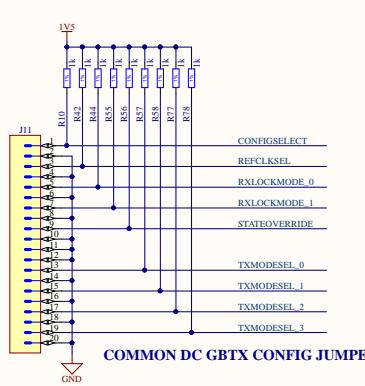
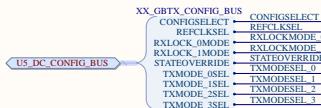
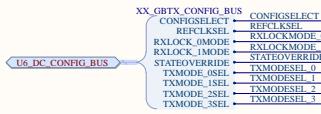
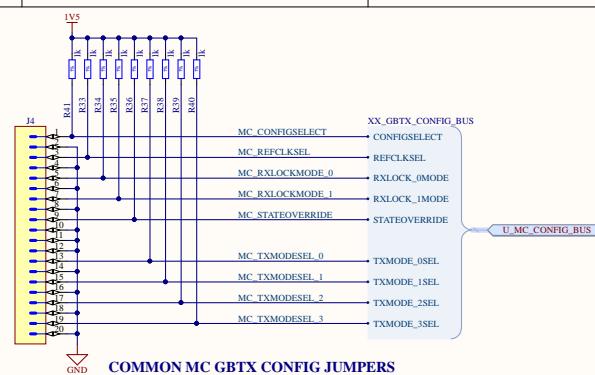
Notes:

- (1) Pinout symmetrical which support either mate orientation.
- (2) Net Class: ClassName: TopLayer---Must be routed on the top side only without using any vias.
- (3) ~15mm of OUTER PCB EDGES (+ addl 5 mm for aluminum heat sink plate) ARE ALLOCATED FOR HEAT PIPES.
- (4) Circuit side of the board has 2mm thick aluminum heat sink plate. Pockets will be milled for small decoupling caps (0201 and 0402 only) to be located under the GBT components. Aluminum heat sink plate extends ~5mm beyond each card guide edge of the PCB.
If the PCB is fully supported only via the aluminum heat sink edges when installed in the card cage.

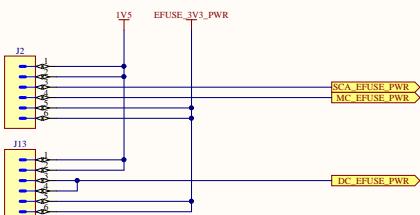
Combined_DC_MCB_Project.Pcb

Title Data Control Board (DCB) Schematic		
Size C	Number Top Combined DC + MCB Hierarchy	Revision A
Date: 7/9/2018	Sheet of 10	A
File: D:\UT...\Top_Combined_DC_MCB.SchDoc	Drawn By: Tom O'Bannon	

A



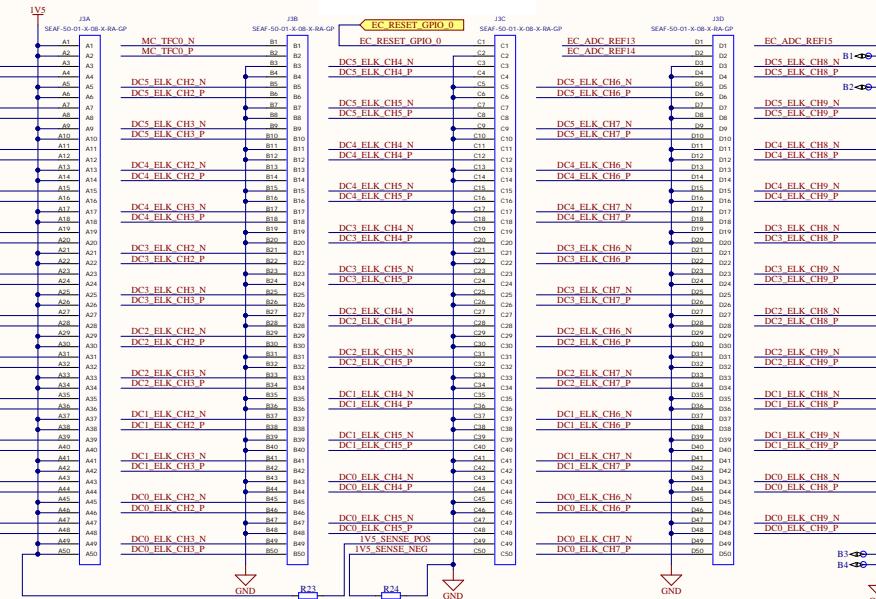
COMMON DC GBTX CONFIG JUMPERS



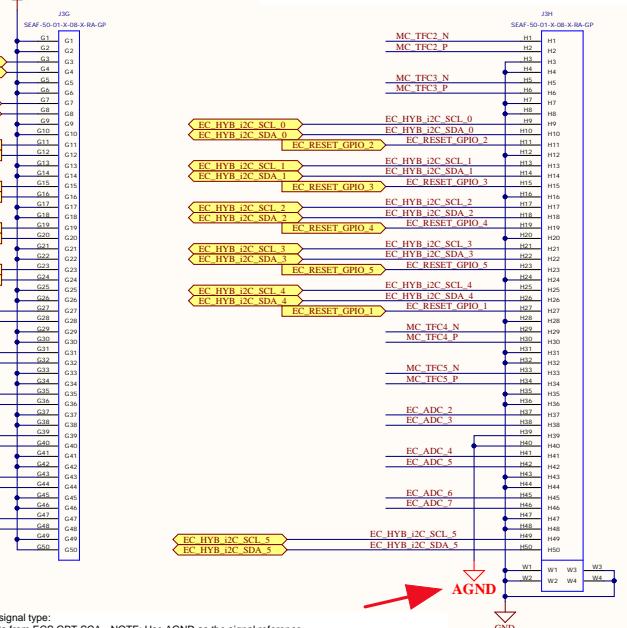
Title Data Control Board (DCB) Schematic		
Size C	Number Config_and_Test_conn.SchDoc	Revision A
Date: 7/9/2018	Sheet 9 of 10	
File: D:\UT\...\Config_and_Test_conn.SchDoc	Drawn By: Tom O'Bannon	

LAYOUT NOTE: NEED DECOUPLING CAPS PLACED AROUND SEAM-RA

72 links (6 GBTx-DC x 12)



LAYOUT NOTE: Place Sense lines near center of Board.



x6 sets of signals for each signal type.

EC_ADC[7:2]: ADC inputs from ECS GBT-SCA --NOTE: Use AGND as the signal reference.

DC_OUT_RCLK[5:0]: GBTx data concentrator reference clock outputs for the hybrids.

MC_TFC[5:0]: Master control GBTx TFC for hybrids.

EC_RESET_GPIO[5:0]: ECS generated reset from GBT-SCA (Also available as general digital I/O)

EC_HYB_I2C_SDA[5:0]: ECS generated I2C busses for hybrids

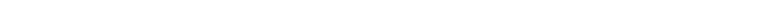
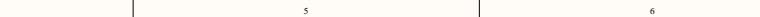
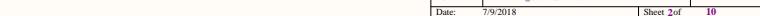
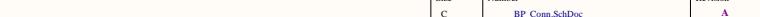
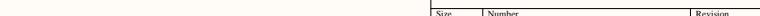
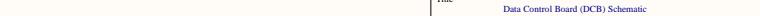
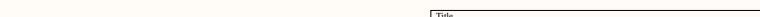
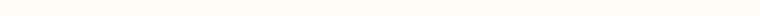
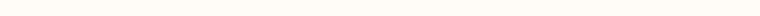
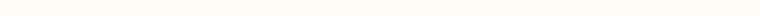
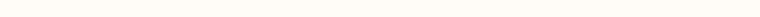
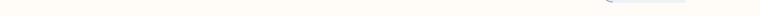
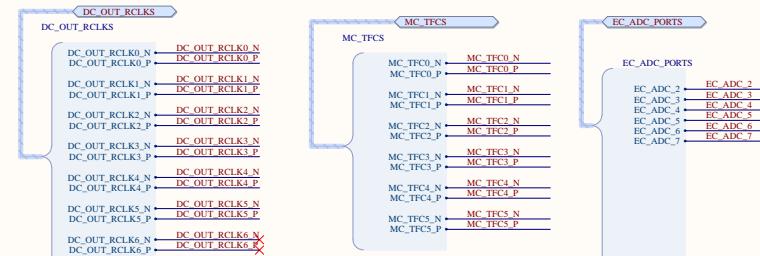
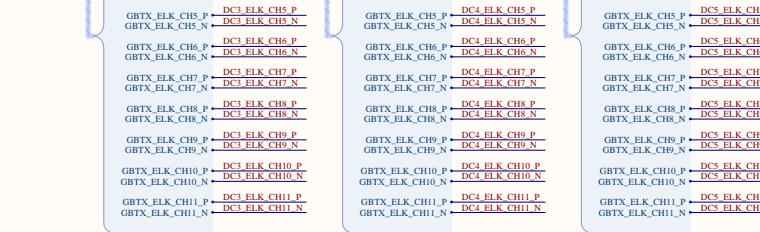
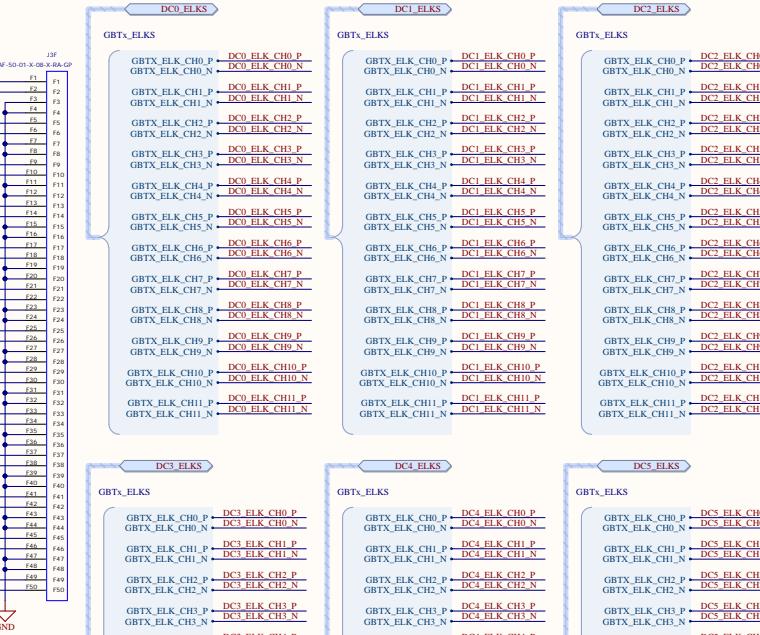
Redundant secondary GBT-SCA control ports:

MC_SEC_ELK: Secondary ECS Elink (DIN, DOUT, and CLK) from GBTx-Master for control of adjacent board GBT-SCA

EC_SEC_ELK: Secondary ECS Elink (DIN, DOUT, and CLK) from adjacent board GBTx-Master for control of GBT-SCA

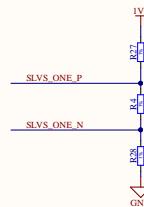
ADC ports for hybrid ground sense measurement:

EC_ADC_xx

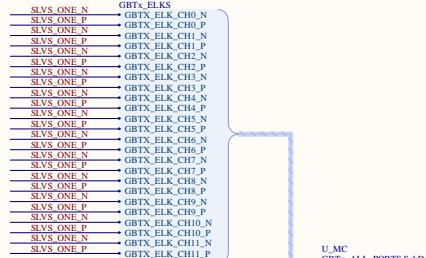


4

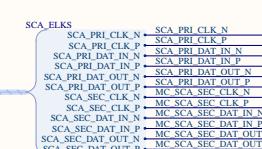
1



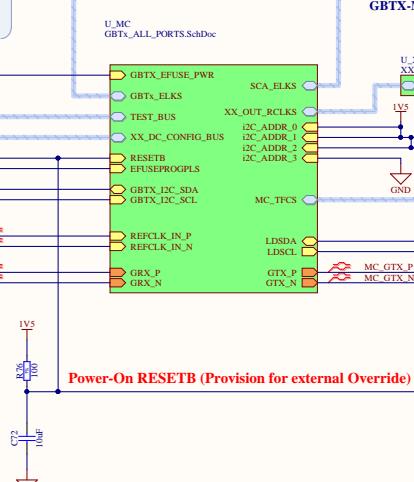
I_C address: Bit<0> has internal pull-up to V_{DDIO}. Bits<3:1> have internal pull-downs to GND



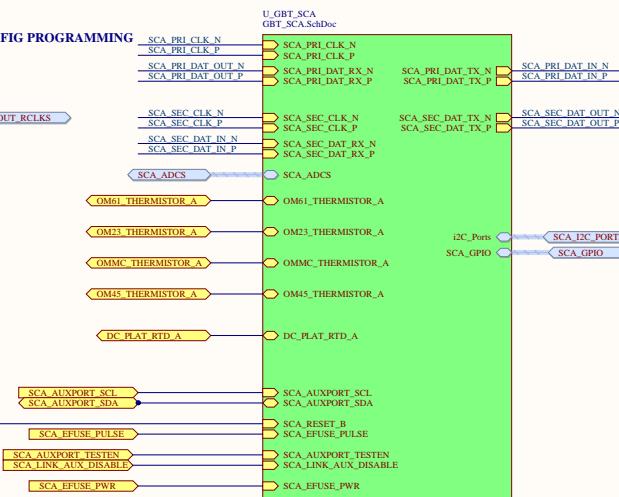
GBTX-MASTER I2c USED ONLY FOR LOCAL CONFIG PROGRAMMING



1

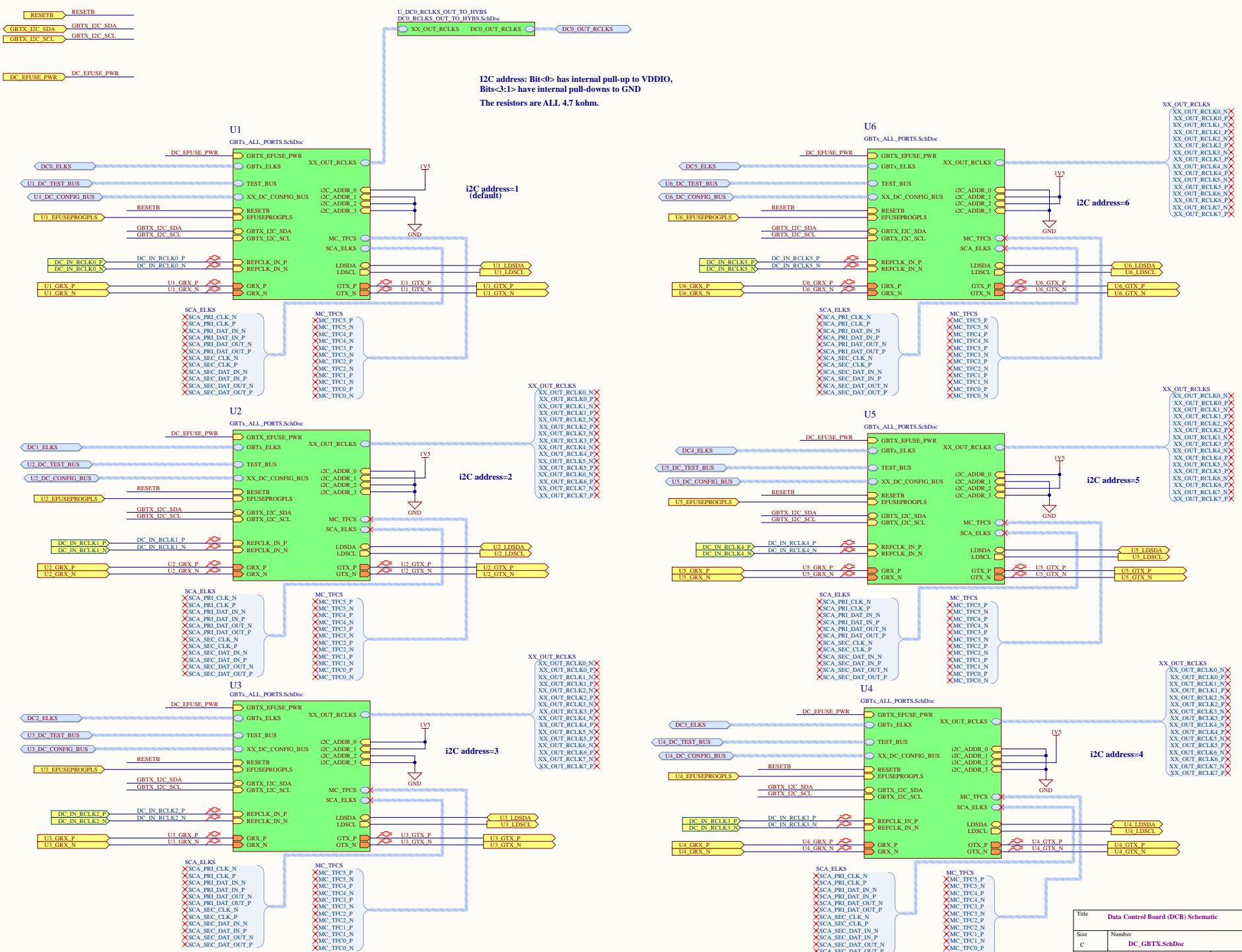


Power-On RESETB (Provision for external Override)



1

Data Control Board (DCB) Schematic		
Size C	Number MC + TFC + ECS - Top Level	Revision A
Date: 7/9/2018	Sheet 3 of 10	
File: D:\UT\MC_TFC_ECS\SchDoc		Drawn By: Tom O'Bannon



A

A

B

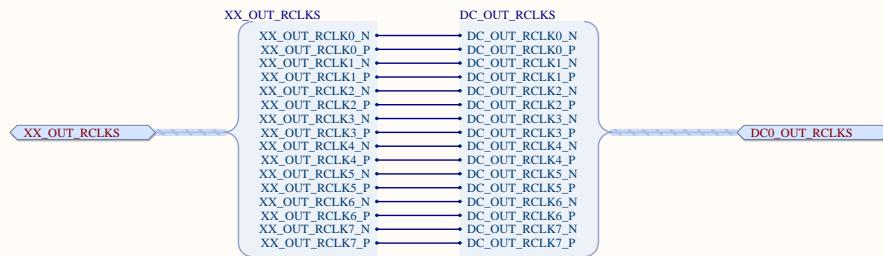
B

C

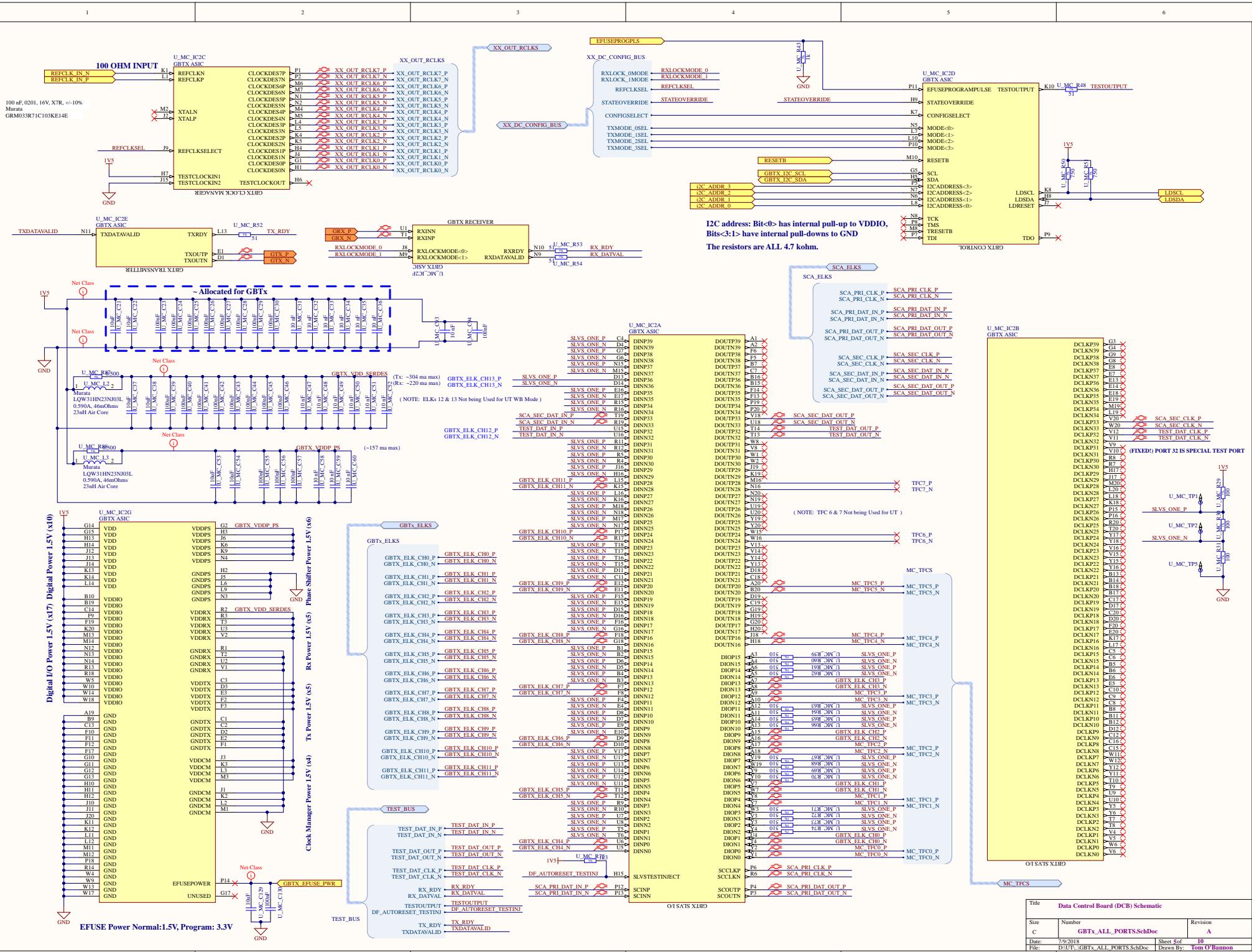
C

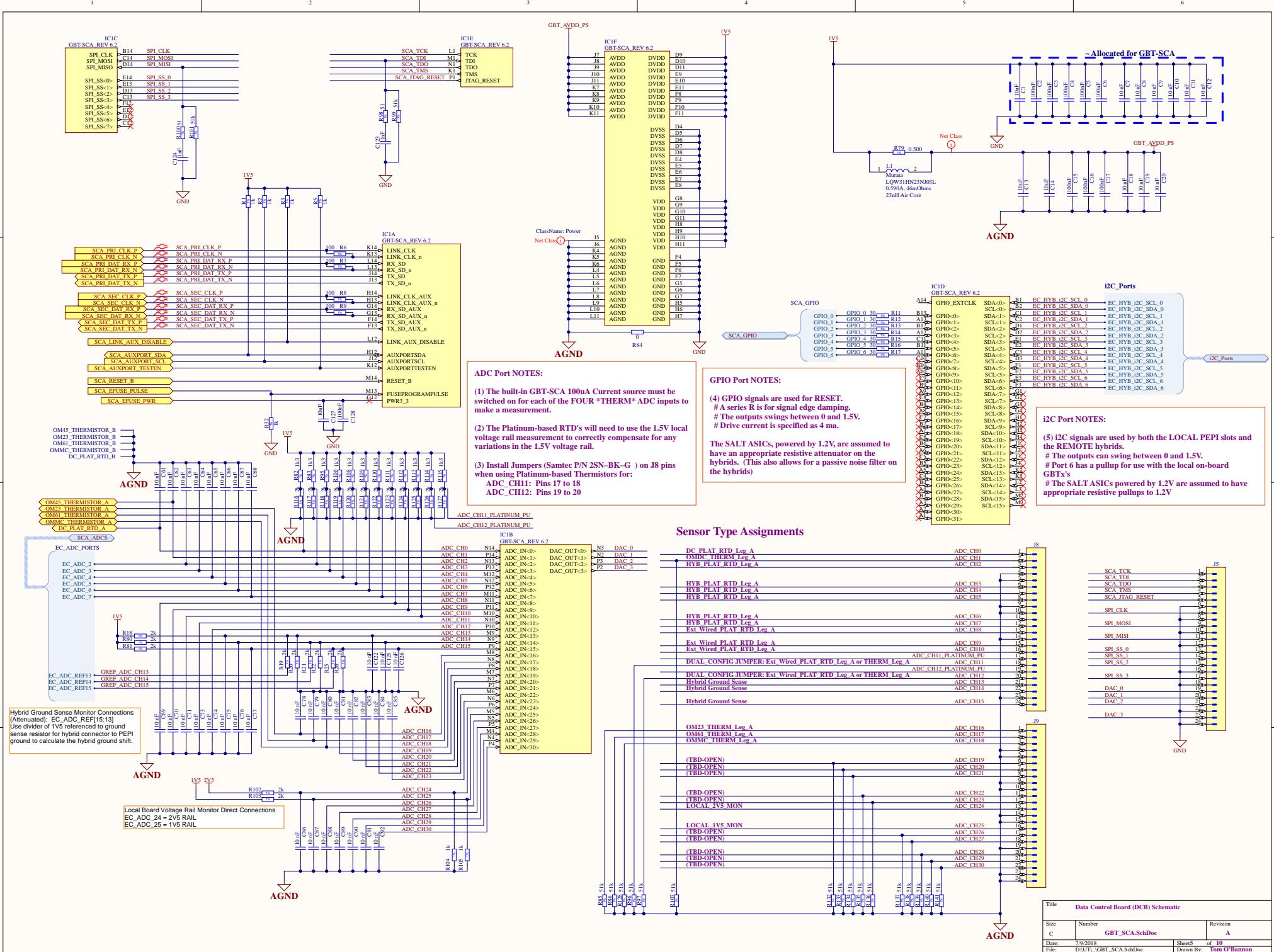
D

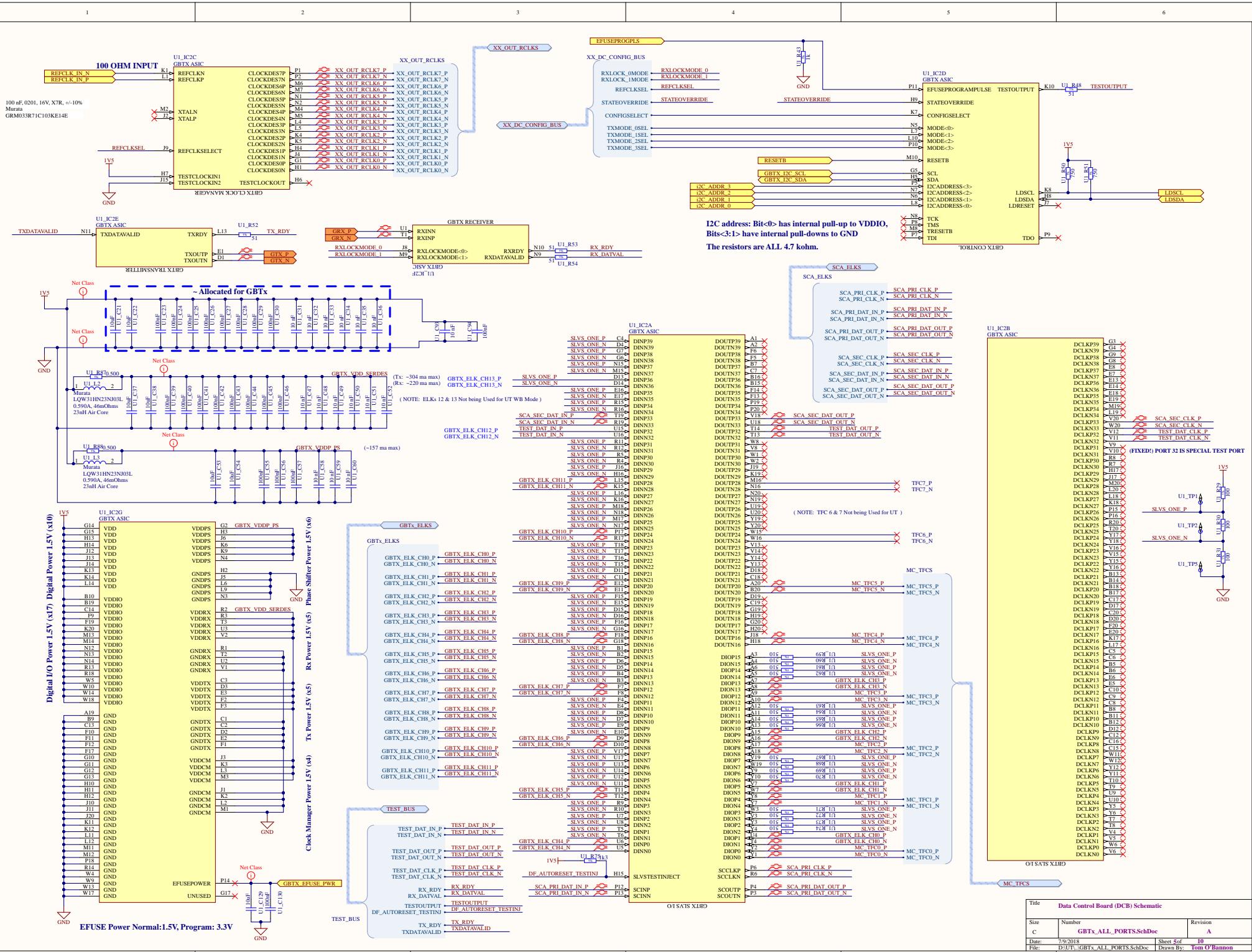
D

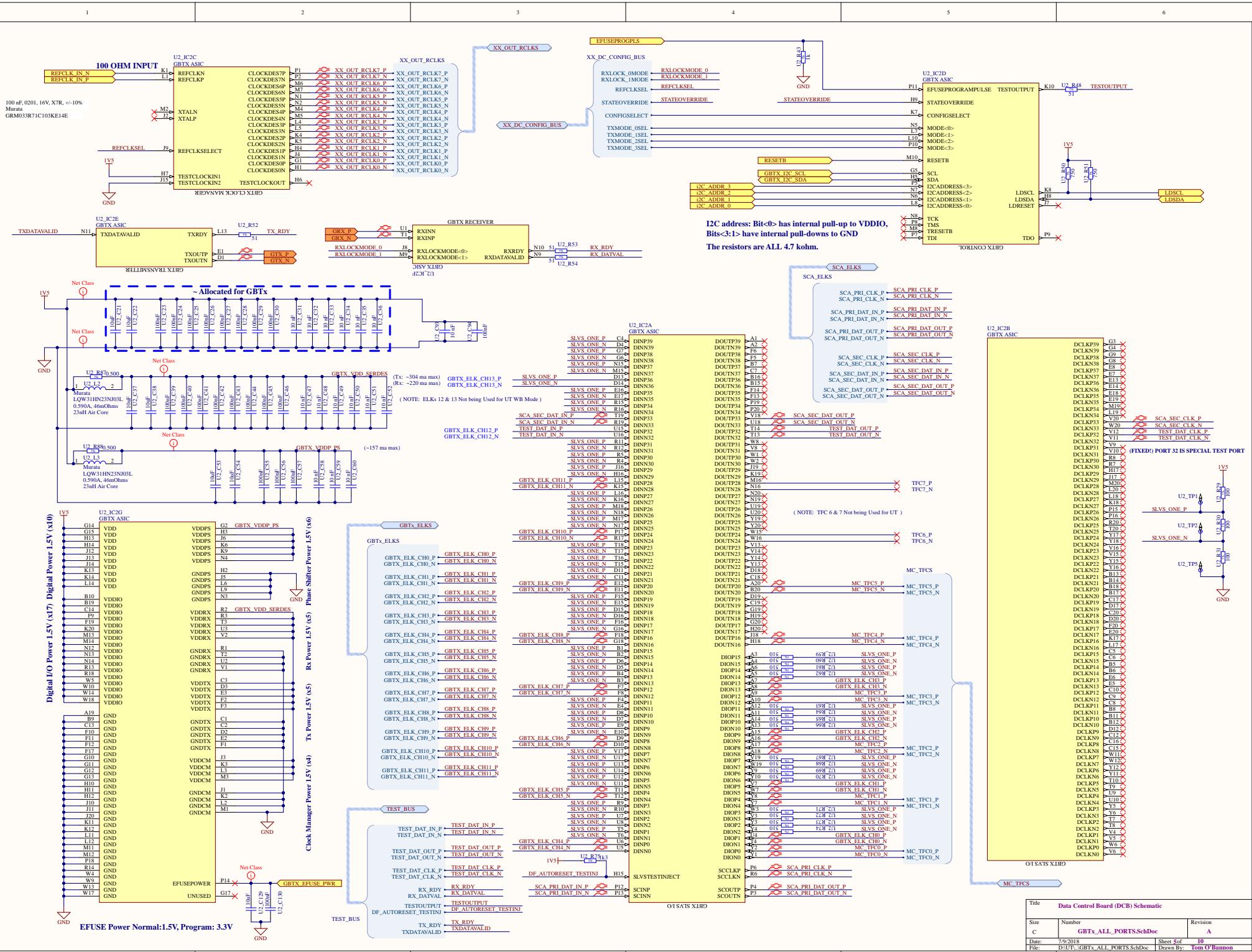


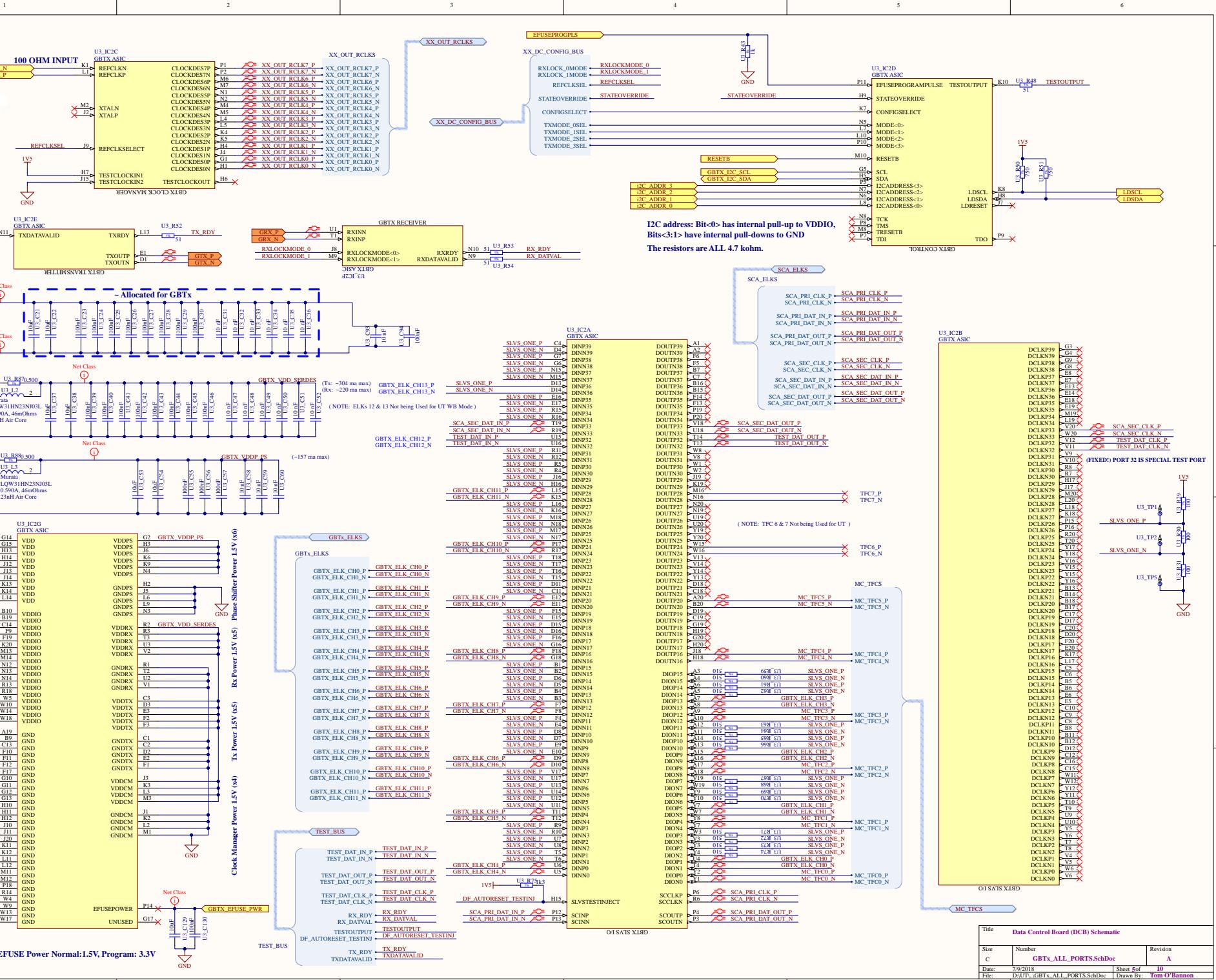
Title Data Control Board (DCB) Schematic		
Size B	Number DCO_RCLKS_OUT_TO_HYBS.SchDoc	Revision A
Date: 7/9/2018	Sheet 8 of 10	File: D:\UT\DCO_RCLKS_OUT_TO_HYBS.SchDoc By: Tom O'Bannon

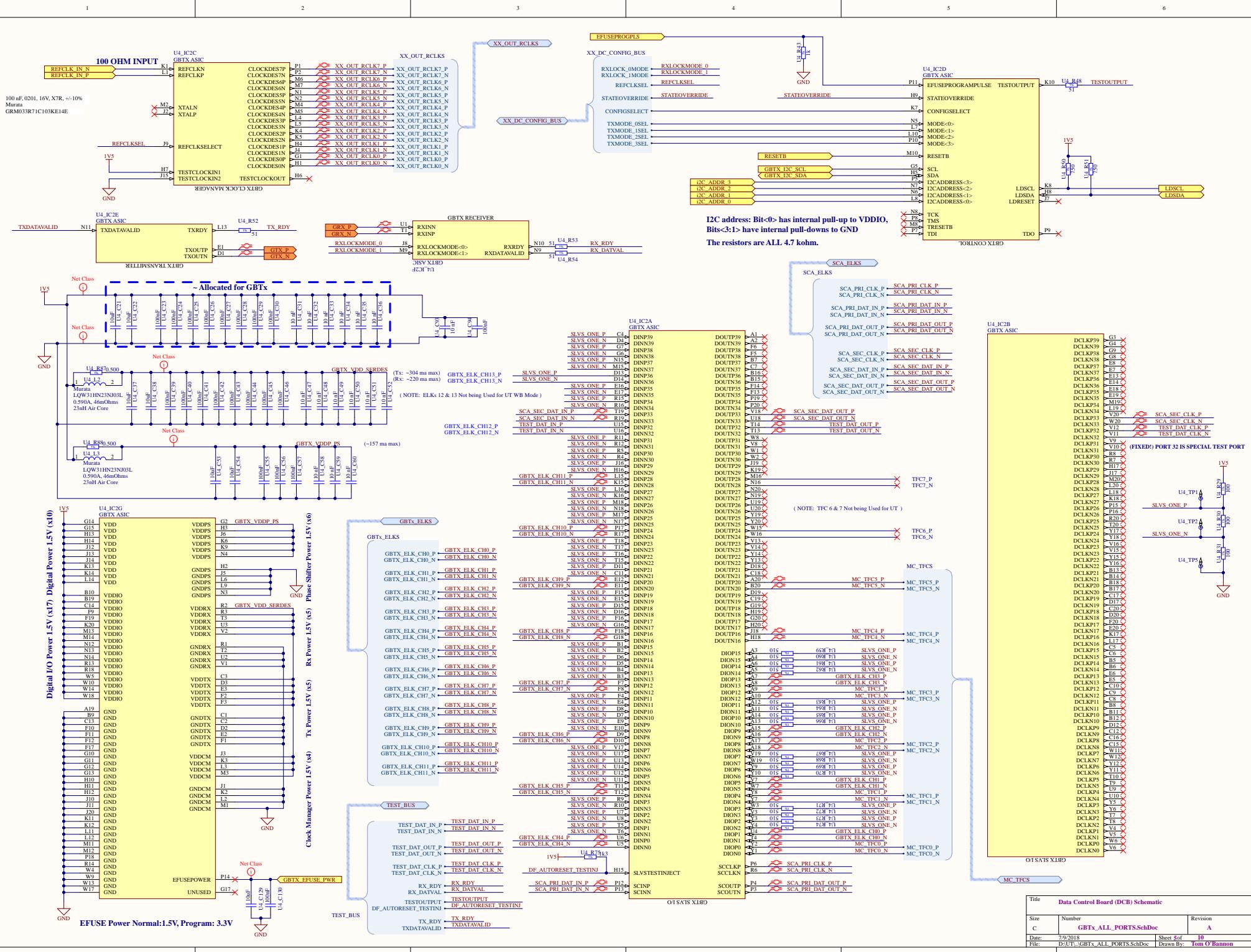


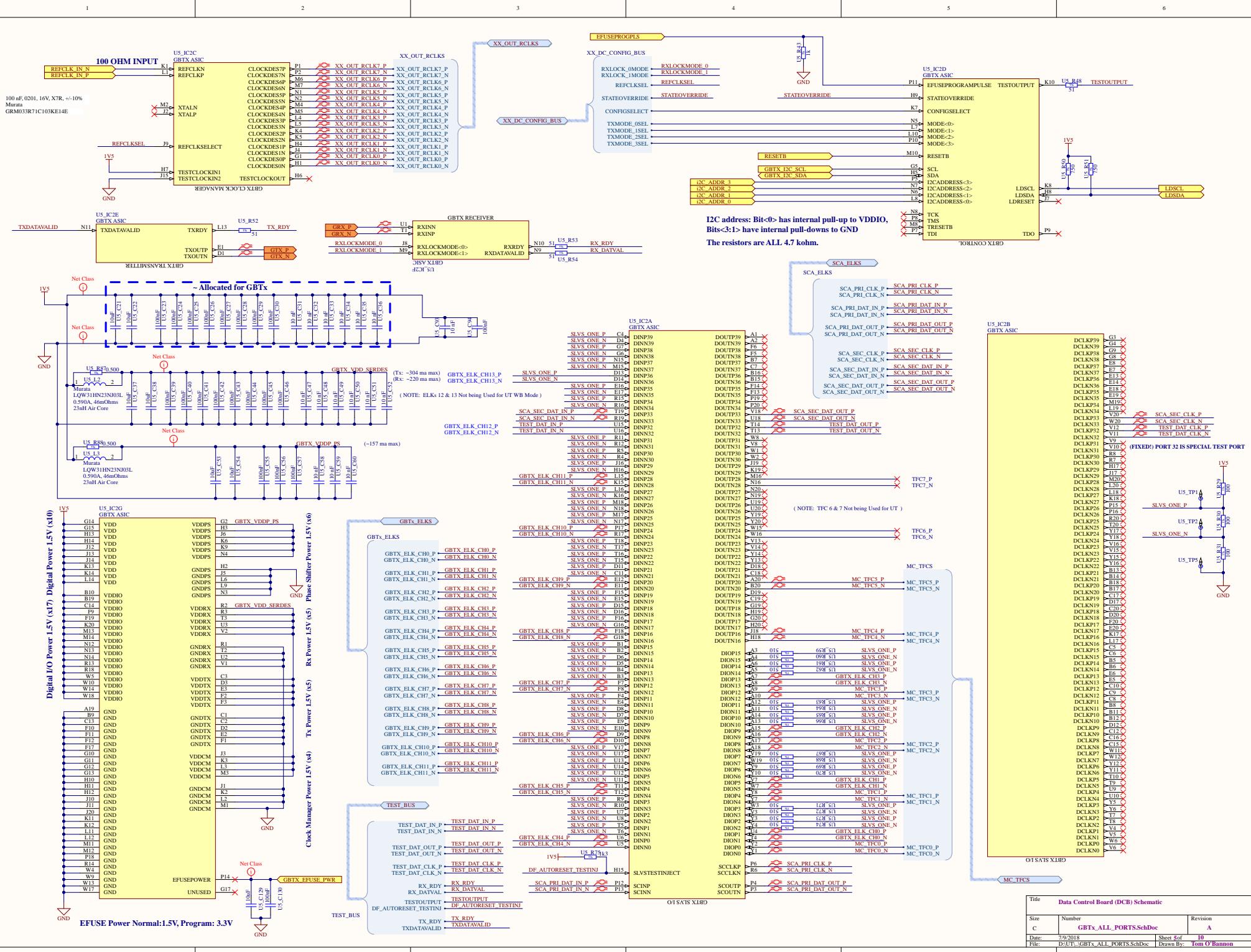


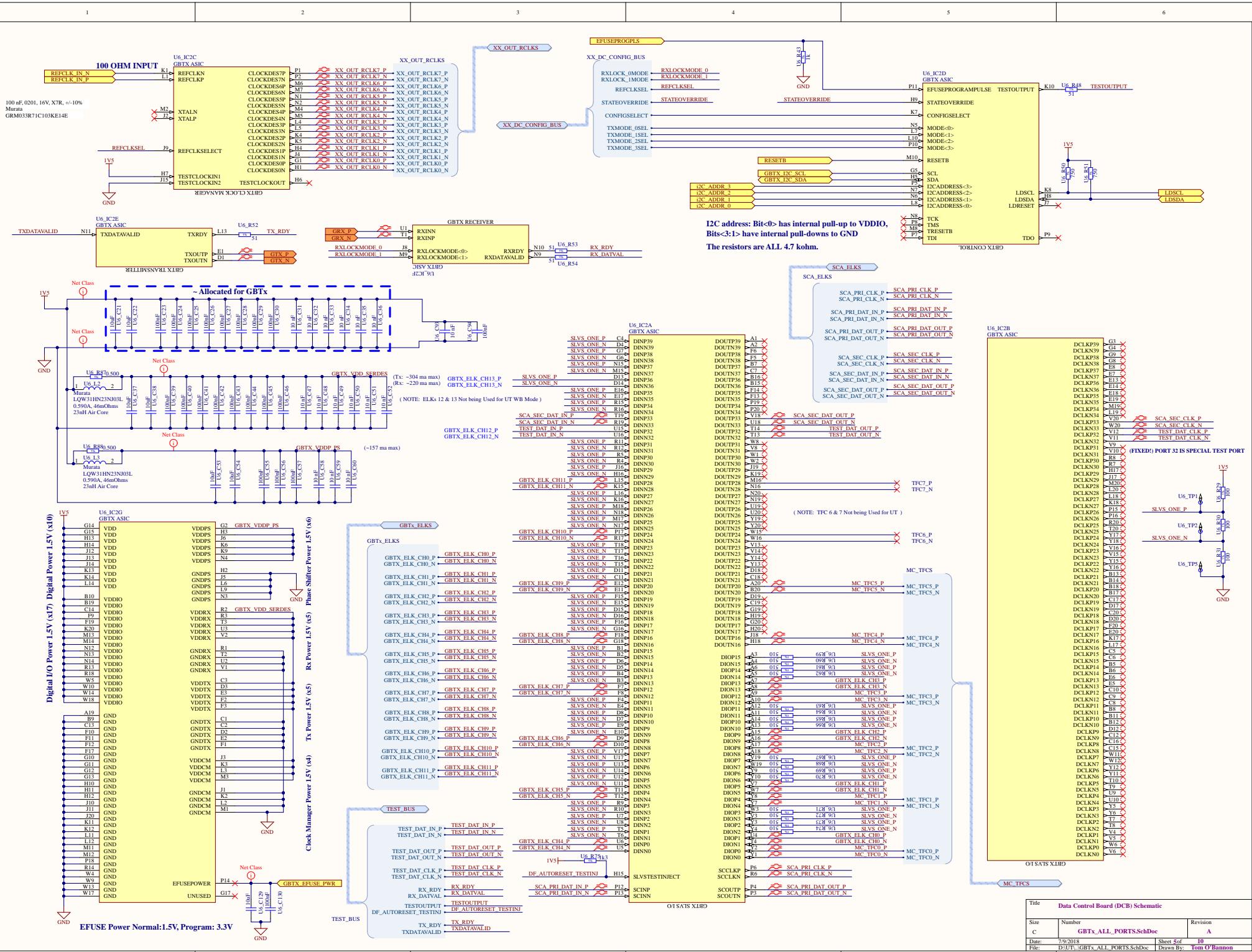


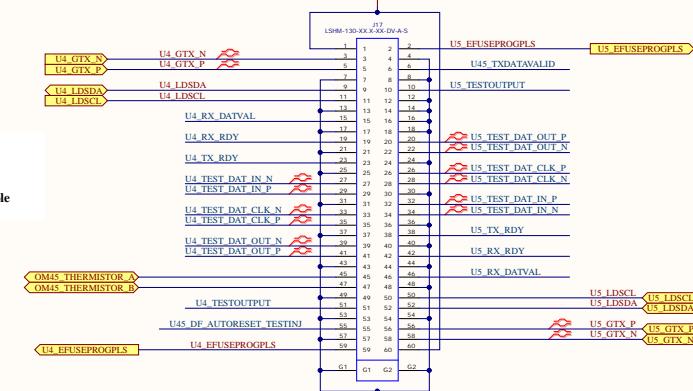
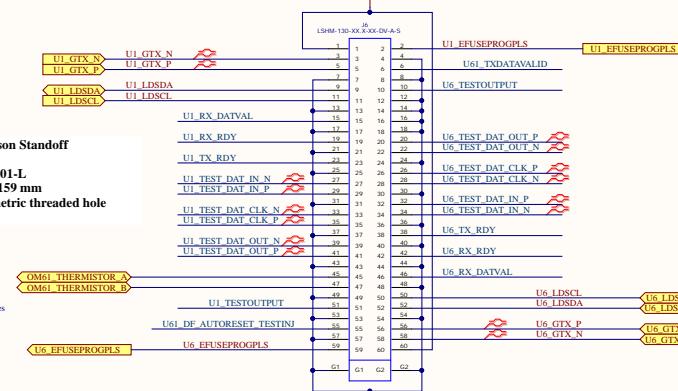
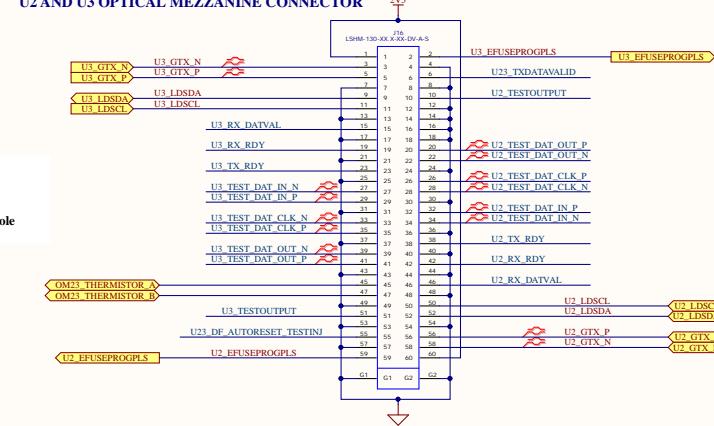
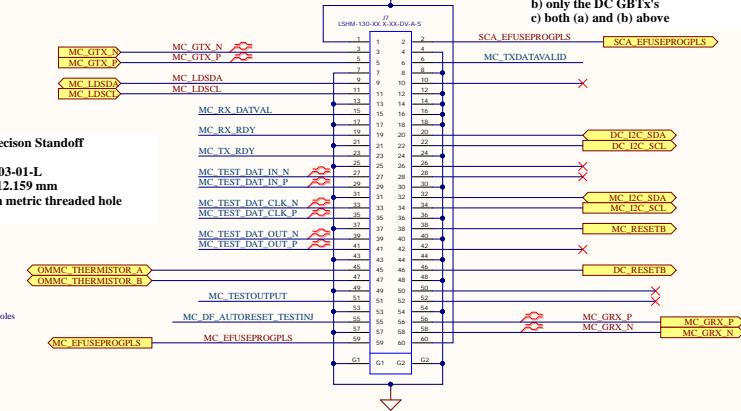










U4 AND U5 OPTICAL MEZZANINE CONNECTOR 2V5**U1 AND U6 OPTICAL MEZZANINE CONNECTOR 2V5****U2 AND U3 OPTICAL MEZZANINE CONNECTOR 2V5****MC OPTICAL MEZZANINE CONNECTOR 2V5**

The UFL connector on the optical mezzanine board can be configured on the DCB to drive:
a) Just the SCA
b) only the DC GBTx's
c) both (a) and (b) above

A

A

B

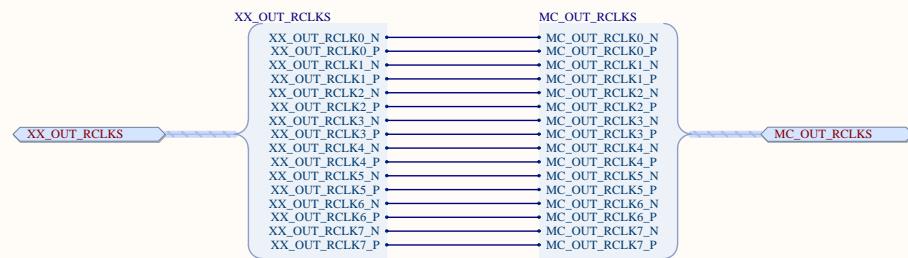
B

C

C

D

D



Title		
Data Control Board (DCB) Schematic		
Size	Number	Revision
B	XX_RCLKS_TO_MC_OUT_RCLKS.SchDoc	A
Date:	7/9/2018	Sheet 6 of 10
File:	D:\UT\XX_RCLKS_TO_MC_OUT_RCLKS.SchDoc	Tom O'Bannon