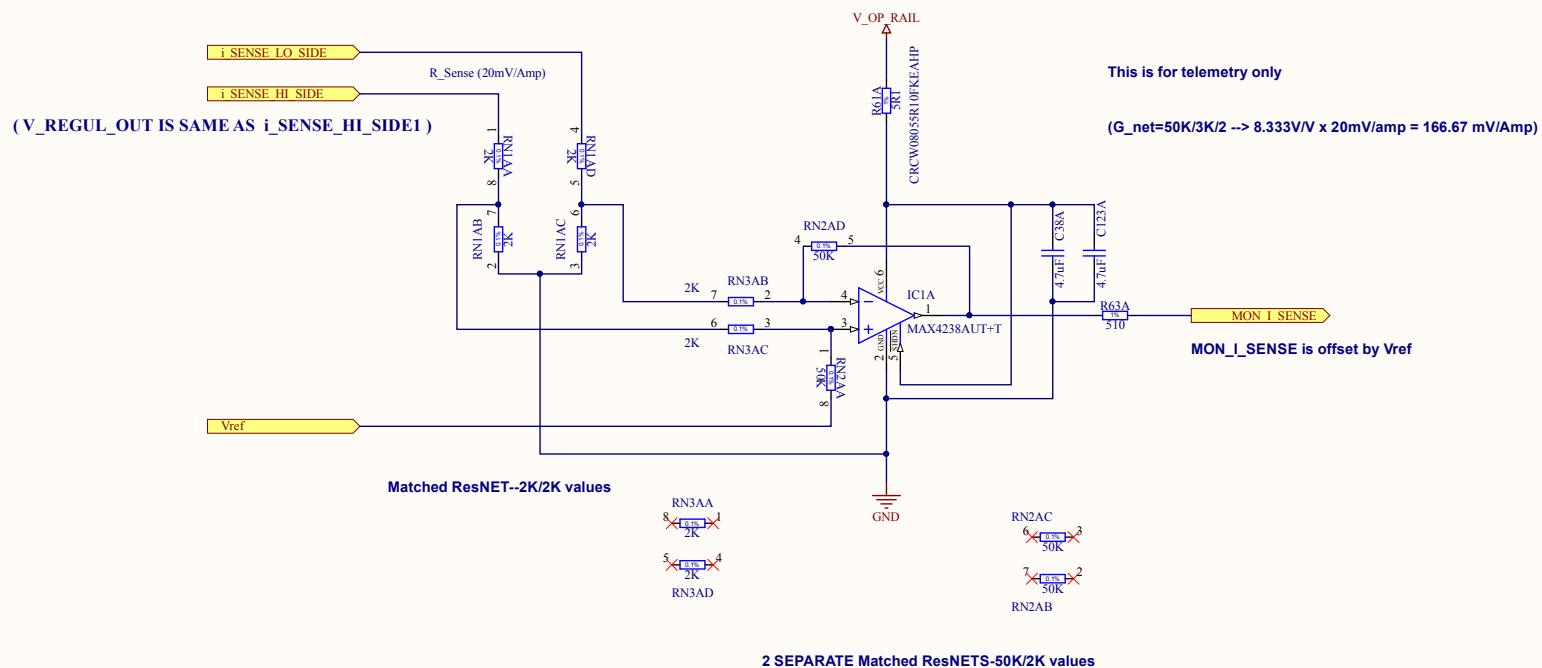
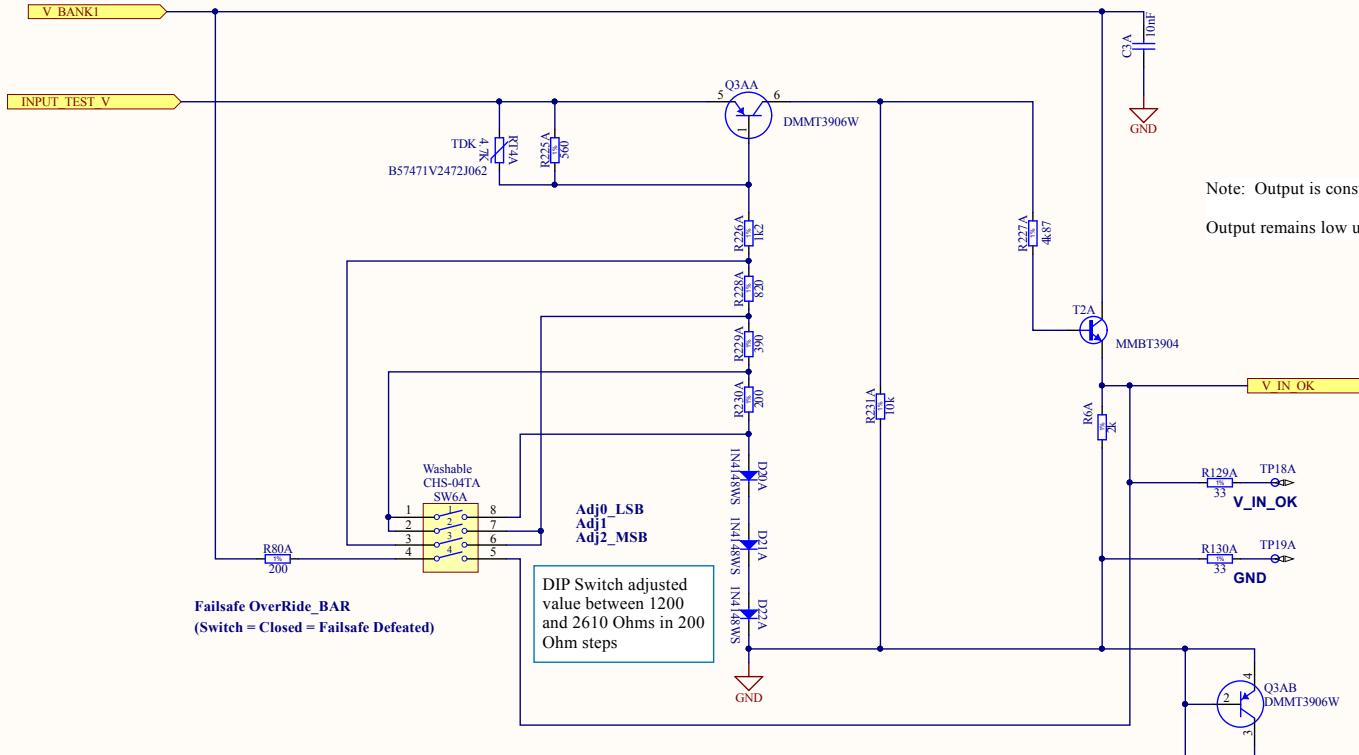


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Size B	Number i-Sense Monitor	Revision A
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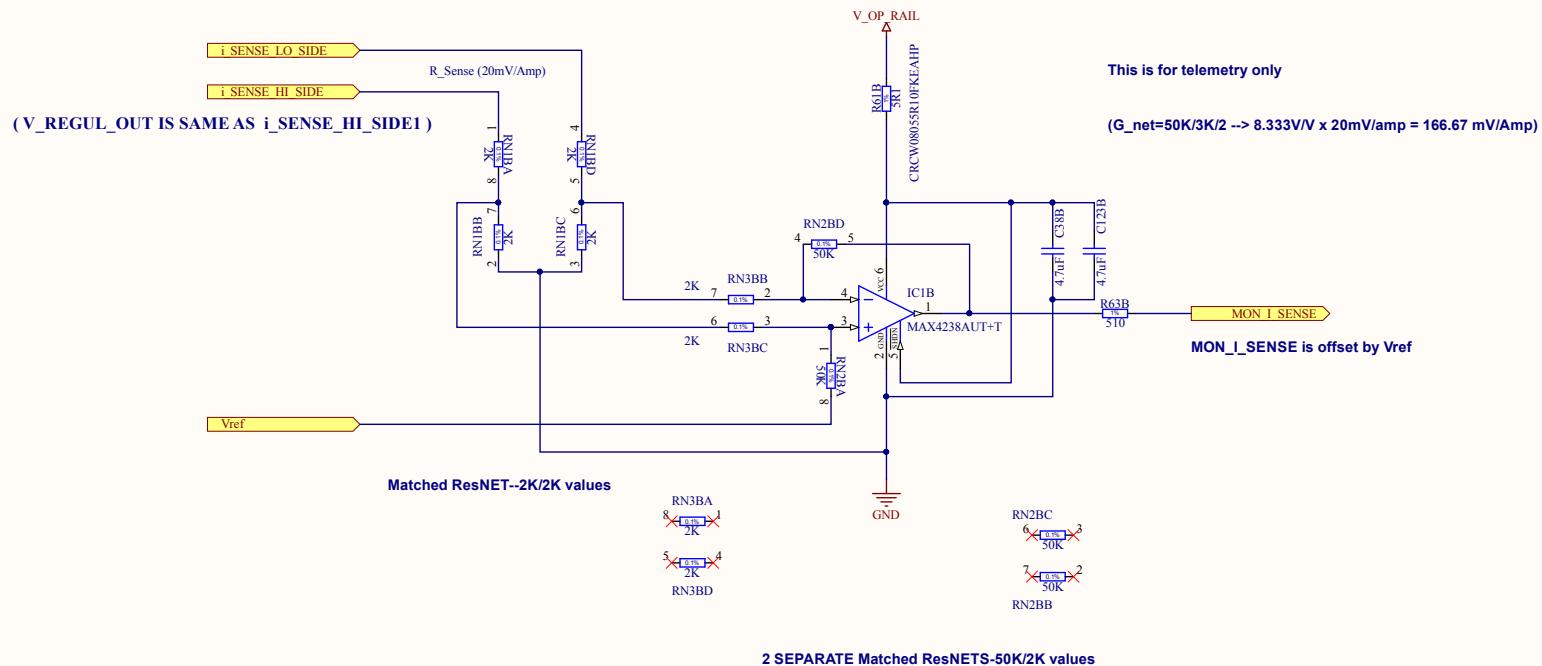
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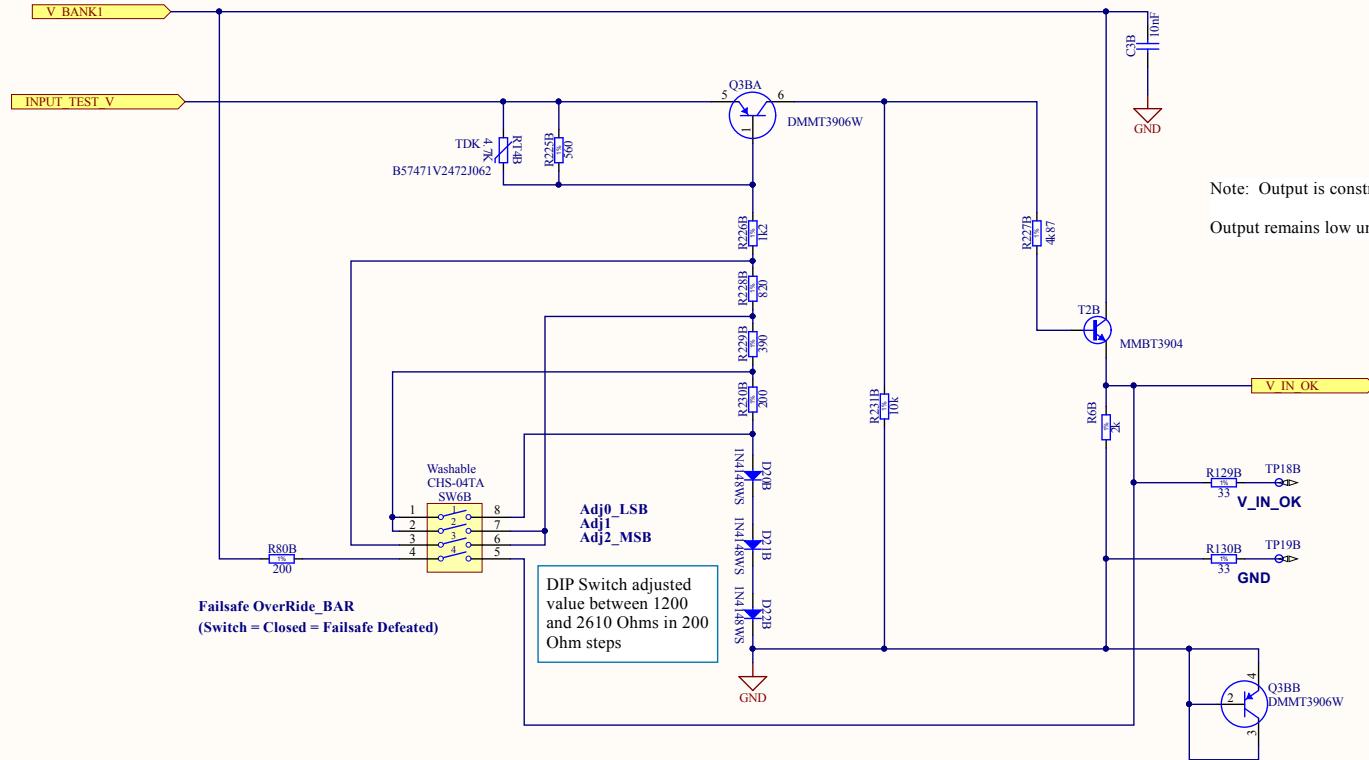
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Size B	Number Under Voltage Lockout (UVL)	Revision A
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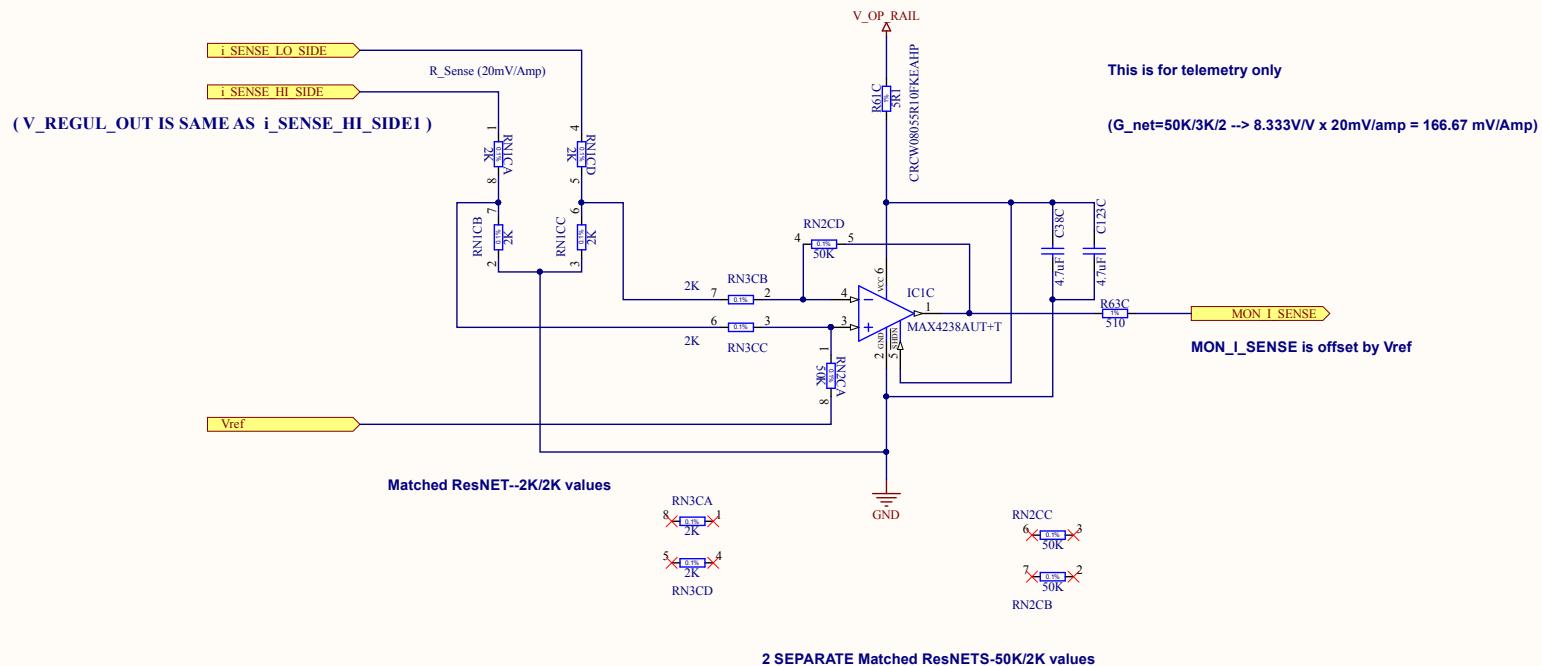


Note: Output is constrained to V_BANK1 max

Output remains low until the input is above the defined threshold

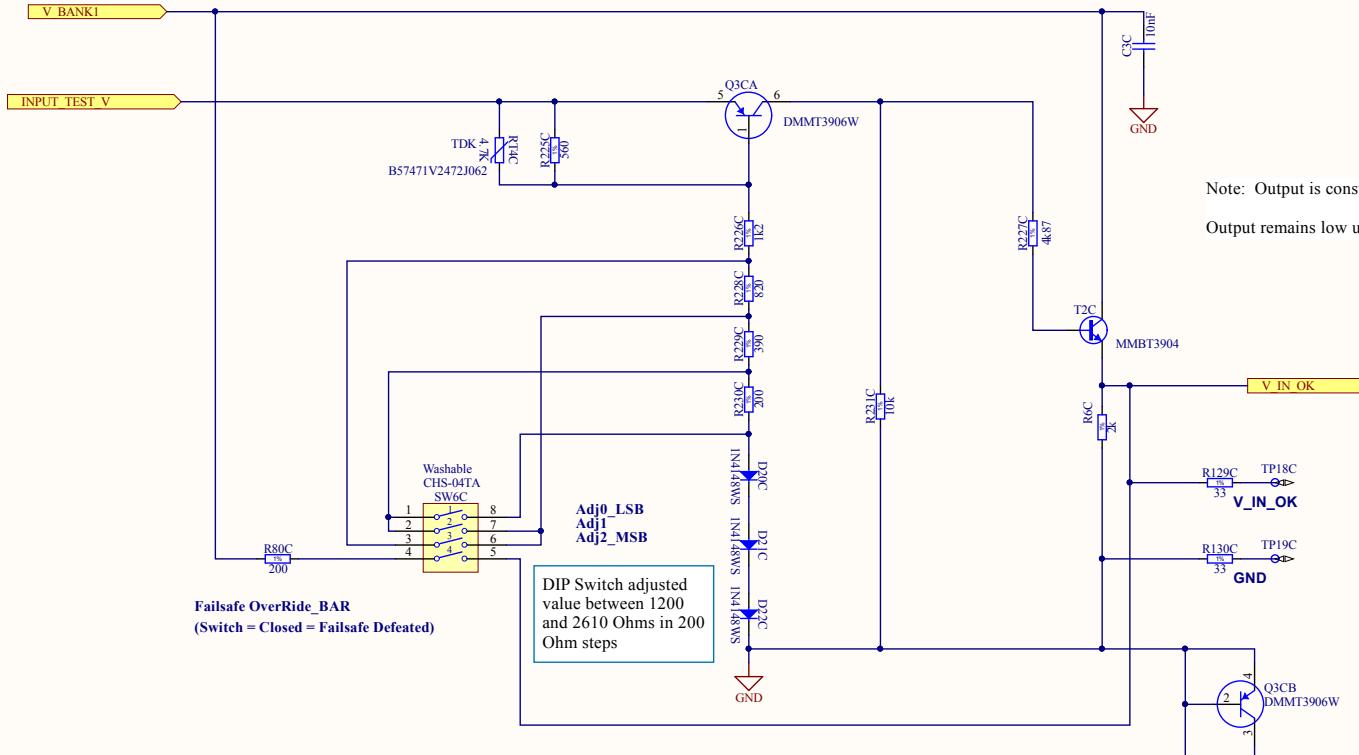
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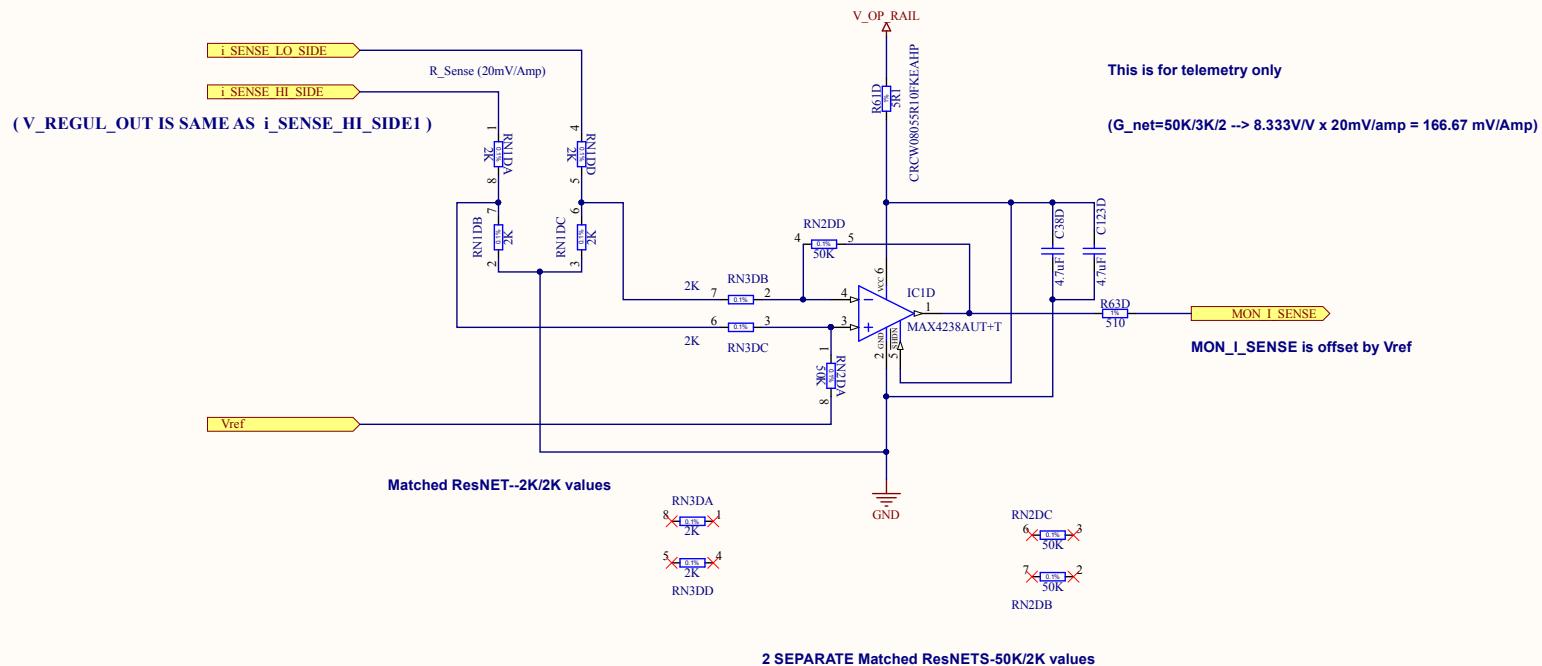
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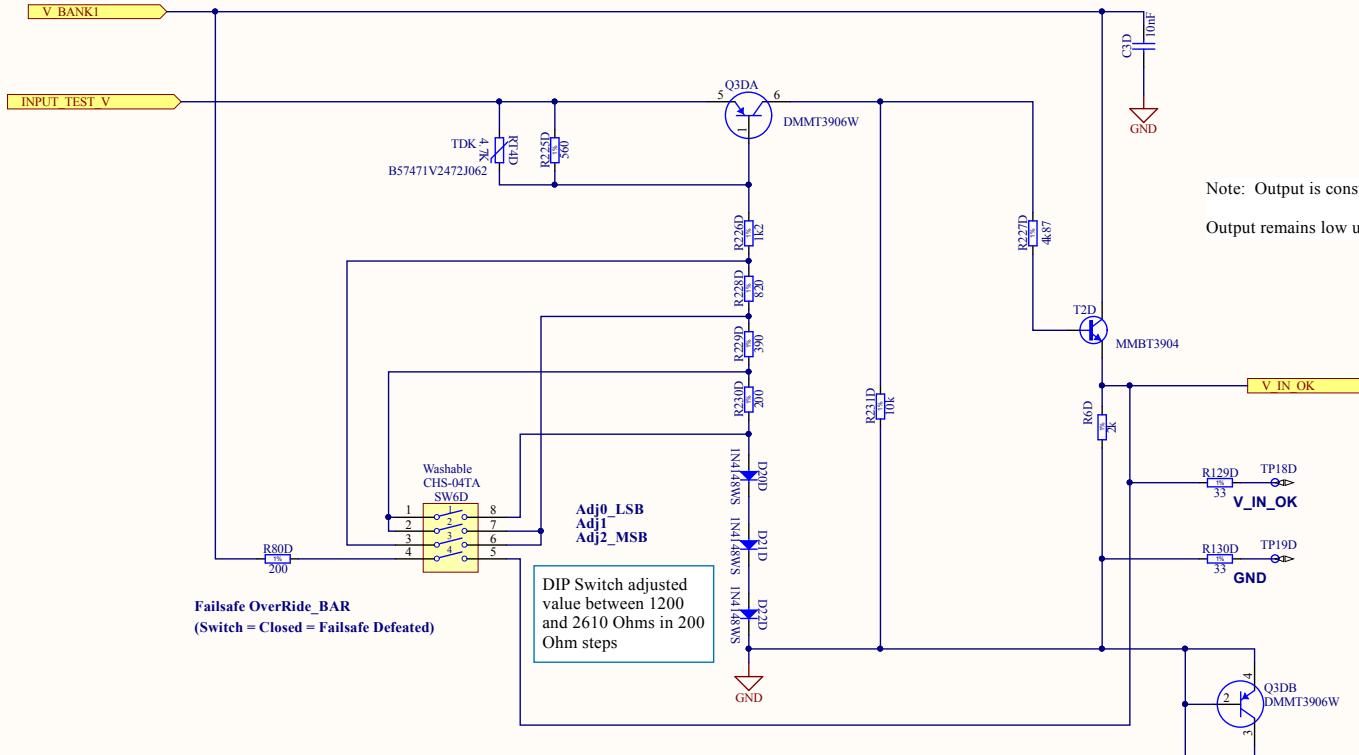
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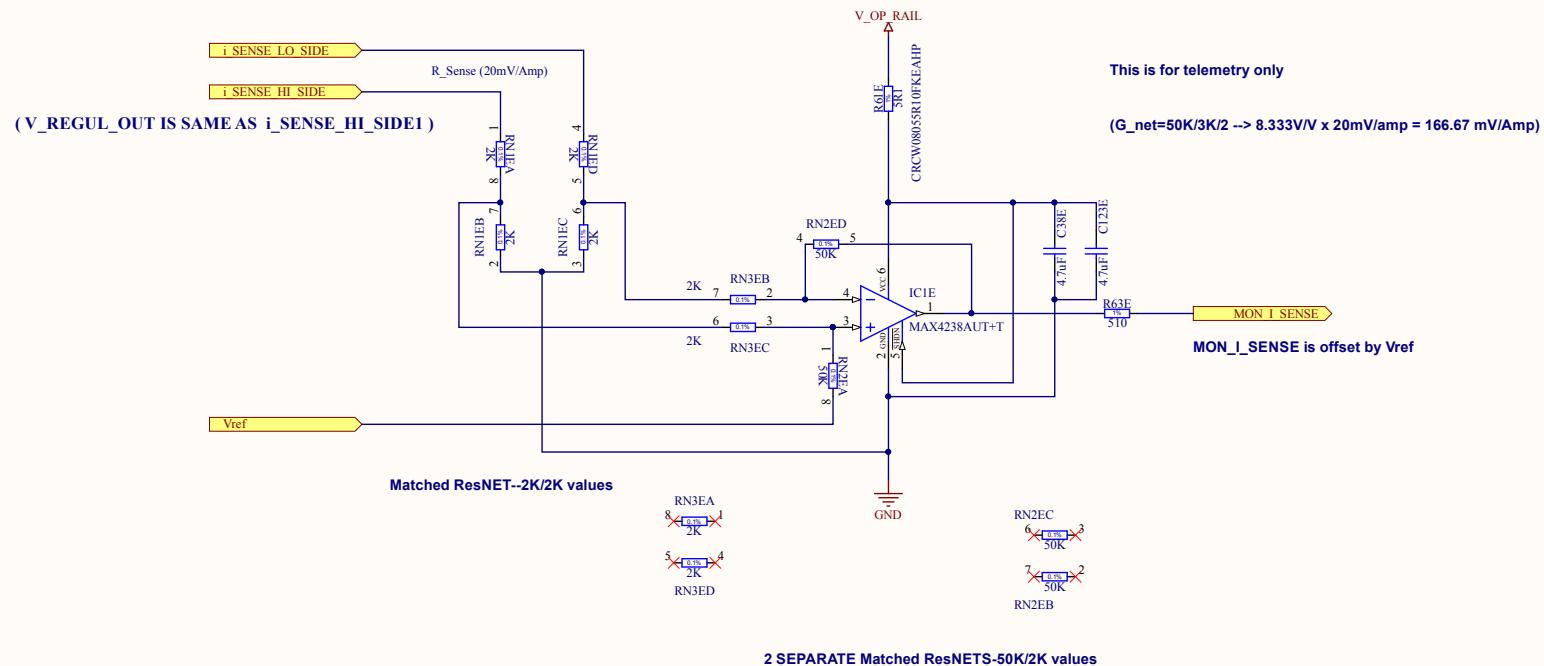
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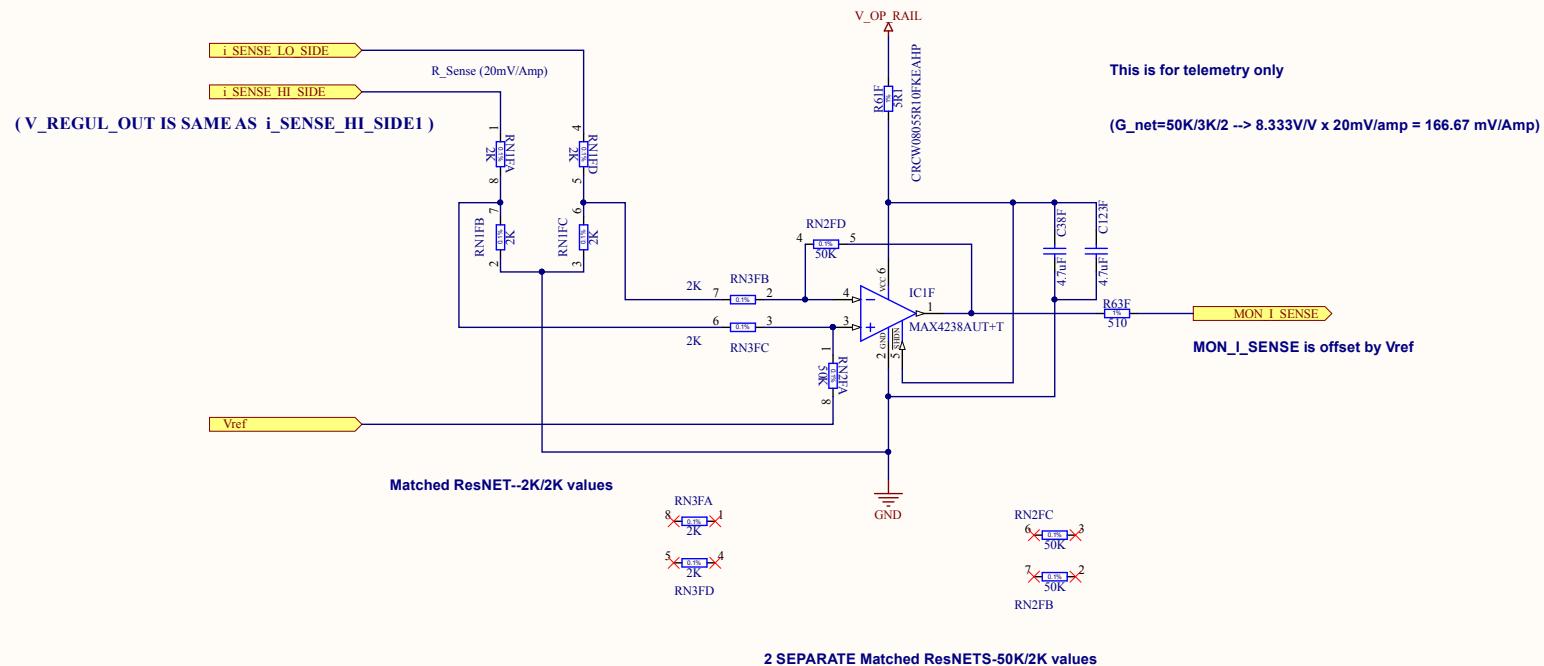


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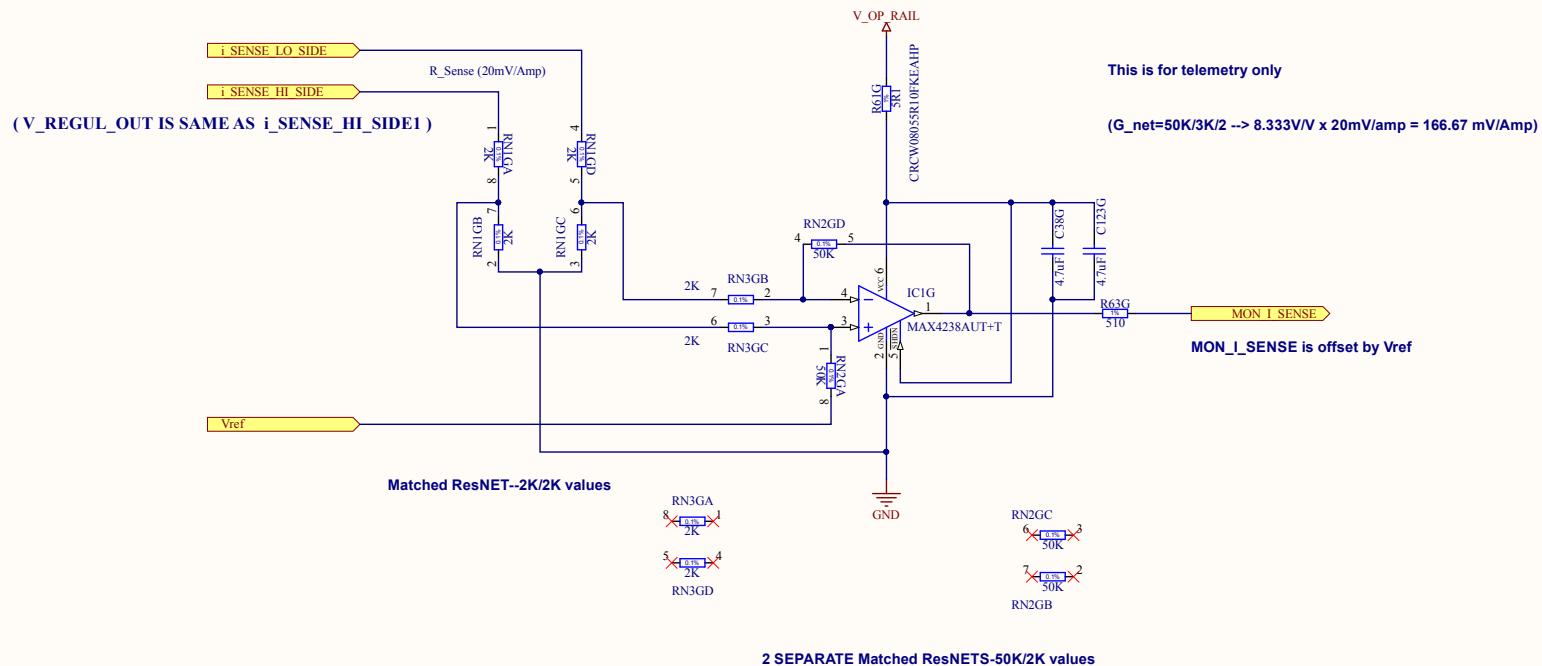
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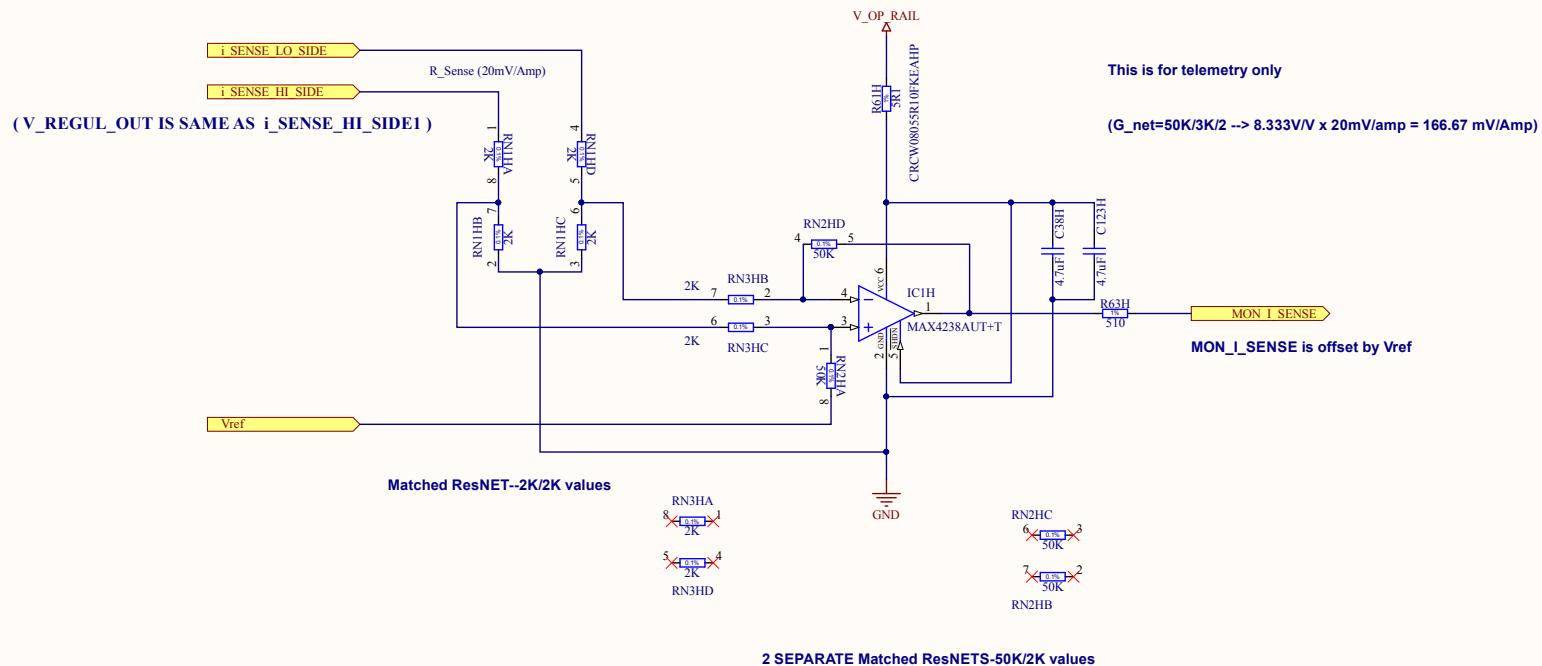
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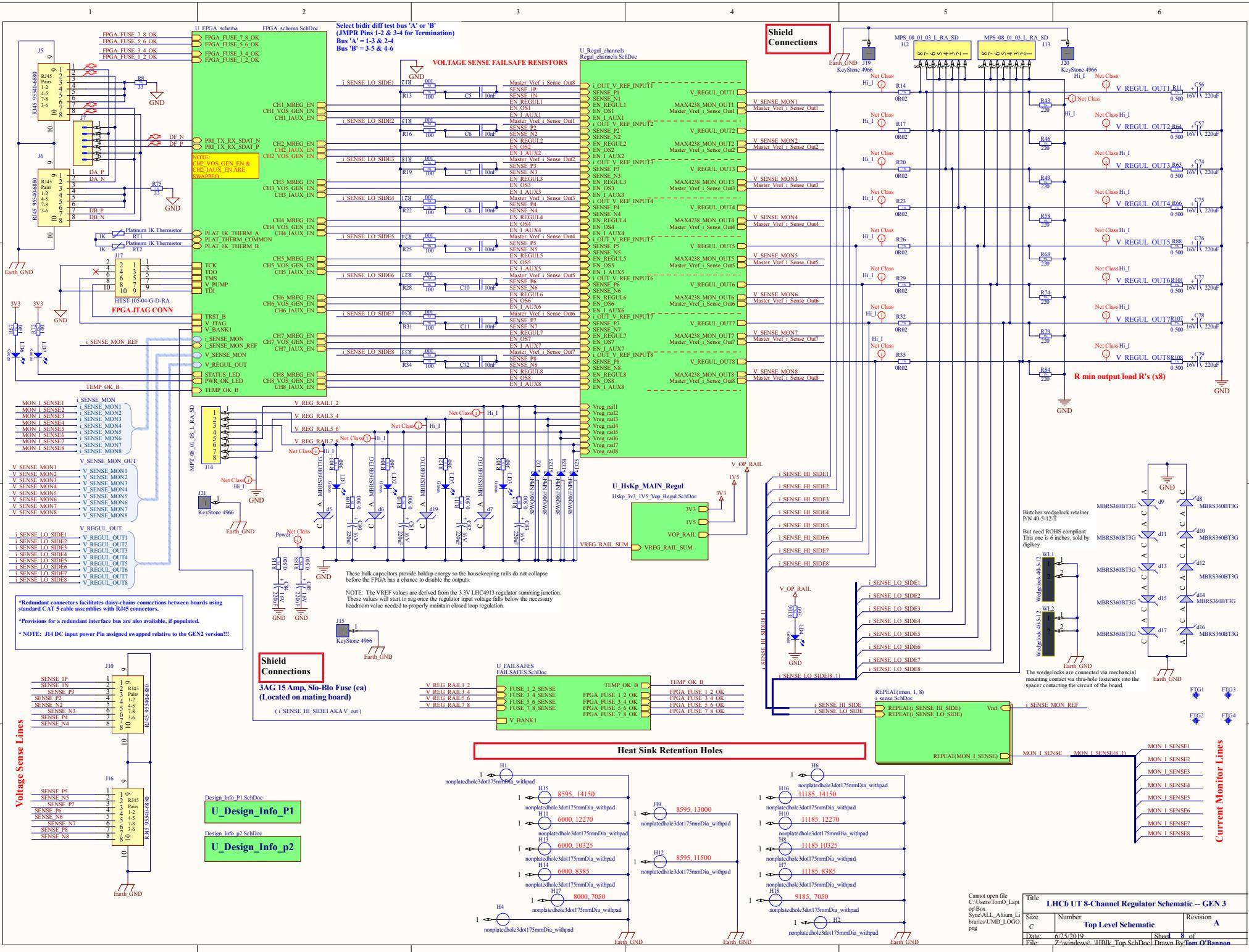
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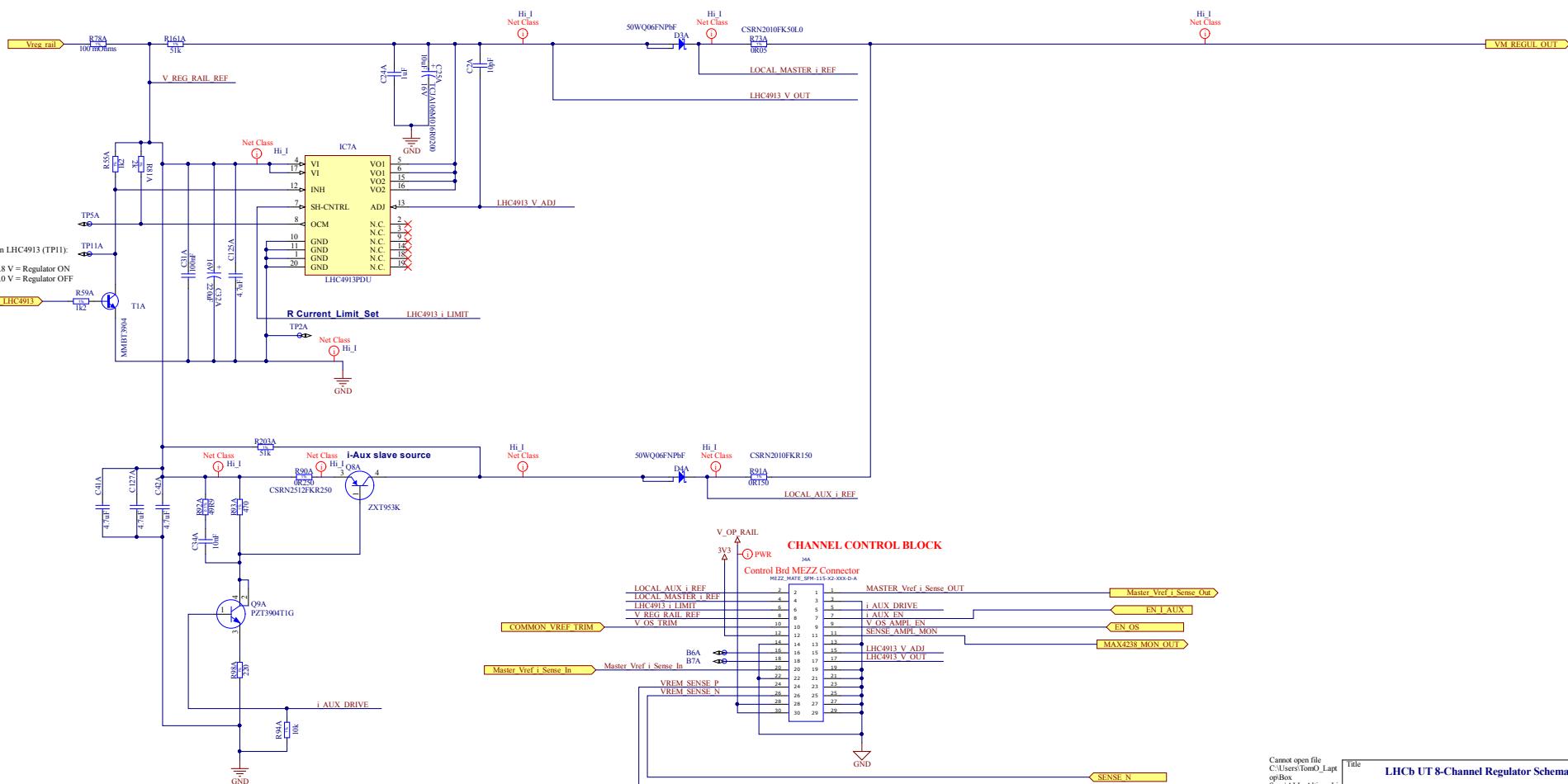
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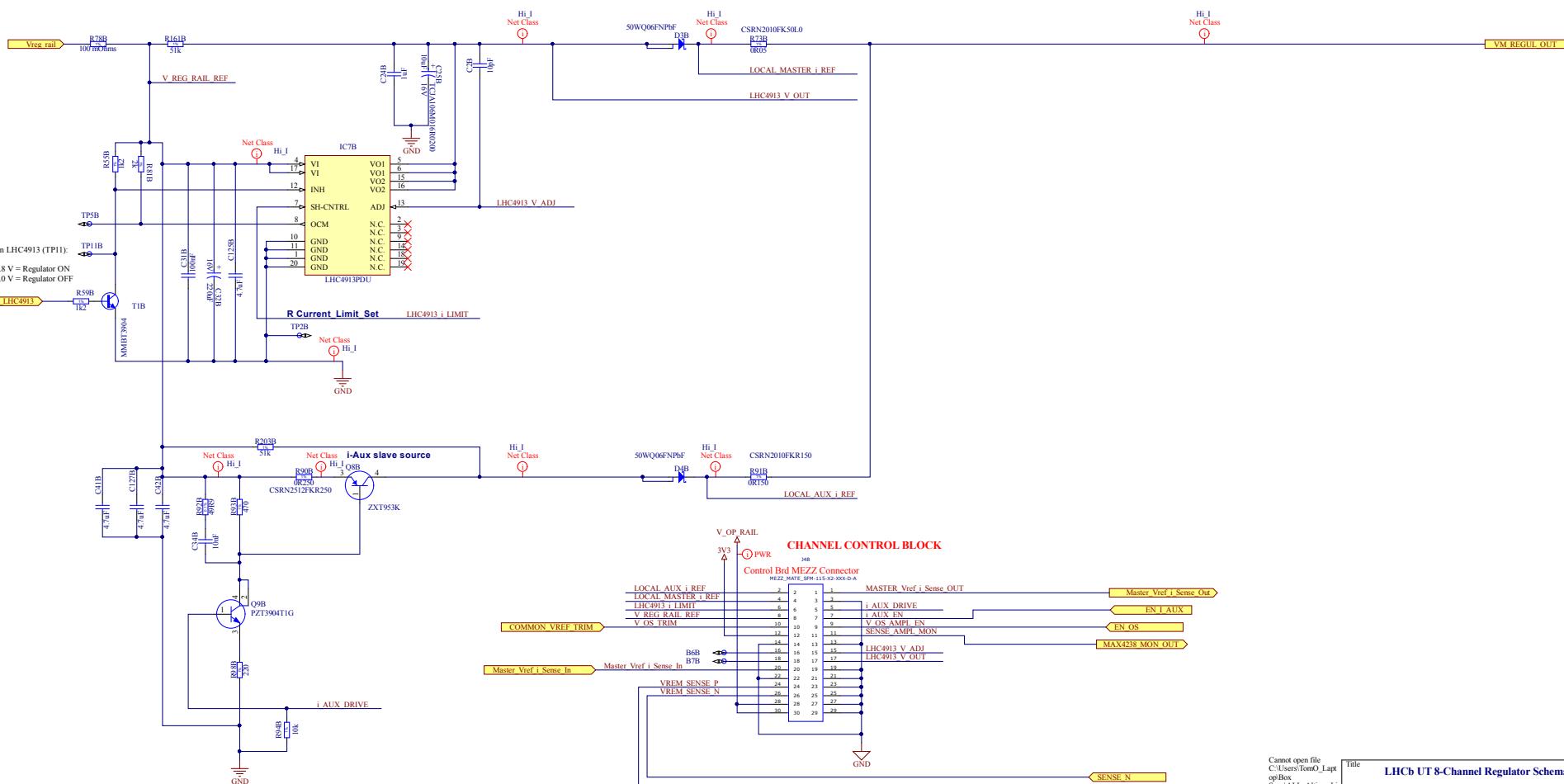
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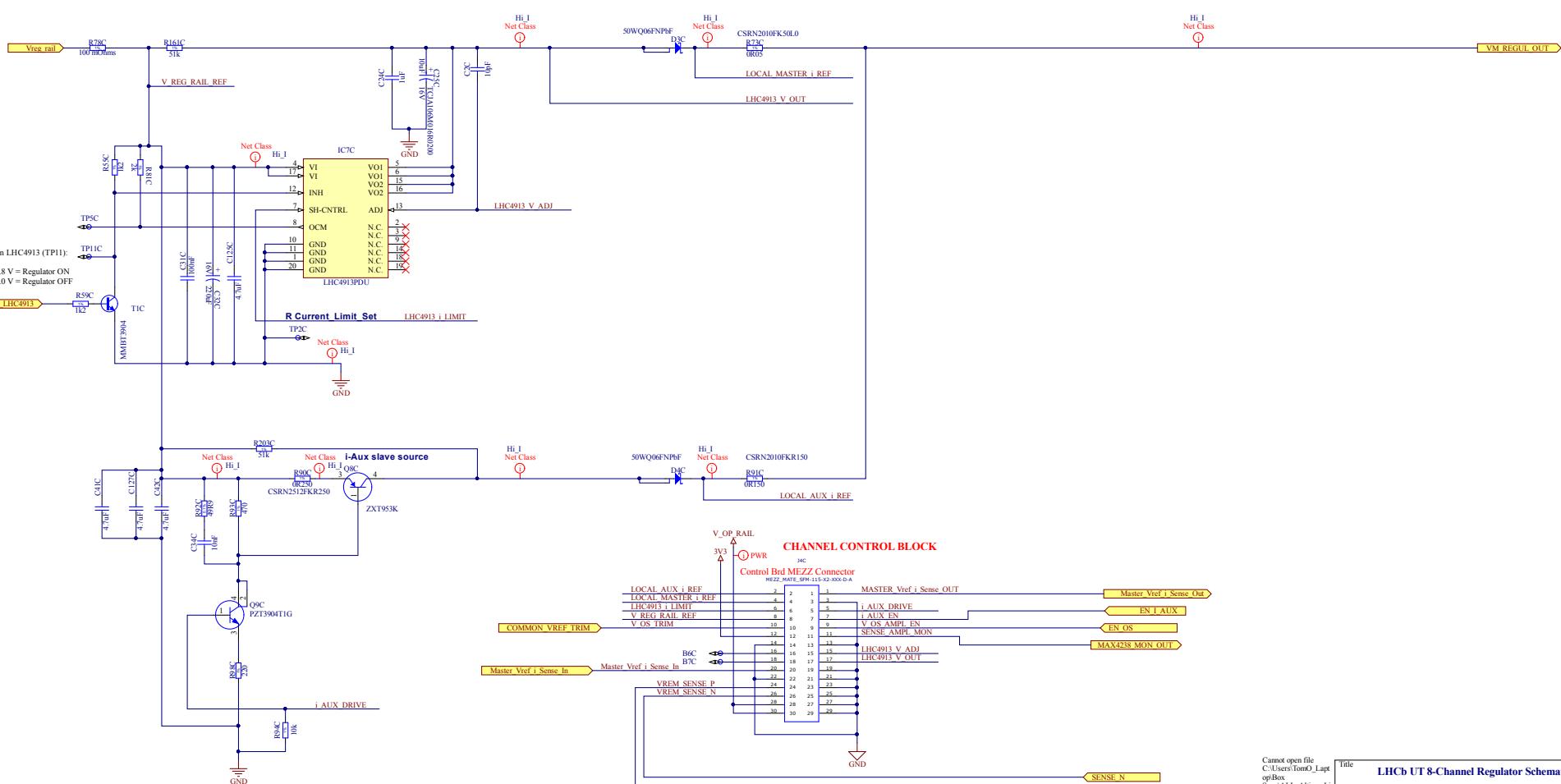
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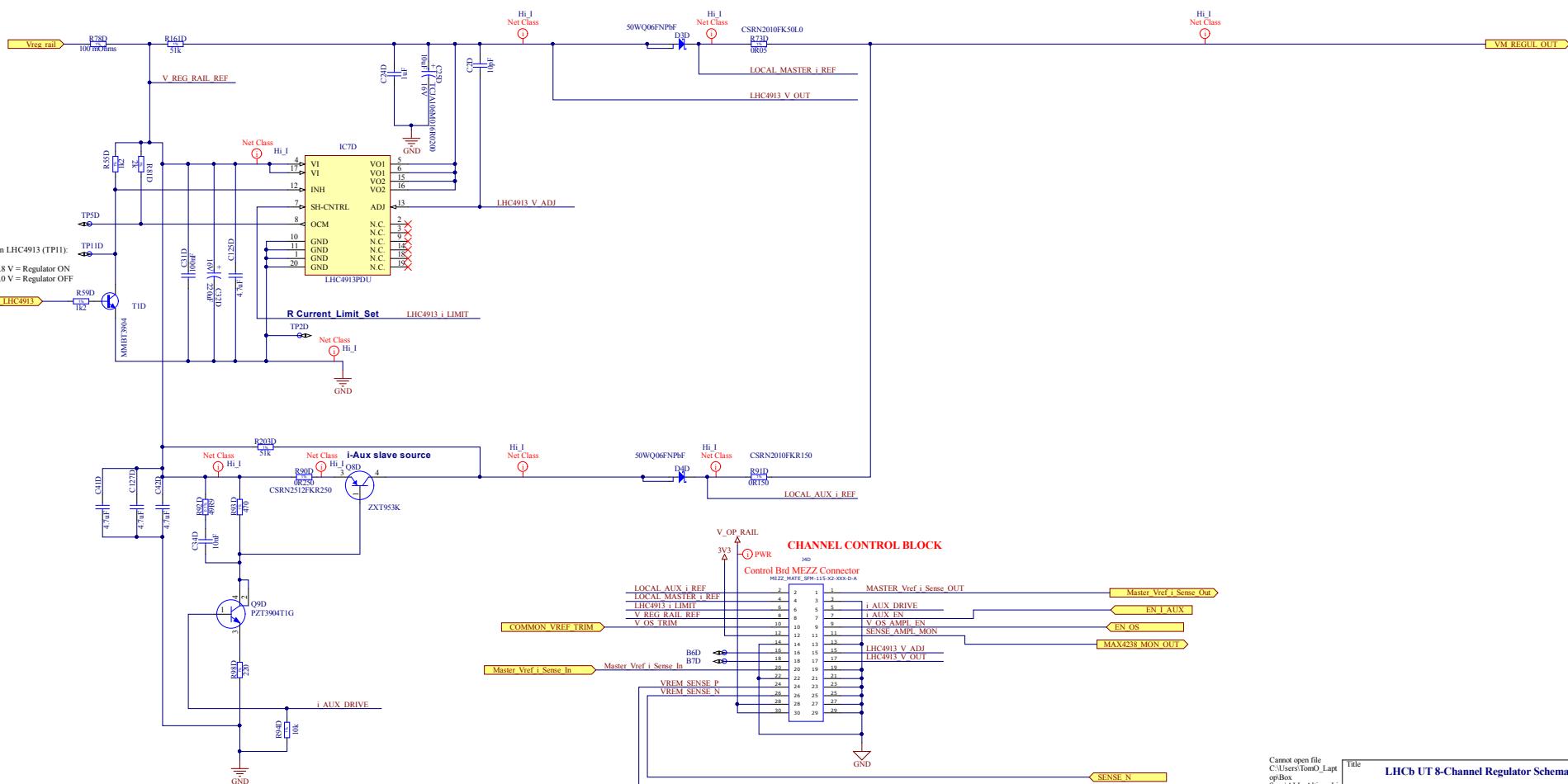
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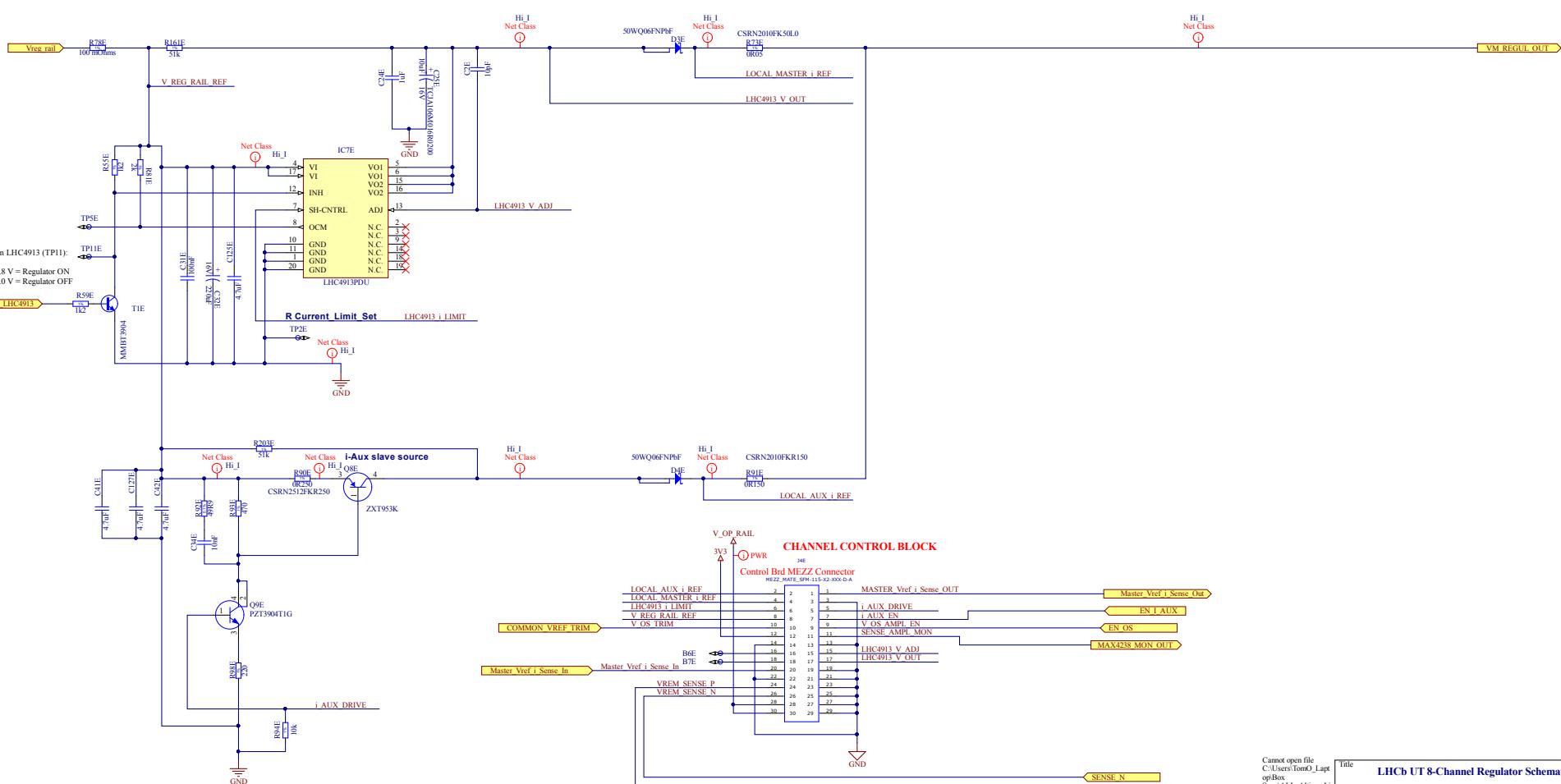
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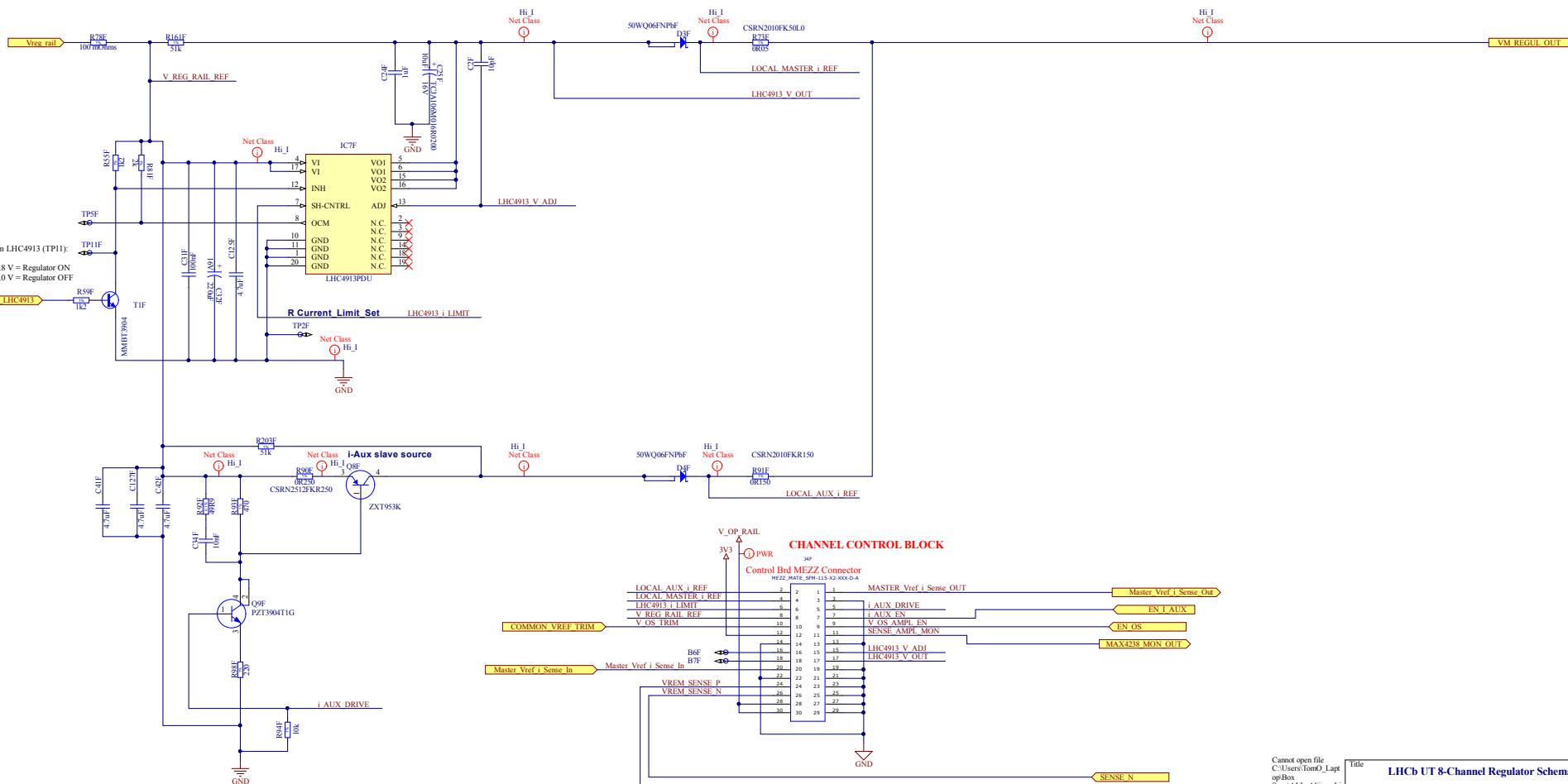
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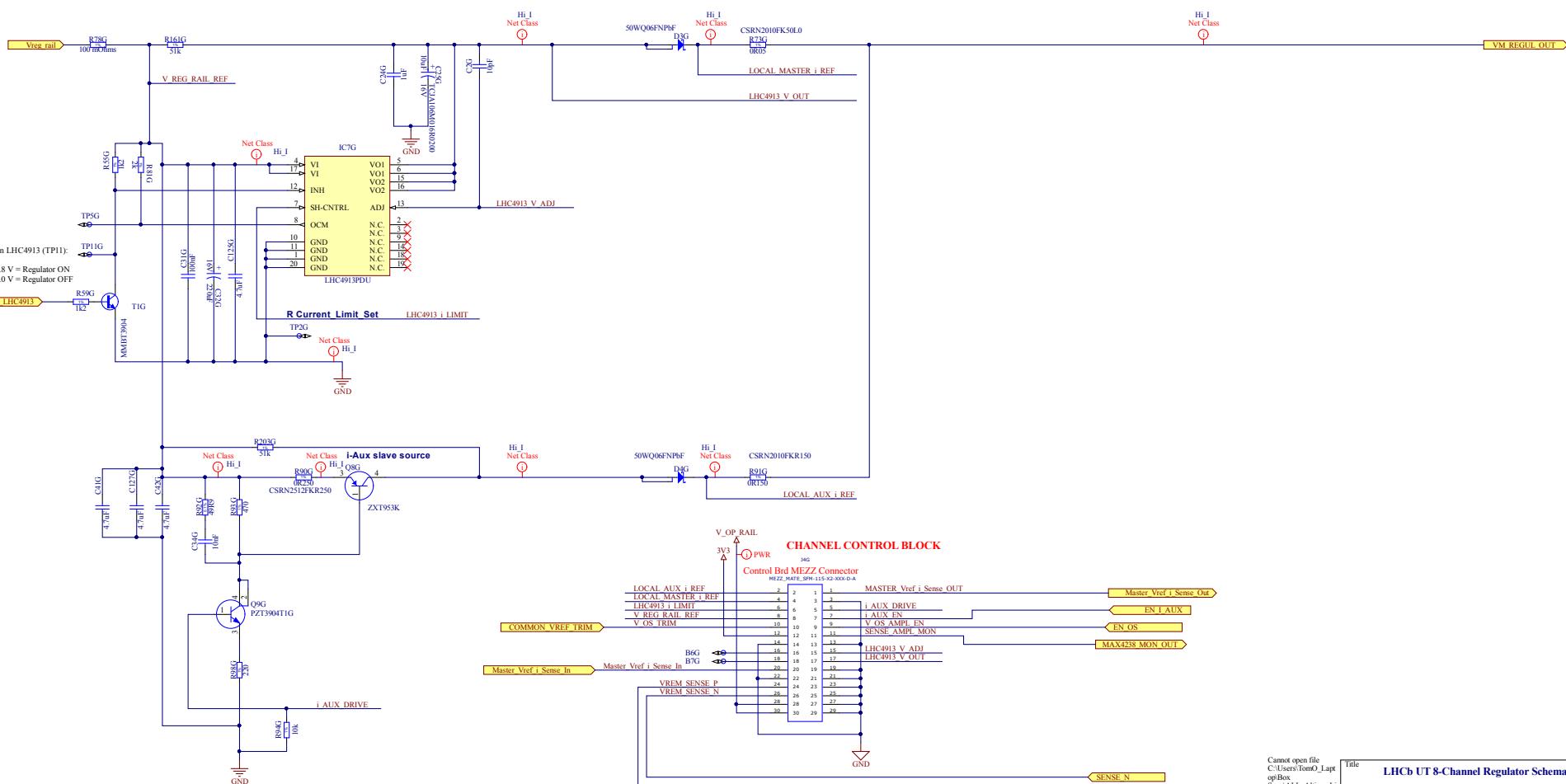
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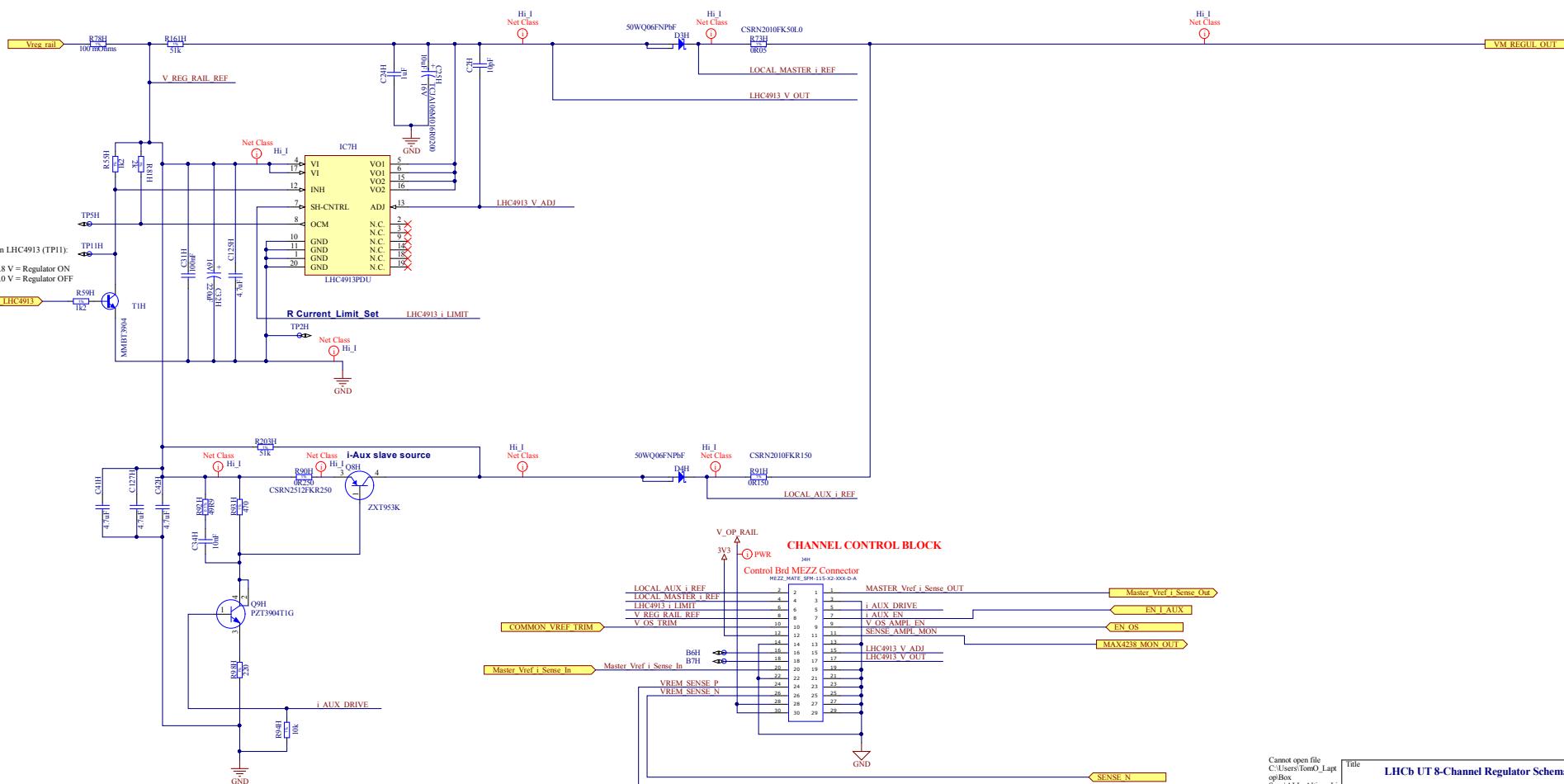
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LHCb UT 8-Channel Regulator Schematic -- GEN 3		
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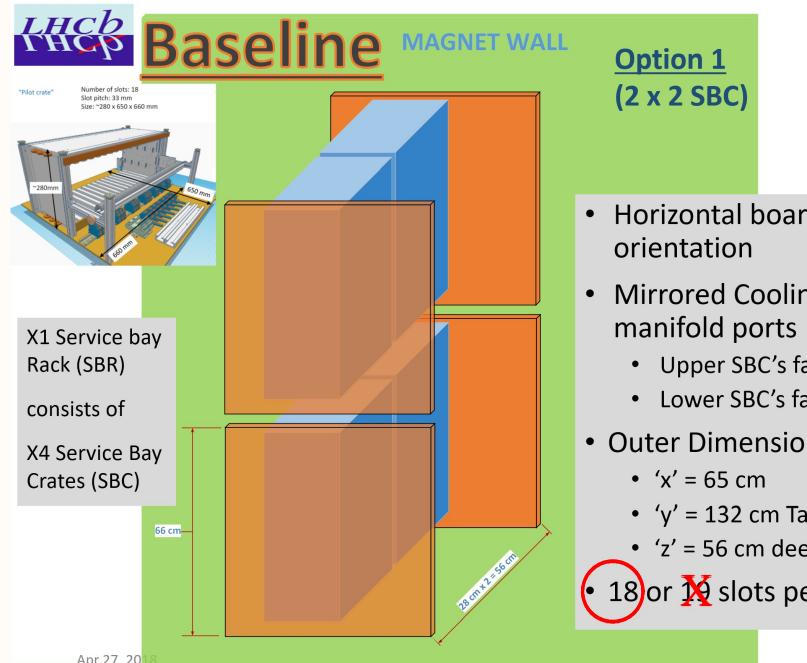
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Sheet: **2** of **2**
Date: **6/25/2019** Drawn By: **Tom O'Bannon**
File: **Z:\windows\RegulatorBlk.SchDoc**

**18 Slots @ 33 mm pitch per SBC
(Preset 'Pilot' SBC Config)**



Supports:

- (a) distributed GBT-SCA daughter brds
- (c) high density telemetry



Option 1 (2 x 2 SBC)

- Horizontal board orientation
- Mirrored Cooling manifold ports
 - Upper SBC's face up
 - Lower SBC's face down
- Outer Dimensions
 - 'x' = 65 cm
 - 'y' = 132 cm Tall
 - 'z' = 56 cm deep
- **18 or ~~10~~ slots per SBC**



64 GBT-SCA user manual

13.2. POWER SUPPLY

The nominal power supply voltages are VDD = DVDD = AVDD = 1.5V.

The core logic is operational at a supply voltage (VDD) down to 1.2 V (at 25C).

The IO pad power supply (DVDD) works at 2.5V allowing to interface with 2.5V powered devices.

13.3. ABSOLUTE MAXIMUM POWER SUPPLY RATINGS

Table 13.1 shows the absolute minimum and maximum voltages for the three supplies power the GBT-SCA ASIC.

	MINIMUM	MAXIMUM
VDD	1.2V - 10%	1.5V + 10% DVDD + 0.3V
AVDD	1.5V - 10%	1.5V + 10% DVDD + 0.3V
DVDD	1.2V - 10%	3.3V

Table 13.1 – Maximum power supply ratings

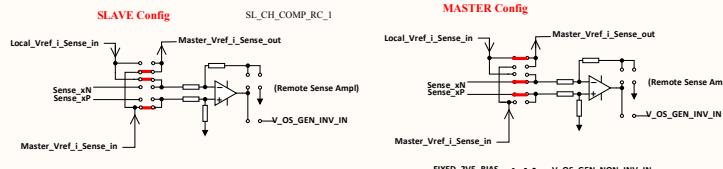
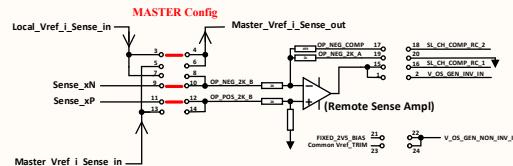
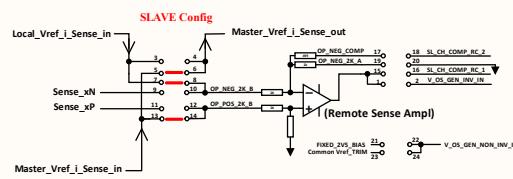
- 1) Fuses should be 12 AMP Slo-Blo max (each)
- 2) Initial turn on procedure needed to make sure 3V3 and 1V5 rails are underspec at initial turn-on and then trimmed to the final desired values. (rotate pots xx turns in xxW direction to ensure setpoints are at lowest value for initial power-on.)

13.5. POWER CONSUMPTION

Measured value at: DVDD = 1.5V, VDD = 1.5V, AVDD = 1.5V

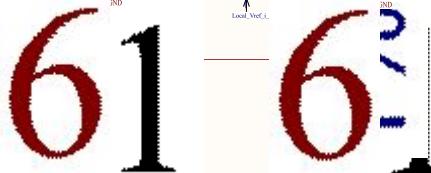
SUPPLY	TYPICAL	MAXIMUM (at the TID peak of leakage)
VDD core	36 mA	63 mA
AVDD analog	0.5 mA	0.8 mA
DVDD Static supply current	7.1 mA	8.2 mA

Table 13.3 – GBT-SCA power consumption



Notes for Gen3 Updates regarding the Master-Slave channel configuration:

- (1) The slave channel Vos_gen needs to be DISABLED by the gateway (ie only the master gets the offset command signal at startup since the slaves are already following the master output synthetic summing junction)
- (2) The slave channel needs a jumper between J8 pins 15 to 16.



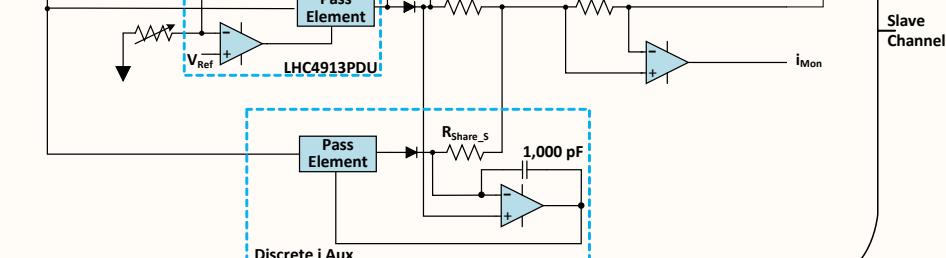
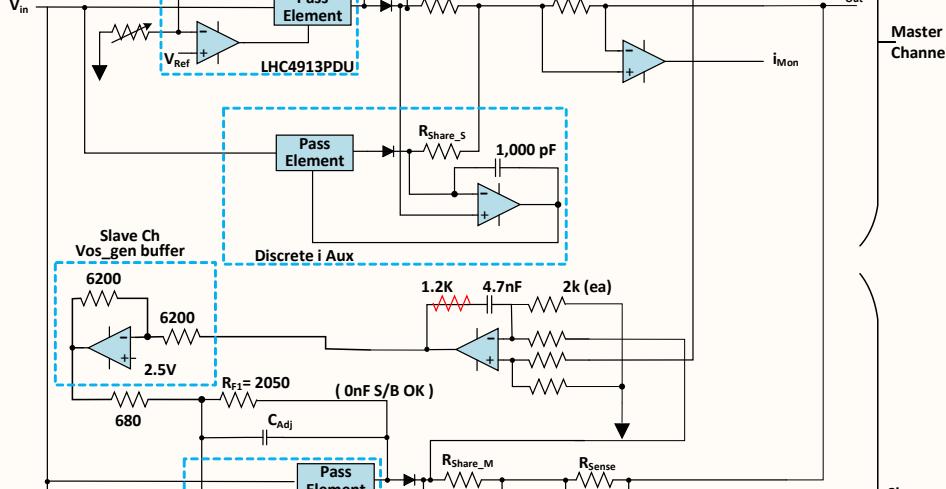
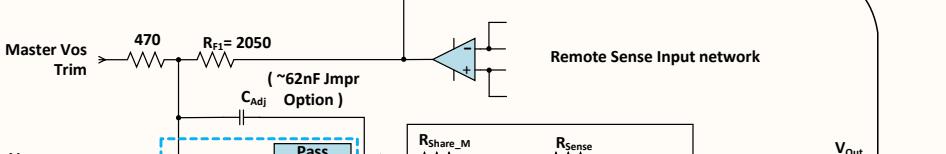
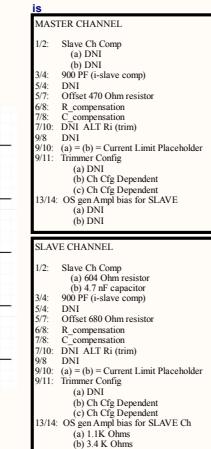
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MASTER CHANNEL

- 1/2: Slave Ch Comp (a) DNI (b) DNI
- 3/4: 900 PF (i-slave comp)
- 5/6: DNI
- 7/8: R compensation
- 9/10: C compensation
- 11/12: DNI ALT Ri (trim)
- 13/14: (a) = (b) = Current Limit Placeholder
- 7/9: Trimmer Config
- (a) DNI
- (b) Ch Cfg Dependent
- (c) Ch Cfg Dependent

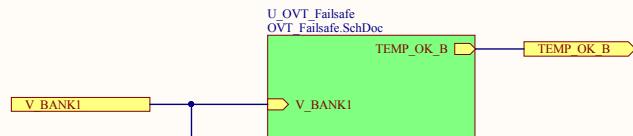
SLAVE CHANNEL

- 1/2: 900 PF (i-slave comp)
- 3/4: Offset 470 Ohm resistor
- 5/6: R compensation
- 7/8: C compensation
- 9/10: DNI ALT Ri (trim)
- 7/9: Trimmer Config
- (a) DNI
- (b) Ch Cfg Dependent
- (c) Ch Cfg Dependent



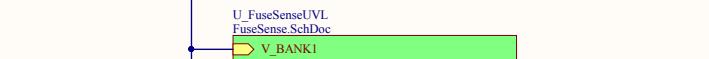
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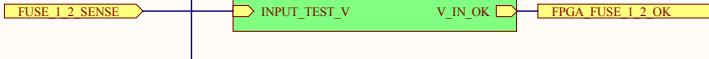
This circuit provides an over-temperature indicator for the FPGA. This allows for a local temperature failsafe protection implemented by the FPGA so outputs can be turned off using the preferred sequence method.

B



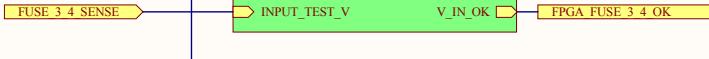
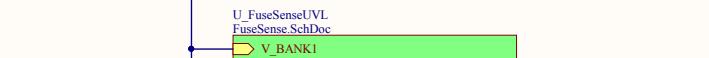
These 4 FusesenseUVL modules perform an under-voltage sense for each of the fuse inputs.

C



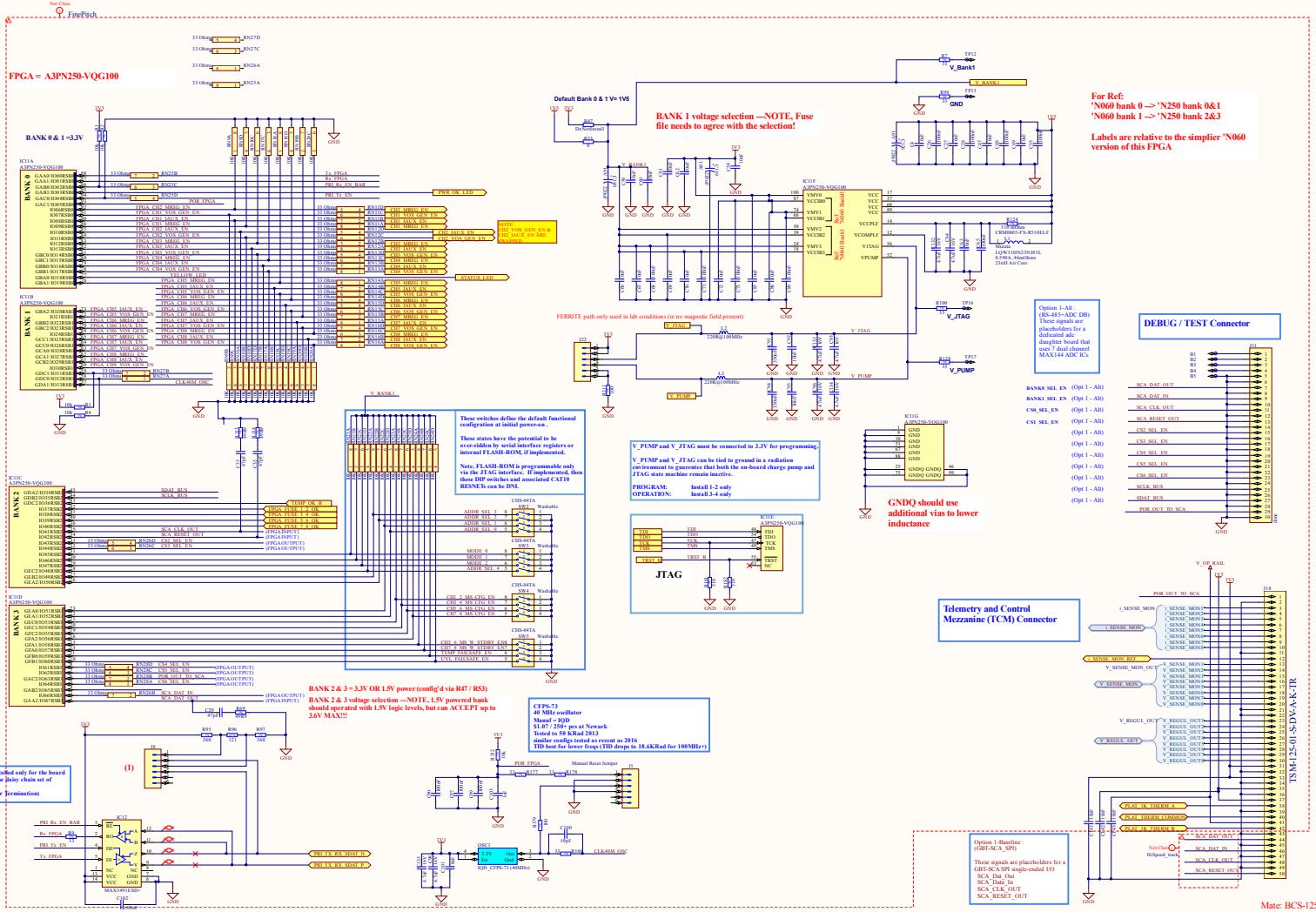
The voltage threshold is determined by discrete components configured with a partial temperature compensation to reduce temperature effects. All other housekeeping voltage rails are inadequate for establishing a threshold since they are essentially derived from the 1.225V ref of the housekeeping LHC4913. This Vref is only guaranteed to be accurate when the input is above 3.3V + 0.5V.

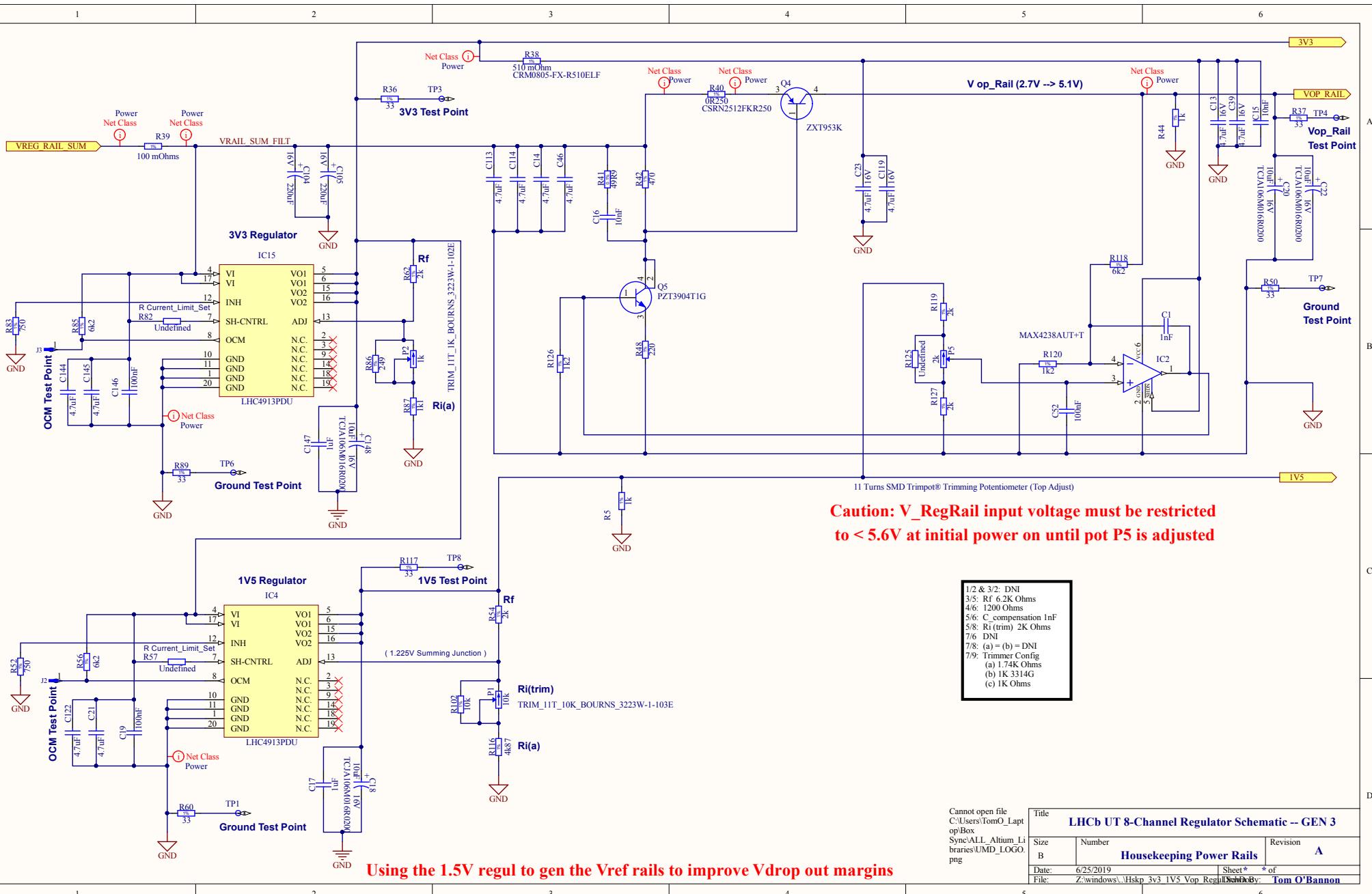
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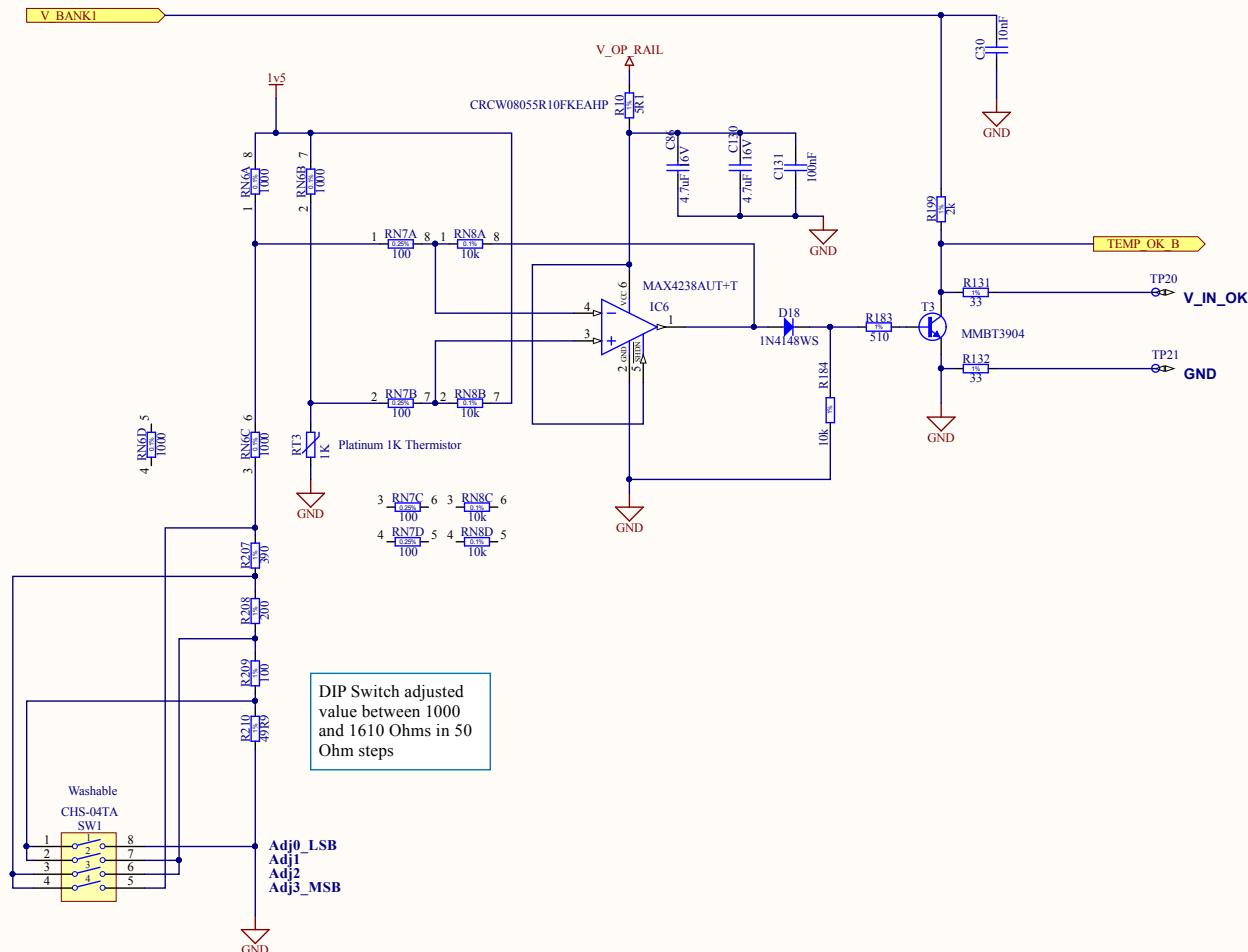


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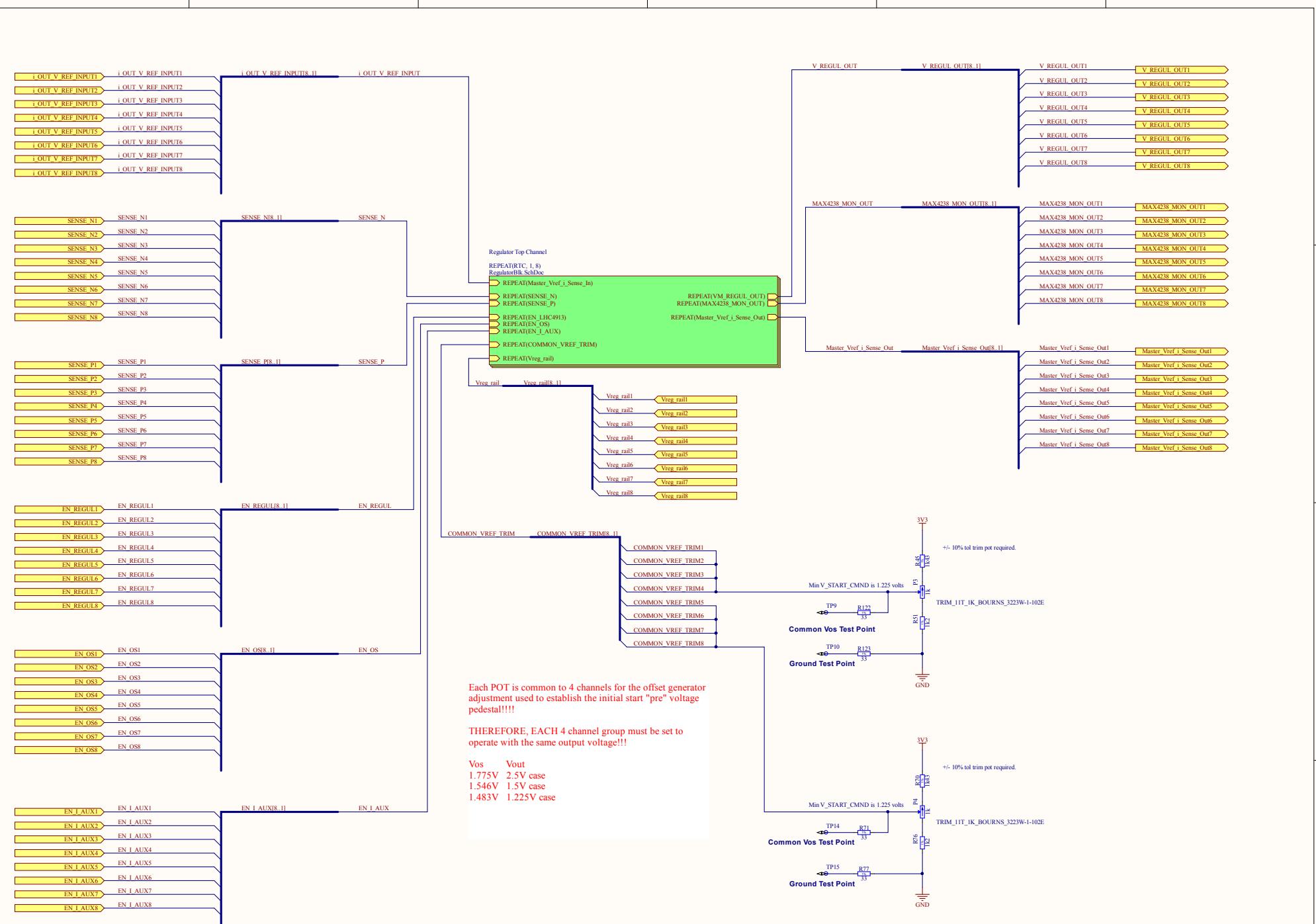






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