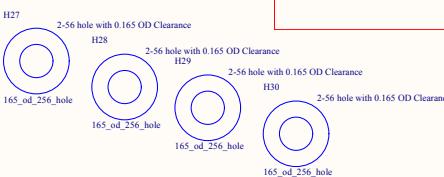
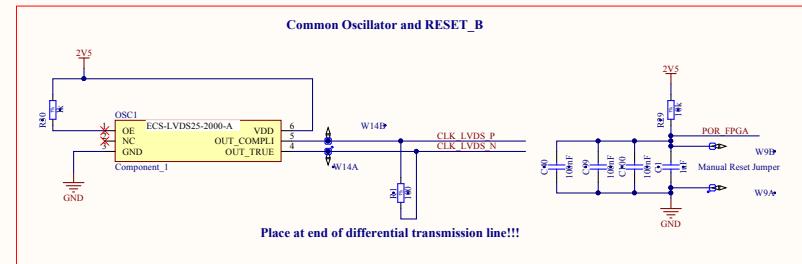
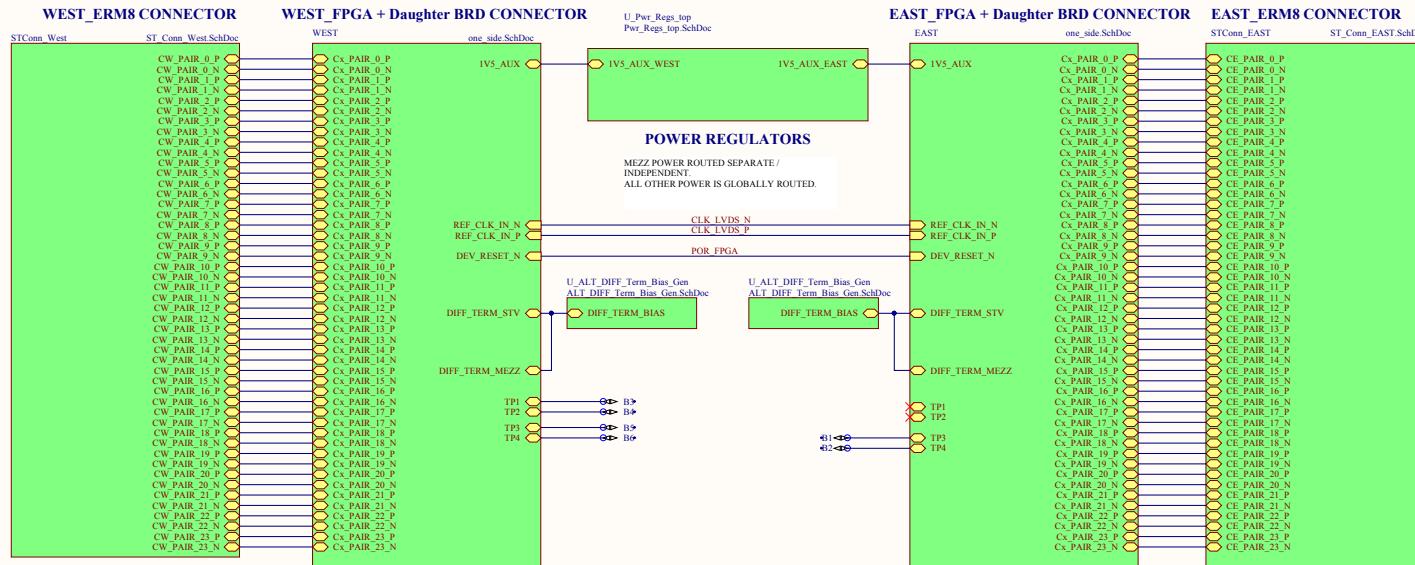


i2C needs option to add filter network (eg low freq RF balun?, RC filter network)  
 NEED OPTIONS TO CONNECT SALT DRIVERS / RECEIVERS

WORSE CASE BOARD SPACING AT MEGARRAY BREAKOUT IS 30 MM BETWEEN BOARD CENTERS



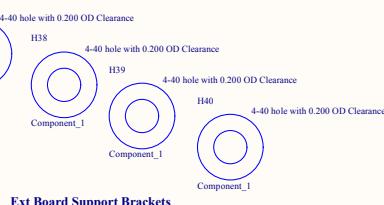
FEAST MP Daughter Board

**two blocks on left and two block on the right need to be in separate hierarchical pages so layout rooms can be defined.**

Daughter boards are used for the following configs:

- 1) Hybrid I/O definition (ie inputs versus outputs)
  - 2) DCB I/O definition
  - 3) GBTx eval carrier with direct physical elink access
- Mezzanine boards provide either plug-in function:
- 1) FPGA derived optical interface
  - 2) GBTx derived interface with elink logical access via FPGA

Use 2 RJ conn per FPGA-->  
 Need at the Service Bay for 1 side of 1/2 of a  
 stave WC:  
 6 clk\_t7 sources  
 6 TFC sources  
 6 i2C sources (what about active buffer at  
 the service bay end to drive the shield to  
 lower effective capacitance?)

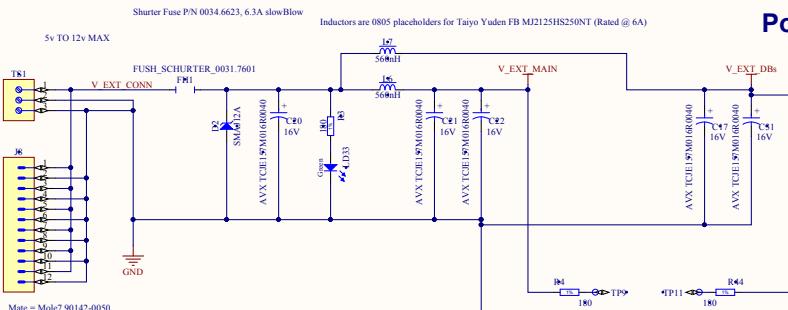


Ext Board Support Brackets

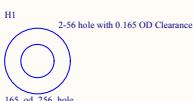
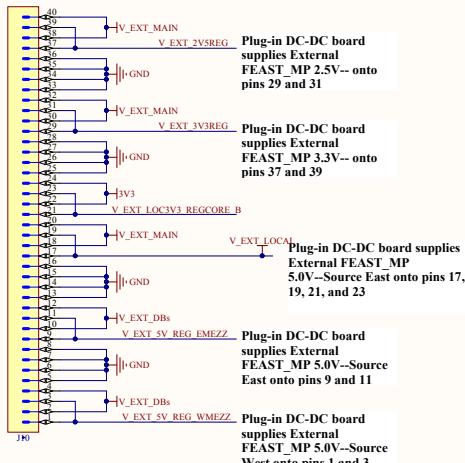
University of Maryland

Title	Hier_Top_Shl1.SchDoc	
Size	Number	Revision
C	COMET	A
Date:	8/21/2015	Sheet 1 of 9
File:	D:/Alum_DOCs/_Hier_Top_Shl1.SchDoc	Drawn By: Tom O'Bannon

## Power Regulators



**Dual-Purpose Connector**  
1) POWER CONFIG JUMPERS  
2) ALT QUAD FEAST-MP REGULATOR PLUG IN SITE



WC FPGA power is 54 pairs at 10ma each= **0.550 Amps** from 2.5V rail.

Need Power for GBTx (1.5V at 1.5 Amps ea)

Need power for VTTx / VTRx (0.5Amps @ 1.5V)

Need power for additional Mezz Serializer ...

## TRIM RESISTOR VALUES

3.3V = 590 ohm

2.5V = 953 ohm

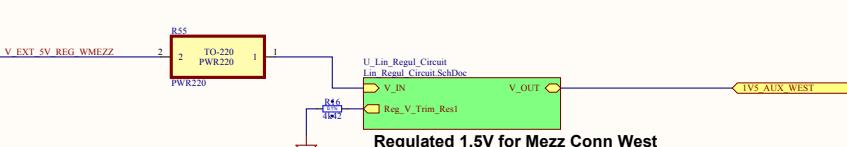
1.5V = 4420 ohm

for  $R_f = 1000$ , use 0.1% tol

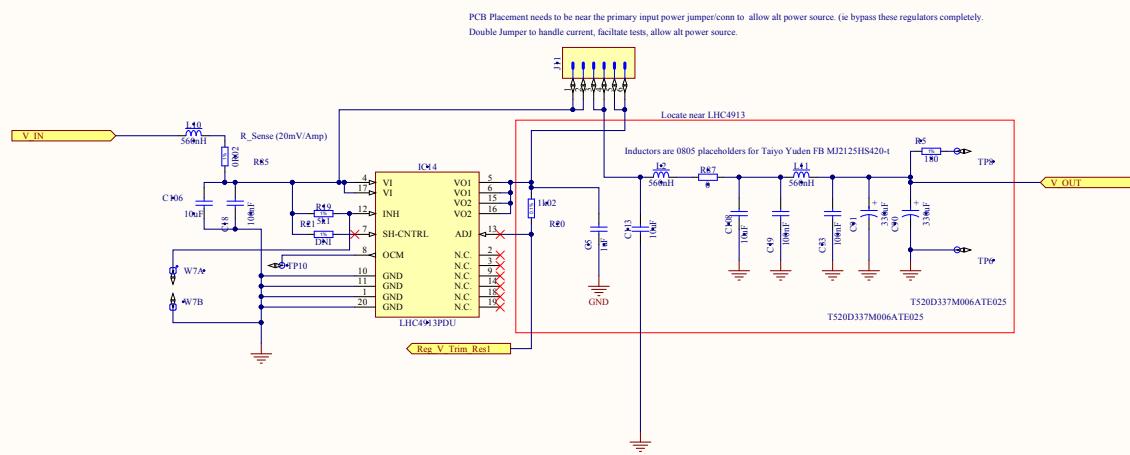
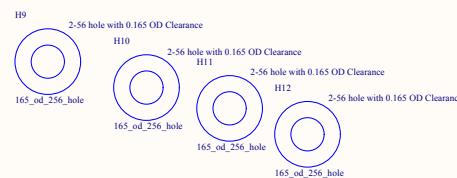
3V3, 2V5, AND 1V5 ARE GLOBAL POWER PLANE SOURCES!



THESE TWO 1V5 OUTPUTS ARE FOR THE EAST AND WEST MEZZ CONNS AS WELL AS THOSE FOR THE DAUGHTER BOARDS



Title		
Pwr_Regs_top.SchDoc		
Size	Number	Revision
C	COMET	A
Date:	8/21/2015	Sheet 2 of 9
File:	D:\Alum\DOCS\IPwr_Regs_top.SchDoc	Drawn By: Tom O'Bannon



**May need a heat sink since the thermal slug faces up**

Determined that a similar package from Ape7 Microtechnology (PA162) as the one for the LHC4913 has a junction-to-air thermal resistance of 25 C/W. This package has the slug down and the estimate assumes the thermal pad is soldered to at least 1 sq inch of copper.

University of Maryland		
Title	<u><a href="#">Lin_Regul_Circuit.SchDoc</a></u>	
Size C	Number <b>COMET</b>	Revision <b>A</b>
Date: 8/21/2015	Sheet 3 of <b>9</b>	
File: D:\Alum\DOCS\Lin_Regul Circuit.SchDoc	Download By: Tom O'Bannon	

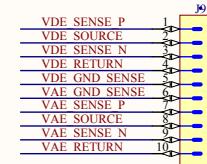
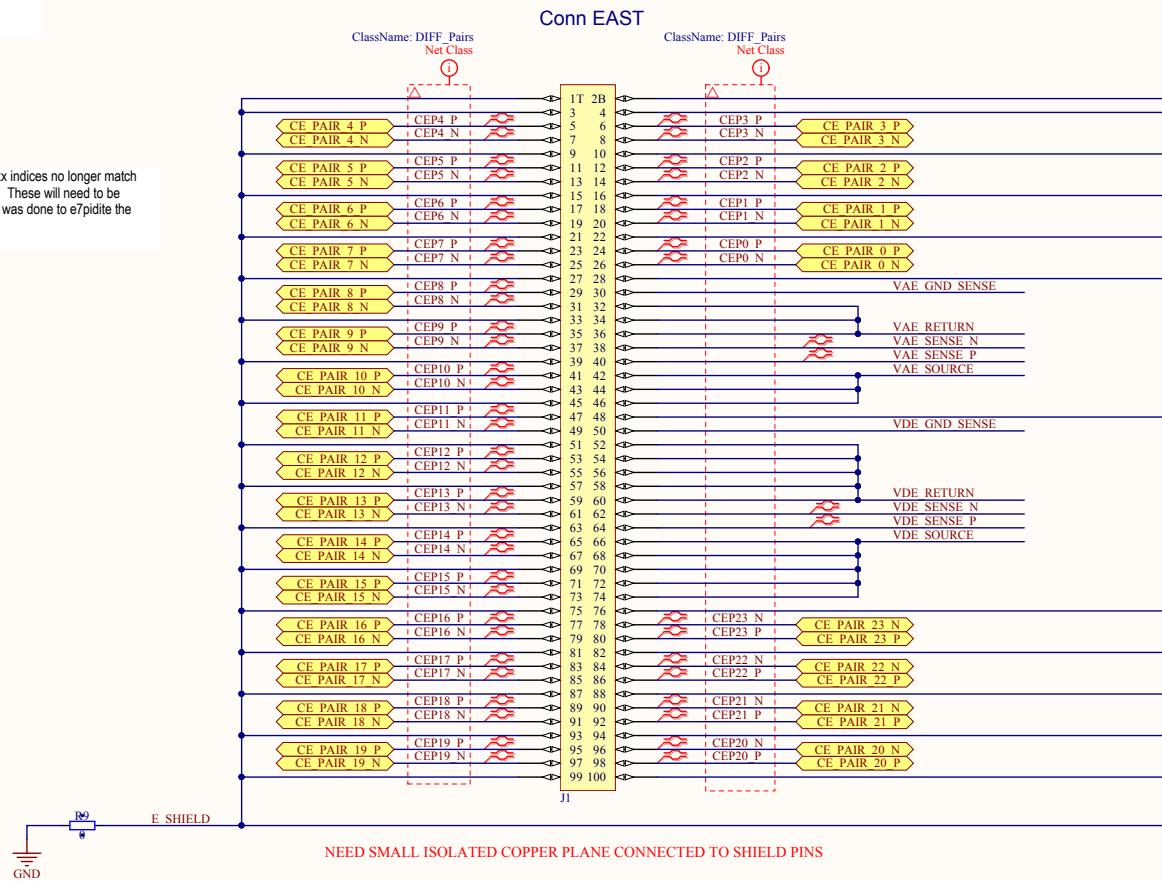
## ST\_CONN\_EAST: Stave Connector Assignments

NOMENCLATURE  
 'CW\_ELINK\_7\_V' = CONNECTOR WEST  
 'CE\_ELINK\_7\_V' = CONNECTOR EAST

VAV\_7 = ANALOG VOLTAGE ON WEST CONNECTOR  
 VDW\_7 = DIGITAL VOLTAGE ON WEST CONNECTOR

EDGE LAUNCH CONNECTOR  
 'T' = TOP ROW OF CONNECTOR PINS  
 'B' = BOTTOM ROW OF CONNECTOR PINS  
 (CONNECTOR ORIENTATION TO THE BOARD IS KEYED BY A NOTCH IN THE BOARD)

Note: The CE\_PAIR\_xx\_xx indices no longer match the stave cable designations. These will need to be re-mapped in firmware. This was done to e7pidite the layout.



Placeholder SALT Load at hybrid end and power inject  
Conns at meg-array end.

2 1  
4 3

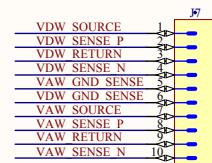
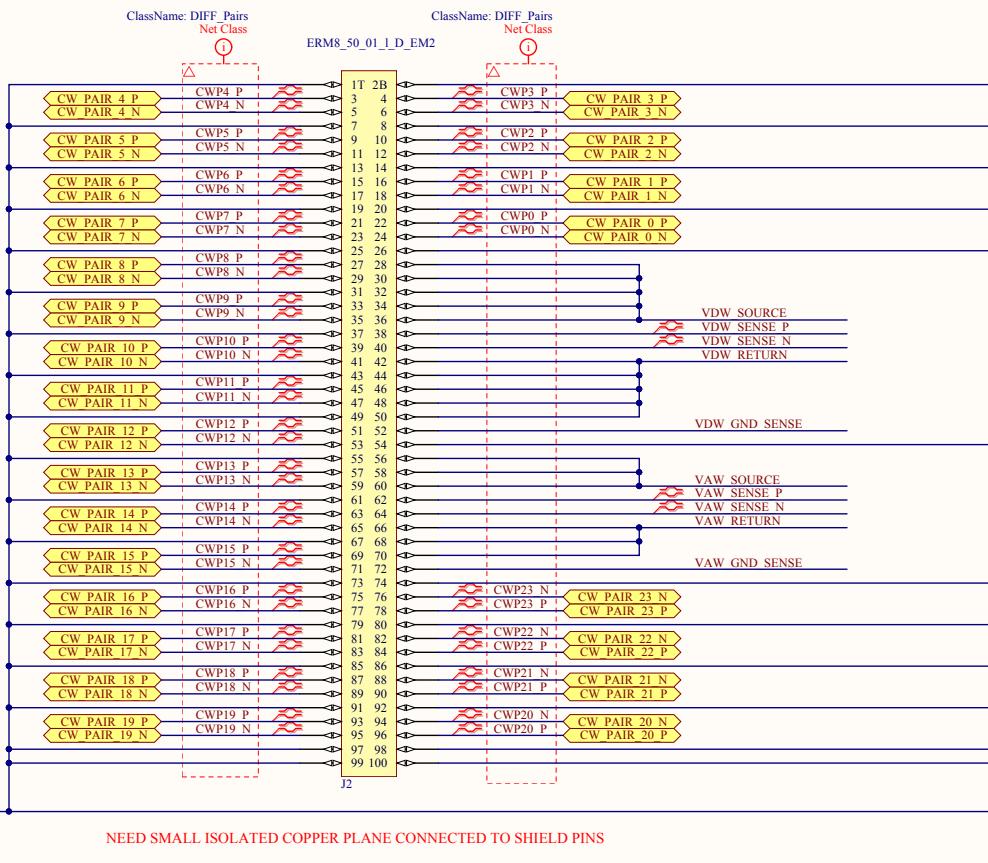
University of Maryland		
Title ST_Conn_East.SchDoc		
Size B	Number COMET	Revision A
Date: 8/21/2015	Sheet 4 of 9	
File: D:\Altium DOCs\ST Conn East.SchDoc		Drawn By: Tom O'Bannon

## ST\_CONN\_WEST: Stave Connector Assignments

NOMENCLATURE  
 'CW\_ELINK\_7\_Y' = CONNECTOR WEST  
 'CE\_ELINK\_7\_Y' = CONNECTOR EAST

VAW\_7 = ANALOG VOLTAGE ON WEST CONNECTOR  
 VDW\_7 = DIGITAL VOLTAGE ON WEST CONNECTOR

EDGE LAUNCH CONNECTOR  
 'T' = TOP ROW OF CONNECTOR PINS  
 'B' = BOTTOM ROW OF CONNECTOR PINS  
 (CONNECTOR ORIENTATION TO THE BOARD IS KEYED BY A NOTCH IN THE BOARD)



Placeholder SALT Load at  
hybrid end and power inject  
Conns at meg-array end.

2 1  
4 3

GND

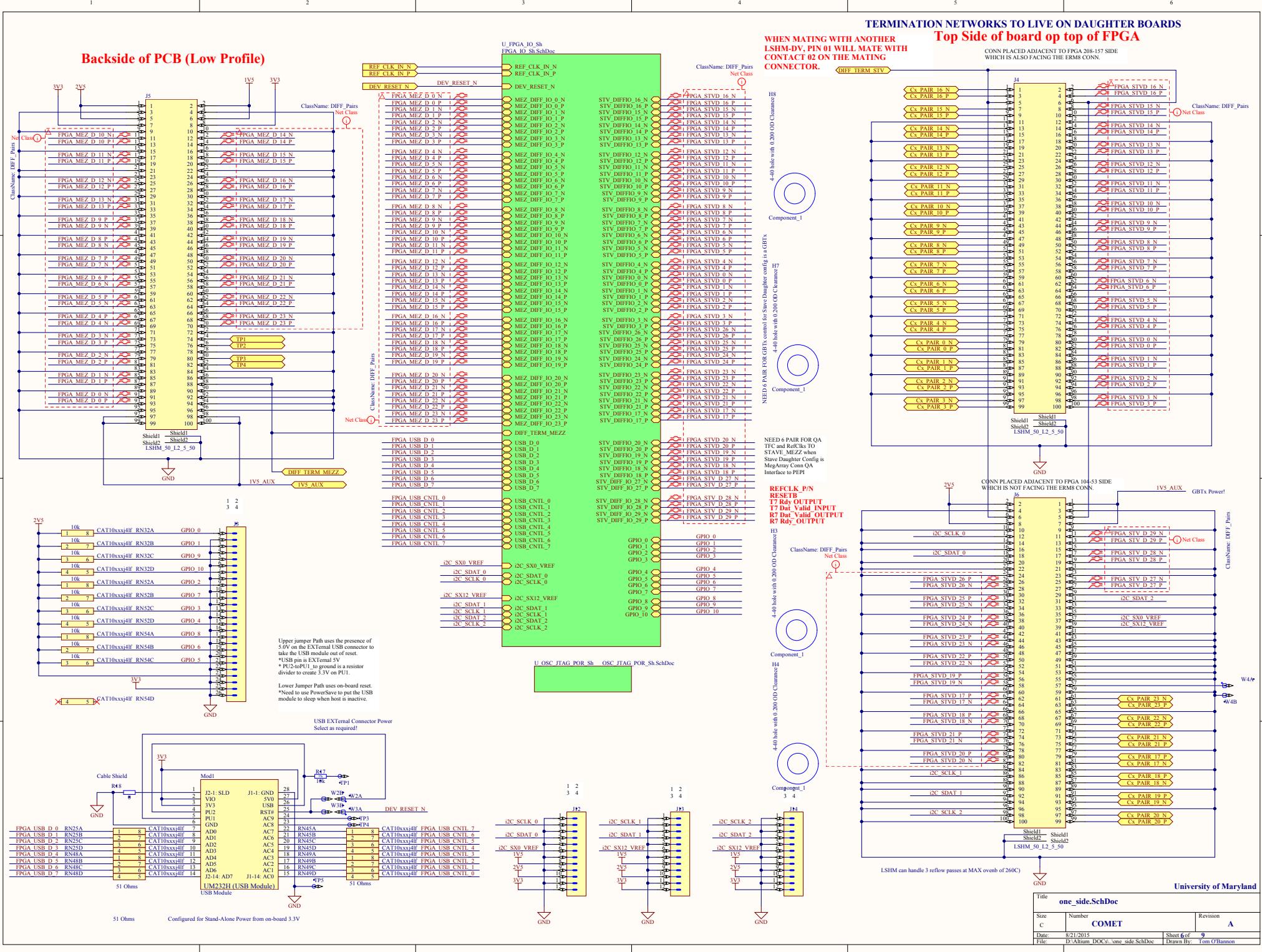
R63

W SHIELD

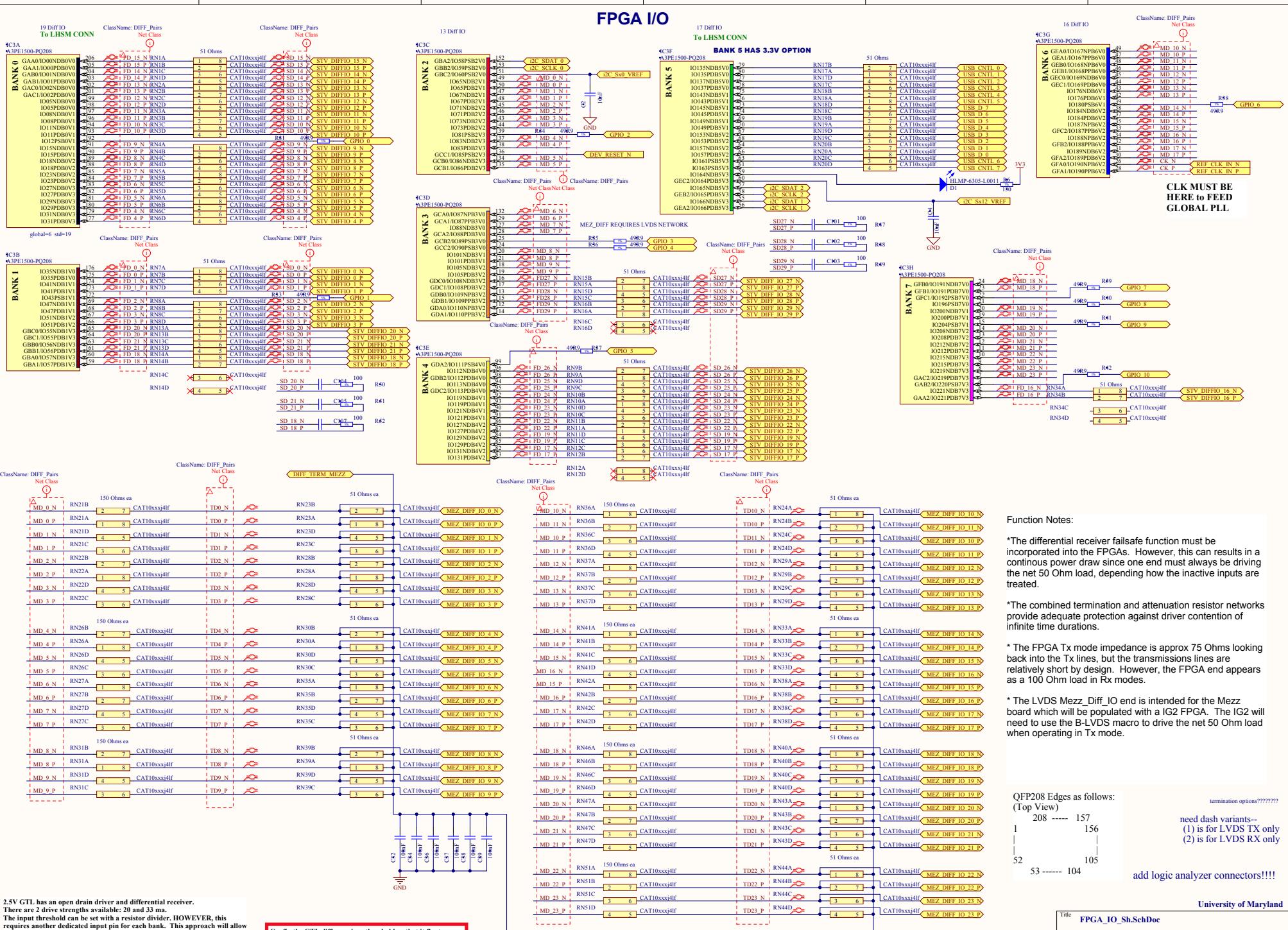
NEED SMALL ISOLATED COPPER PLANE CONNECTED TO SHIELD PINS

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Title ST_Conn_West.SchDoc		
Size B	Number COMET	Revision A
Date: 8/21/2015	Sheet 5 of 9	
File: D:\Altium DOCs\ST Conn West.SchDoc	Drawn By: Tom O'Bannon	



# FPGA I/O



2.5V GTL has open drain drivers and differential receiver. There are 2 drive strengths available: 20 and 33 mA. The input threshold can be set with a resistor divisor. HOWEVER, this requires another dedicated input pin for each bank. This approach will allow the GTL to be used as the I2C receiver via establishing a threshold of 1.5V / 2 (ie 1/2 of power rail).

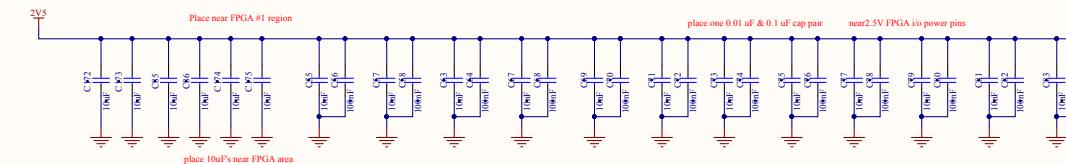
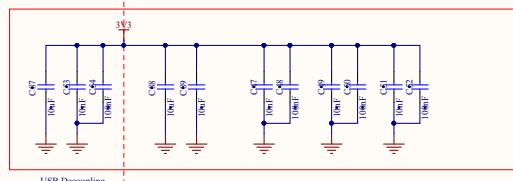
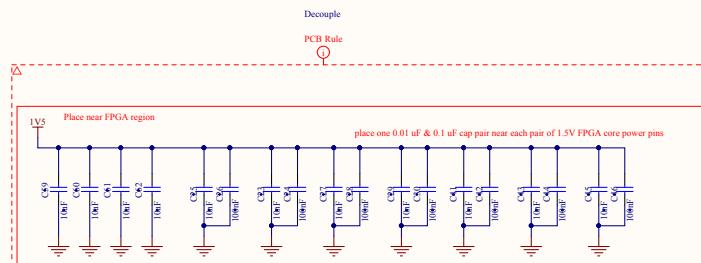
Config the GTL diff receiver threshold so that it floats relative to the remote ground ref at the SALT IC location

## FPGA SUPPORT: JTAG, LVDS Clk, and POR

A

Decouple

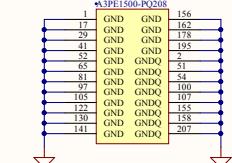
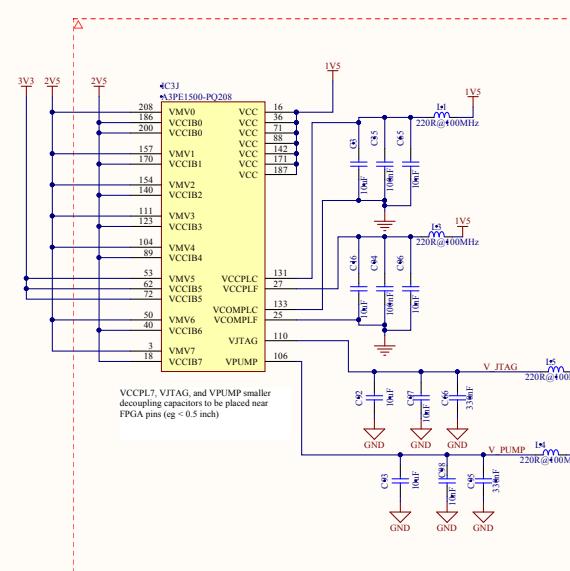
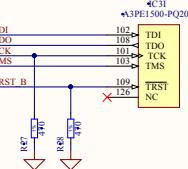
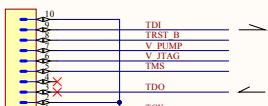
PCB Rule



A

### JTAG

(Separate JTAG ports allow build variants containing only 1 of the FPGAs)

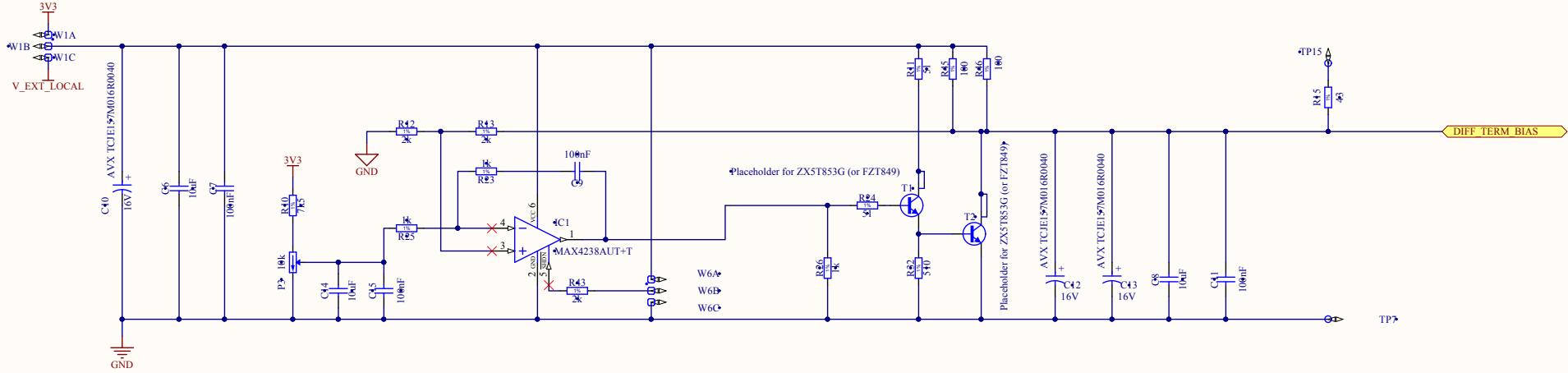


THE 'G7' AND 'GC' I/O ARE CHIP WIDE GLOBAL I/O'S.  
THE OTHER 'G' I/O'S ARE LIMITED TO SINGLE QUADRANTS ONLY.

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Title	OSC_JTAG_POR_Sh.SchDoc	
Size	Number	Revision
C	COMET	A
Date: 8/21/2015 File: D:\Alum\DOC\\$\\OSC_JTAG_POR_Sh.SchDoc	Sheet 8 of 9	Tom O'Bannon

## Differential Termination V Bias Gen (SINK)



University of Maryland

Title		
ALT_DIFF_Term_Bias_Gen.SchDoc		
Size	Number	Revision
B	COMET	A
Date:	8/21/2015	Sheet 9 of 9
File:	D:\Altium DOCs\ALT DIFF Term Bias Gen.SchDoc	Tom O'Bannon

