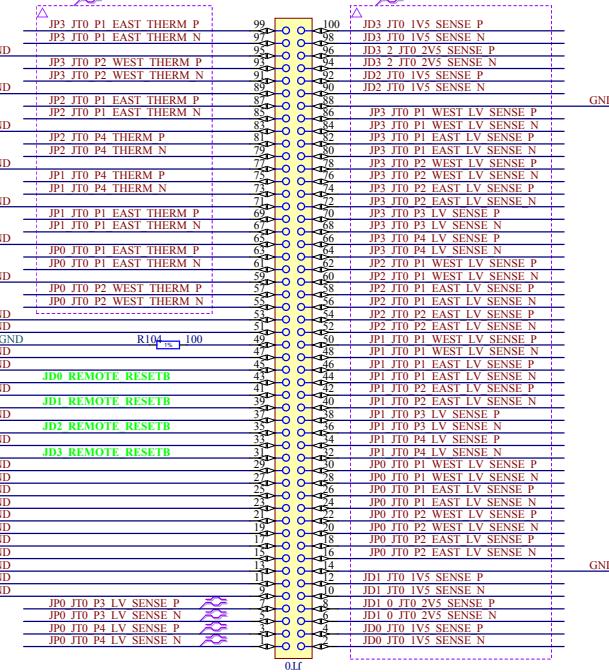
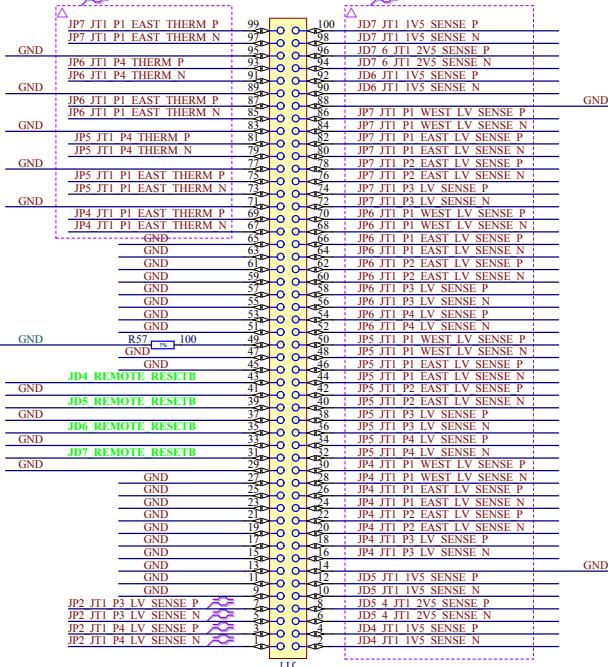
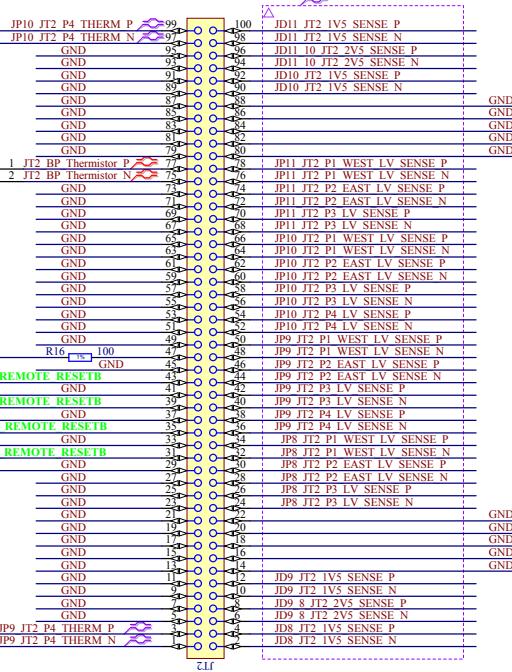


- 1) The final backplane has to route some of the thermistors for CO2 system.
- 2) MAKE the DIFF PAIR Track width UNIQUE to facilitate find and replace
- 3) NEED PLACE TO ATTACH GROUND BRAIDS to the breakout boards (grounds to be via breakout board conn)
- 4) Place a platinum thermistor on each backplane
- 5) The plug-in power conns may need to short the power hybrid groups together since there are different configurations for each backplane location! ALT solution is to have the bus-bars allow for this custom config.
- 6) ALL Pigtails are electrically identical!

Depopulation resistors:

- All floating copper must be grounded (e.g. depopulating lines that go to empty DCB slots)
- Depopulating Elinks that go to active DCBs must be biased using that DCB's power rails
- Depopulating hybrid LV sense also terminated on backplane
- Actual LV power lines that depopulate will be handled in PPBB

Project/Equipment		PEPI	
Document		Designer	T. O'Bannon
		Drawn by	P.M. Hamilton
		Date	18/3/2018
TE/MP/E		Last Rev	18/3/2018
B50	FIG1	Last Mod.	6/26/2019
B50	FIG2	File Notes	Sheet Sched Doc
B50	FIG3	File	Top Notes Sheet Sched Doc
B50	FIG4	Rev	1.00
B50	FIG5	Page	1 of 21
B50	FIG6	Sheet	A2
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-04066-V1-0	



NOTE: The GND connected via the series 100 Ohm can be used as a remote ground signal reference where needed.

IMPORTANT NOTE: The "GND" pins **MUST NOT EVER** be connected to any remote ground nodes.



Project/Equipment					
Document		Designer	Designer		
TE/MPE 	Title Title2	Drawn by	DrawnBy	XX/XX/XXXX	
		Check by	-	-	
		Last Mod.	-	8/12/2019	
		File	Telemetry IO UpperComms SchDoc		
		Print Date	12/18/2019 9:28:22 AM	Sheet	2 of 21
				Size	Rev
				A3	-
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X			

A
UPPER Power Conns--(All dedicated to pigtail power routes)
JPUx connectors located directly on the Pigtail Power Breakout Board

NOTE: ALL 3 of these contact / pigtail assignment grouping needed to be identical so one PCB design can be used in 3 places on the rear of the backplane

Fed by JPU2 on the Pigtail Power Breakout Brd

JS_JPU_TWO_1	JP11 JPU2 PI WEST LV SOURCE	100nf	C30
JS_JPU_TWO_2	JP10 JPU2 PI WEST LV SOURCE	100nf	C50
JS_JPU_TWO_3	JP10 JPU2 PI EAST LV SOURCE	100nf	C55
JS_JPU_TWO_4	JP10 JPU2 PI EAST LV SOURCE	100nf	C56
JS_JPU_TWO_5	JP10 JPU2 PI EAST LV SOURCE	100nf	C57
JS_JPU_TWO_6	JP10 JPU2 PI EAST LV SOURCE	100nf	C58
JS_JPU_TWO_7	JP10 JPU2 PI EAST LV SOURCE	100nf	C59
JS_JPU_TWO_8	JP10 JPU2 PI EAST LV SOURCE	100nf	C60
JS_JPU_TWO_9	JP10 JPU2 PI WEST LV SOURCE	100nf	C61
JS_JPU_TWO_10	JP10 JPU2 PI WEST LV SOURCE	100nf	C62
JS_JPU_TWO_11	JP10 JPU2 PI WEST LV SOURCE	100nf	C63
JS_JPU_TWO_12	JP10 JPU2 PI WEST LV SOURCE	100nf	C64
JS_JPU_TWO_13	JP10 JPU2 PI WEST LV SOURCE	100nf	C65
JS_JPU_TWO_14	JP10 JPU2 PI WEST LV SOURCE	100nf	C66
JS_JPU_TWO_15	JP10 JPU2 PI WEST LV SOURCE	100nf	C67
JS_JPU_TWO_16	JP10 JPU2 PI WEST LV RETURN	100nf	C20
JS_JPU_TWO_17	JP11 JPU2 PI EAST LV RETURN	100nf	C68
JS_JPU_TWO_18	JP10 JPU2 PI EAST LV RETURN	100nf	C69
JS_JPU_TWO_19	JP10 JPU2 PI EAST LV RETURN	100nf	C70
JS_JPU_TWO_20	JP10 JPU2 PI EAST LV RETURN	100nf	C71
JS_JPU_TWO_21	JP10 JPU2 PI EAST LV RETURN	100nf	C72
JS_JPU_TWO_22	JP10 JPU2 PI EAST LV RETURN	100nf	C73
JS_JPU_TWO_23	JP10 JPU2 PI EAST LV RETURN	100nf	C74
JS_JPU_TWO_24	JP10 JPU2 PI EAST LV RETURN	100nf	C75
JS_JPU_TWO_25	JP10 JPU2 PI EAST LV RETURN	100nf	C76
JS_JPU_TWO_26	JP10 JPU2 PI EAST LV RETURN	100nf	C77
JS_JPU_TWO_27	JP10 JPU2 PI EAST LV RETURN	100nf	C78
JS_JPU_TWO_28	JP10 JPU2 PI EAST LV RETURN	100nf	C79
JS_JPU_TWO_29	JP10 JPU2 PI EAST LV RETURN	100nf	C80
JS_JPU_TWO_30	JP10 JPU2 PI EAST LV RETURN	100nf	C81

NOTE: These 100 Ohm bleed resistors are only installed in cases where the copper tracks are NOT being used (ie floating)

Fed by JPU1 on the Pigtail Power Breakout Brd

JS_JPU_ONE_1	JP11 JPU1 PI WEST LV SOURCE	100nf	C162
JS_JPU_ONE_2	JP10 JPU1 PI EAST LV SOURCE	100nf	C168
JS_JPU_ONE_3	JP10 JPU1 PI EAST LV SOURCE	100nf	C170
JS_JPU_ONE_4	JP10 JPU1 PI EAST LV SOURCE	100nf	C171
JS_JPU_ONE_5	JP10 JPU1 PI EAST LV SOURCE	100nf	C172
JS_JPU_ONE_6	JP10 JPU1 PI EAST LV SOURCE	100nf	C173
JS_JPU_ONE_7	JP10 JPU1 PI EAST LV SOURCE	100nf	C174
JS_JPU_ONE_8	JP10 JPU1 PI WEST LV SOURCE	100nf	C179
JS_JPU_ONE_9	JP10 JPU1 PI WEST LV SOURCE	100nf	C180
JS_JPU_ONE_10	JP10 JPU1 PI WEST LV SOURCE	100nf	C181
JS_JPU_ONE_11	JP10 JPU1 PI WEST LV SOURCE	100nf	C182
JS_JPU_ONE_12	JP10 JPU1 PI WEST LV SOURCE	100nf	C183
JS_JPU_ONE_13	JP10 JPU1 PI WEST LV SOURCE	100nf	C184
JS_JPU_ONE_14	JP10 JPU1 PI WEST LV SOURCE	100nf	C185
JS_JPU_ONE_15	JP10 JPU1 PI WEST LV SOURCE	100nf	C186
JS_JPU_ONE_16	JP10 JPU1 PI EAST LV RETURN	100nf	C163
JS_JPU_ONE_17	JP10 JPU1 PI EAST LV RETURN	100nf	C164
JS_JPU_ONE_18	JP10 JPU1 PI EAST LV RETURN	100nf	C173
JS_JPU_ONE_19	JP10 JPU1 PI EAST LV RETURN	100nf	C174
JS_JPU_ONE_20	JP10 JPU1 PI EAST LV RETURN	100nf	C175
JS_JPU_ONE_21	JP10 JPU1 PI EAST LV RETURN	100nf	C176
JS_JPU_ONE_22	JP10 JPU1 PI EAST LV RETURN	100nf	C177
JS_JPU_ONE_23	JP10 JPU1 PI EAST LV RETURN	100nf	C178
JS_JPU_ONE_24	JP10 JPU1 PI EAST LV RETURN	100nf	C179
JS_JPU_ONE_25	JP10 JPU1 PI EAST LV RETURN	100nf	C180
JS_JPU_ONE_26	JP10 JPU1 PI EAST LV RETURN	100nf	C181
JS_JPU_ONE_27	JP10 JPU1 PI EAST LV RETURN	100nf	C182
JS_JPU_ONE_28	JP10 JPU1 PI EAST LV RETURN	100nf	C183
JS_JPU_ONE_29	JP10 JPU1 PI EAST LV RETURN	100nf	C184
JS_JPU_ONE_30	JP10 JPU1 PI EAST LV RETURN	100nf	C185

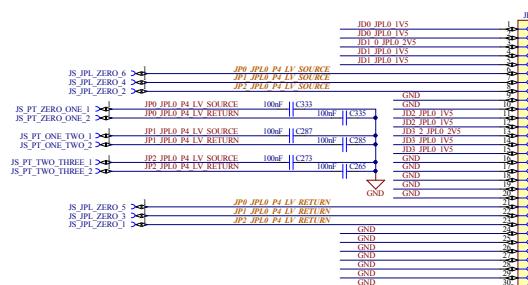
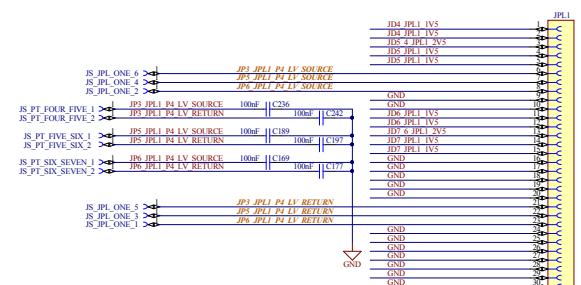
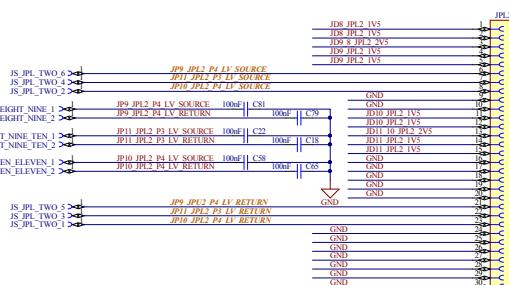
Fed by JPU0 on the Pigtail Power Breakout Brd

JS_JPU_ZERO_1	JP11 JPU0 PI WEST LV SOURCE	100nf	C252
JS_JPU_ZERO_2	JP10 JPU0 PI EAST LV SOURCE	100nf	C258
JS_JPU_ZERO_3	JP10 JPU0 PI EAST LV SOURCE	100nf	C257
JS_JPU_ZERO_4	JP10 JPU0 PI EAST LV SOURCE	100nf	C258
JS_JPU_ZERO_5	JP10 JPU0 PI EAST LV SOURCE	100nf	C259
JS_JPU_ZERO_6	JP10 JPU0 PI EAST LV SOURCE	100nf	C260
JS_JPU_ZERO_7	JP10 JPU0 PI WEST LV SOURCE	100nf	C262
JS_JPU_ZERO_8	JP10 JPU0 PI WEST LV SOURCE	100nf	C264
JS_JPU_ZERO_9	JP10 JPU0 PI WEST LV SOURCE	100nf	C265
JS_JPU_ZERO_10	JP10 JPU0 PI EAST LV SOURCE	100nf	C266
JS_JPU_ZERO_11	JP10 JPU0 PI EAST LV SOURCE	100nf	C267
JS_JPU_ZERO_12	JP10 JPU0 PI EAST LV SOURCE	100nf	C268
JS_JPU_ZERO_13	JP10 JPU0 PI EAST LV SOURCE	100nf	C269
JS_JPU_ZERO_14	JP10 JPU0 PI EAST LV SOURCE	100nf	C270
JS_JPU_ZERO_15	JP10 JPU0 PI EAST LV SOURCE	100nf	C271
JS_JPU_ZERO_16	JP10 JPU0 PI EAST LV RETURN	100nf	C163
JS_JPU_ZERO_17	JP10 JPU0 PI EAST LV RETURN	100nf	C164
JS_JPU_ZERO_18	JP10 JPU0 PI EAST LV RETURN	100nf	C173
JS_JPU_ZERO_19	JP10 JPU0 PI EAST LV RETURN	100nf	C174
JS_JPU_ZERO_20	JP10 JPU0 PI EAST LV RETURN	100nf	C175
JS_JPU_ZERO_21	JP10 JPU0 PI EAST LV RETURN	100nf	C176
JS_JPU_ZERO_22	JP10 JPU0 PI EAST LV RETURN	100nf	C177
JS_JPU_ZERO_23	JP10 JPU0 PI EAST LV RETURN	100nf	C178
JS_JPU_ZERO_24	JP10 JPU0 PI EAST LV RETURN	100nf	C179
JS_JPU_ZERO_25	JP10 JPU0 PI EAST LV RETURN	100nf	C180
JS_JPU_ZERO_26	JP10 JPU0 PI EAST LV RETURN	100nf	C181
JS_JPU_ZERO_27	JP10 JPU0 PI EAST LV RETURN	100nf	C182
JS_JPU_ZERO_28	JP10 JPU0 PI EAST LV RETURN	100nf	C183
JS_JPU_ZERO_29	JP10 JPU0 PI EAST LV RETURN	100nf	C184
JS_JPU_ZERO_30	JP10 JPU0 PI EAST LV RETURN	100nf	C185

EACH Power Group receives SOURCE power from a single Maraton Channel.

The Maraton Channel is indirectly connected to system power ground via the ground sense resistor connections (ie one per 4-ASICs)

LOWER Power Conns--(All DCB slot power routes and a few pigtail power routes)



NOTE: (1) The pigtail power lines on JPL2, JPL1, and JPL0 get routed via the individual JS contacts to the PIGTAIL_POWER_Breakout_PCB.

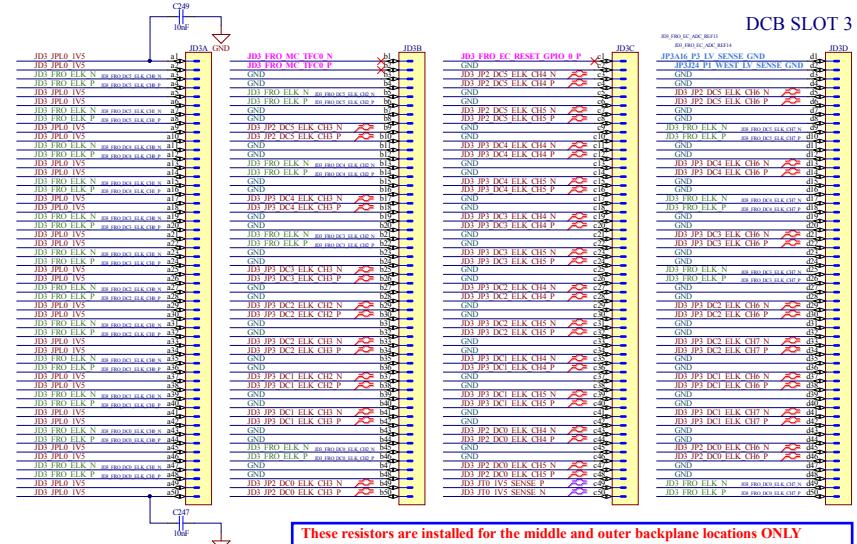
(2) Each DCB slot uses 1 master + 1 slave channel. Both connector pins are labeled '_1V5'. Therefore, one is for the Master cable and the second is for the slave cable.

(3) The power group 'returns' being joined together also prevents any unused pigtail and Stave flex cable tracks from being left floating.

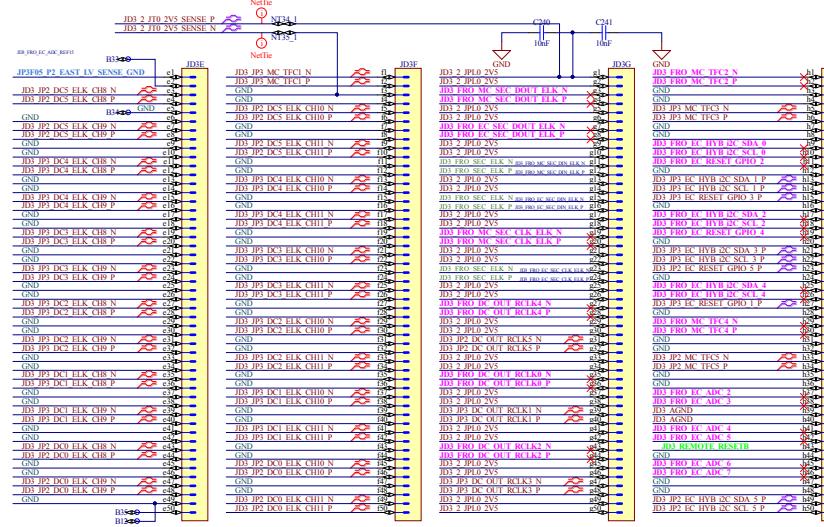
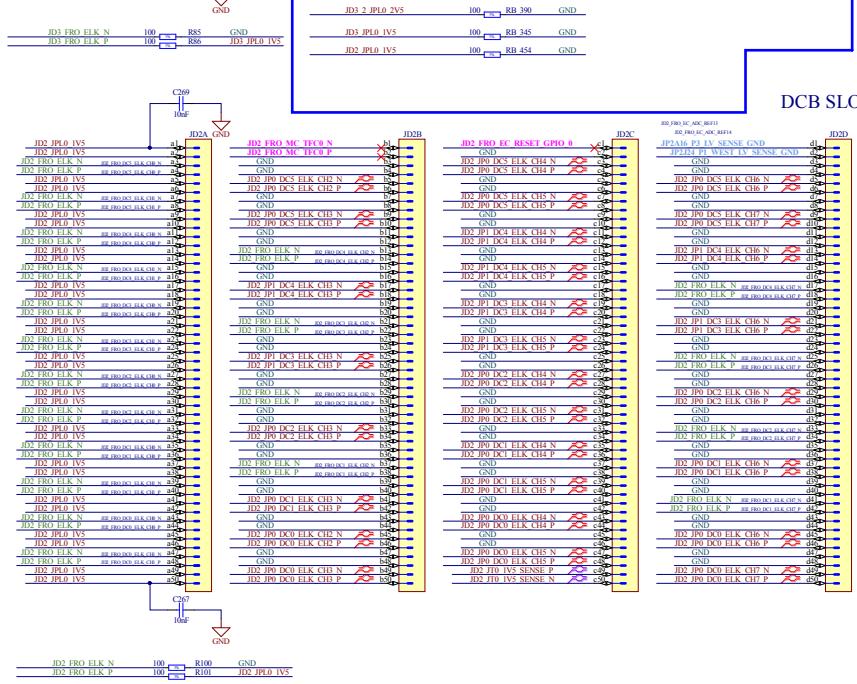
(4) The power group 'Source' lines in depopulated 'beta' and 'gamma' BP positions are connected via resistors with designators R_B? and R_G?, respectively, to the associated power group returns to avoid being left floating.

ProjectEquipment -		Designer _____	Designer Drawn by _____	XX/XXXXXX
Document _____		Title _____	Title _____	
TE/MP/E _____		- Power Bank Conn's -	- Power Bank Conn's -	
18 SEPTEMBER 2019		European Organization for Nuclear Research CERN/GENEVA-23-Switzerland		Sheet 1 of 21
FILE: Power Bank Conn.SchDwg		FILE: Power Bank Conn.SchDwg		A2 -
Printed on 10/10/2019 at 10:00 AM		Printed on 10/10/2019 at 10:00 AM		
EDA-XXXXXX-VX-X				

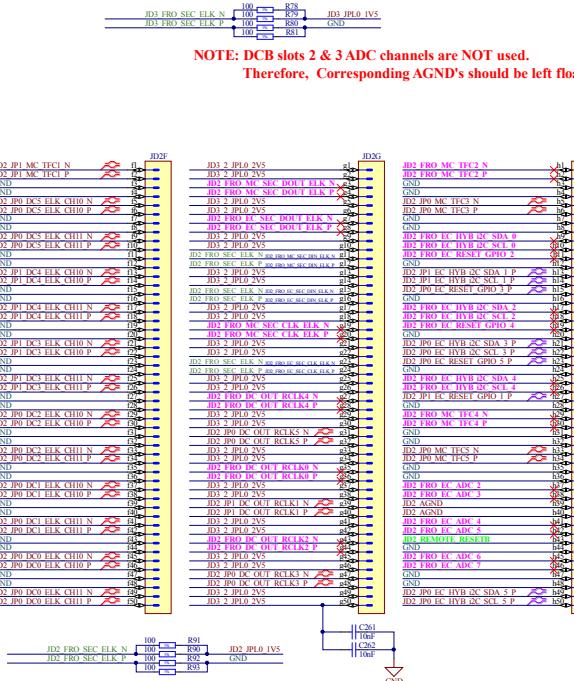




These resistors are installed for the middle and outer backplane locations ONLY



**NOTE: DCB slots 2 & 3 ADC channels are NOT used.
Therefore, Corresponding AGND's should be left floating.**

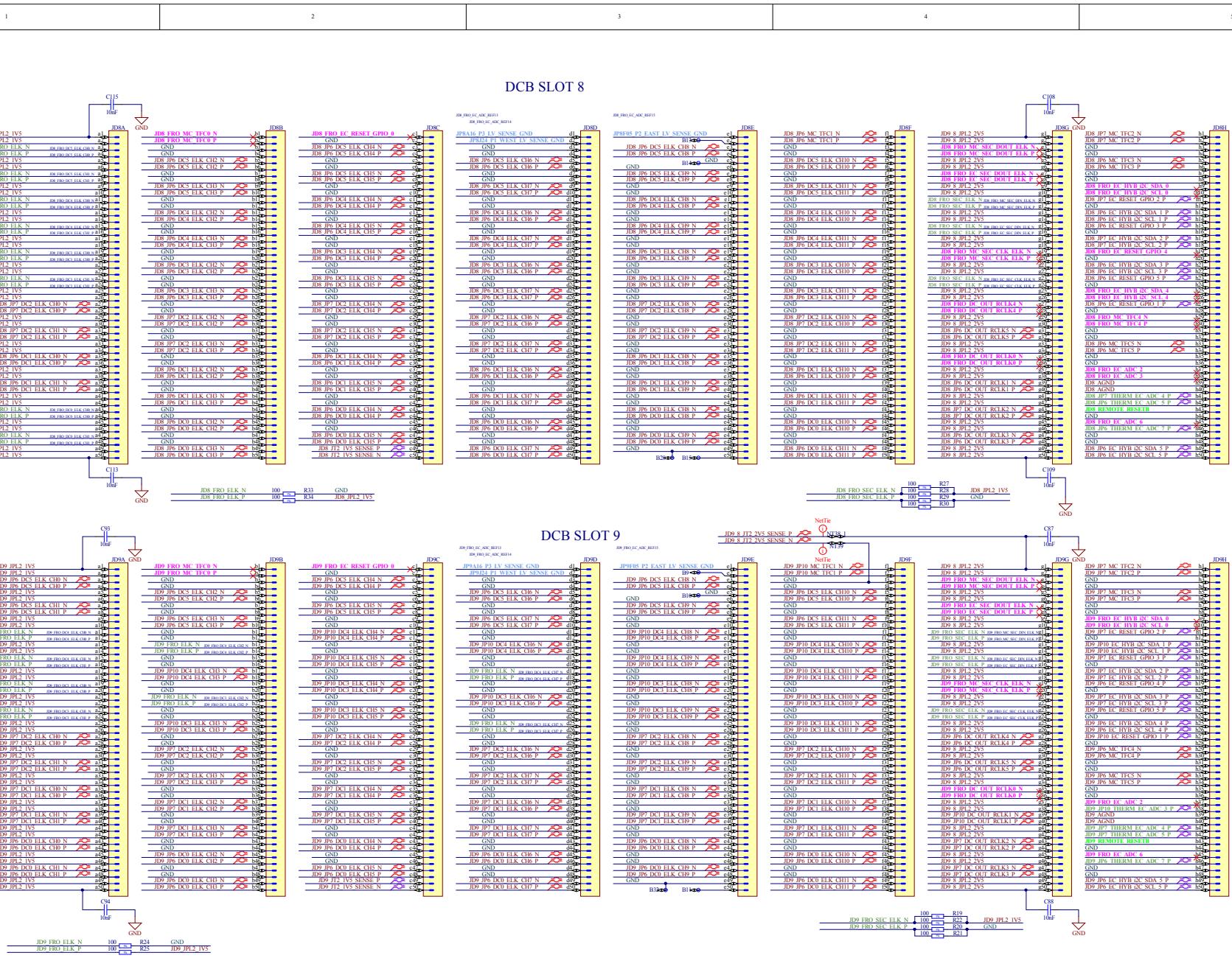


ProjectEquipment		Designer	Designer
Document		Drawn by	XN/XN/XXXX
	Title	Check by	-
	Title2	Last Mod.	8/27/2019
		File	DCB Comis 2.mnSchnell
		Last modified by: [Signature]	
European Organization for Nuclear Research CH-1211 Genvee 23 - Switzerland		Sheet 5 of 21	
		EDA-XXXXX-VX-X	
		A2	Rev B

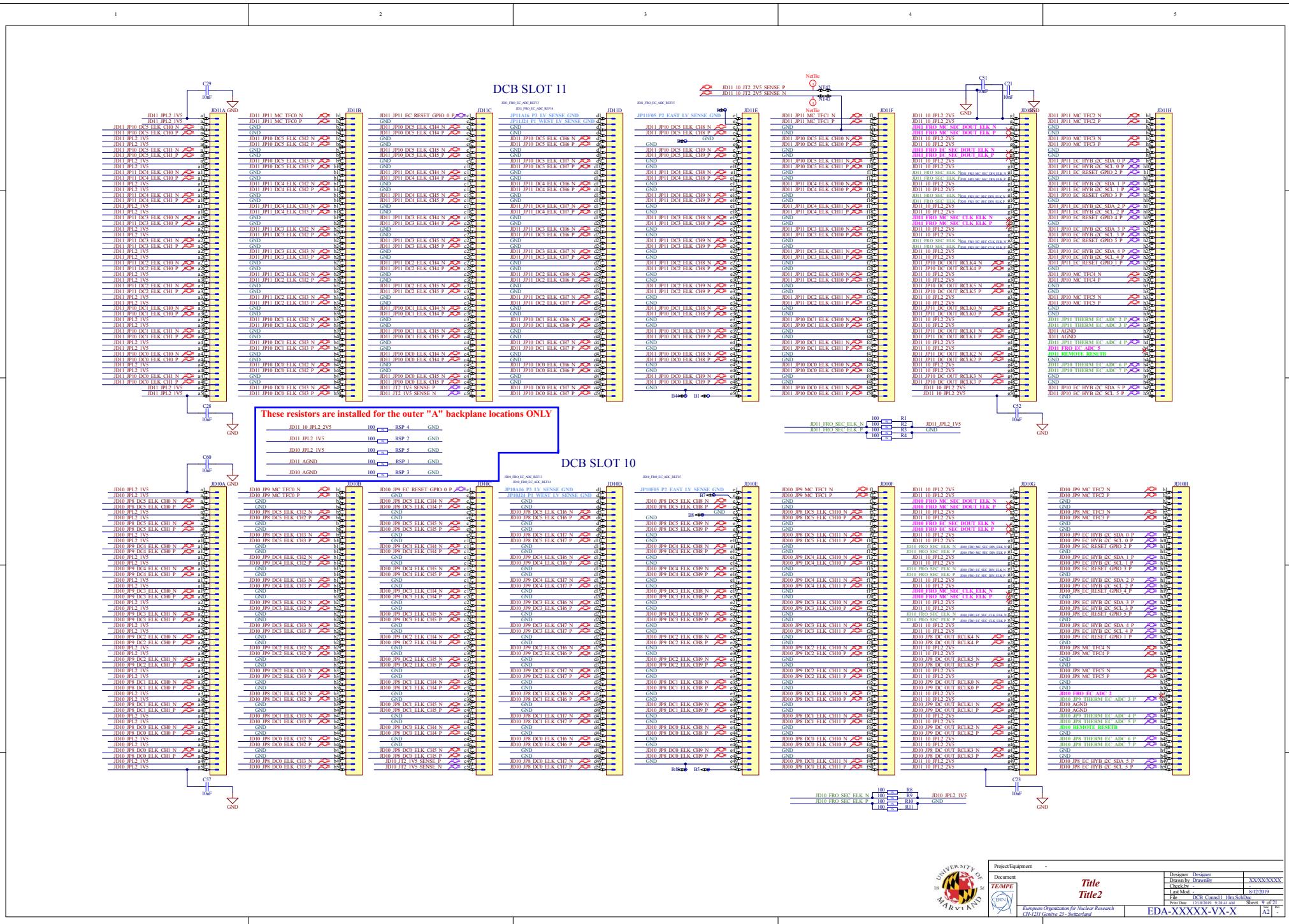


Project/Equipment	PEPI
Document	PEPI Backplane Mirror DCB Slot Connector 4 & 5
TEMPA	Drafter: M. Franco Sevilla Drafter by: M. Franco Sevilla Check by: B Cuel Last Mod: B Cuel DCB Comm: 4m Schell Print Date: 04/06/2019
CIRAS	01/05/2019 04/06/2019 07/05/2019 Sheet 6 of 21
European Organization for Nuclear Research CERN-1111 Geneva 23 Switzerland	
EDA-04066-VI-0	
Rev. A2 -	

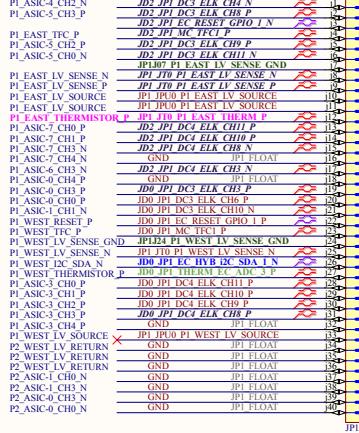
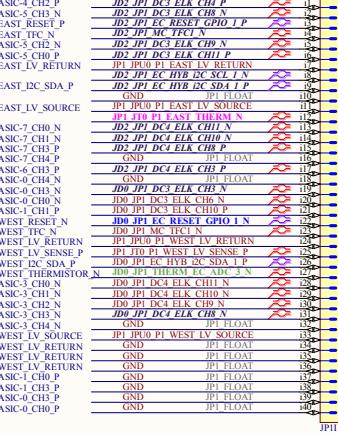
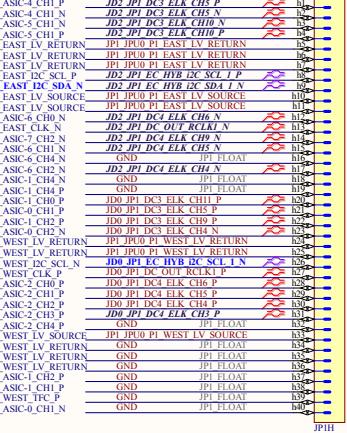
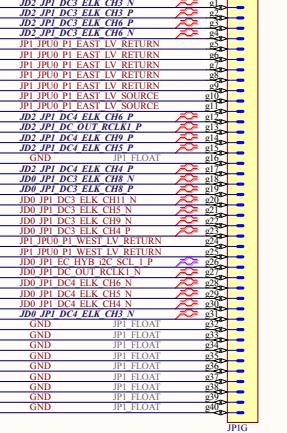
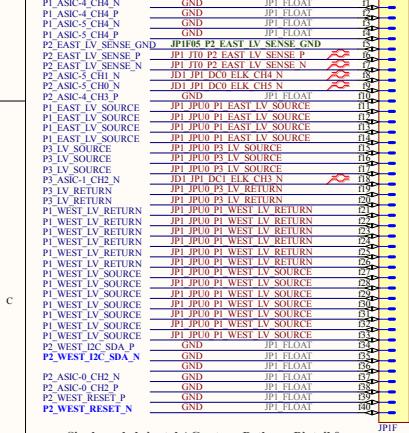
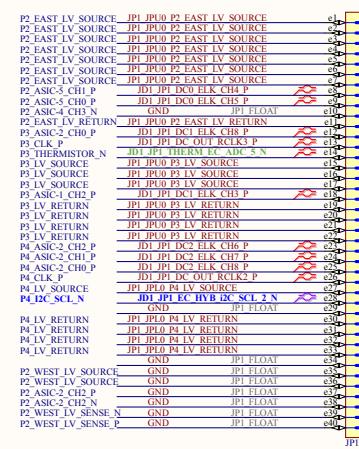
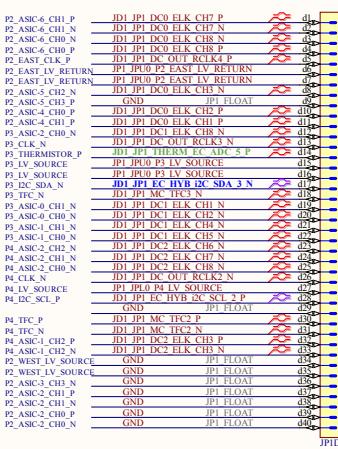
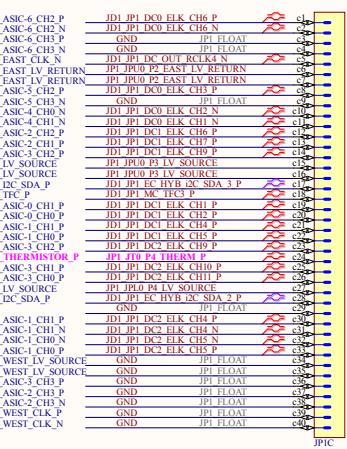
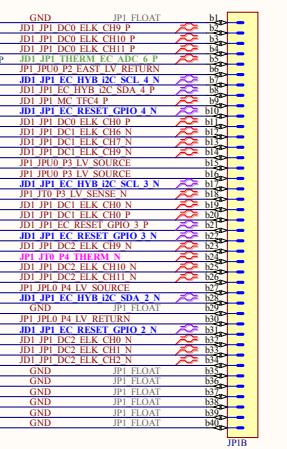
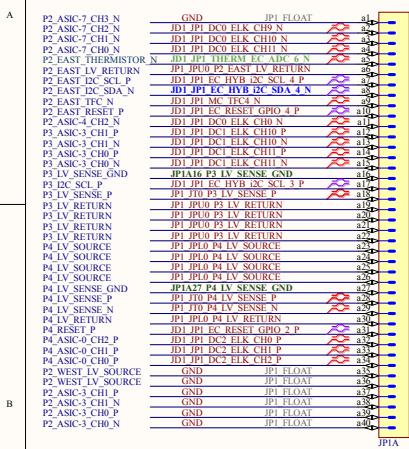




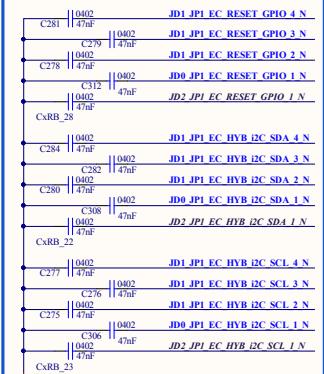
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European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland			
EDA-XXXXX-VX-X			



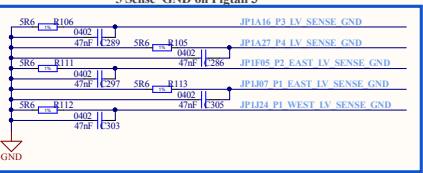
Pigtail 1



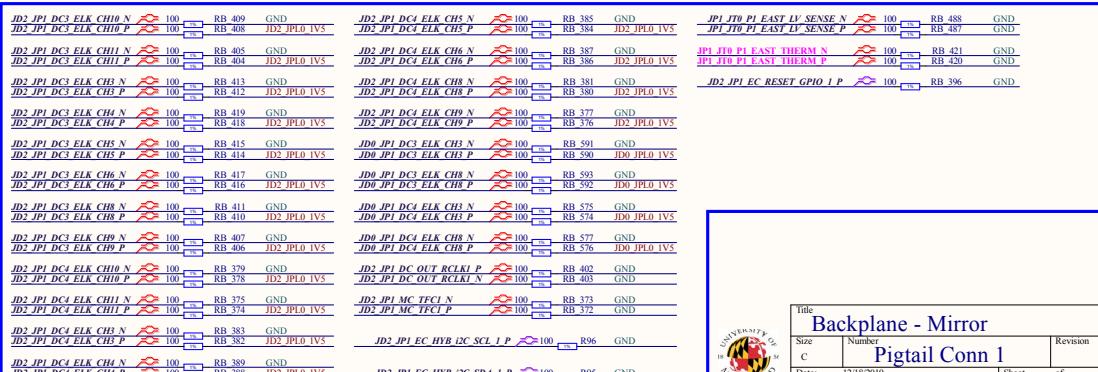
Single-ended signal AC return Paths on Pigtail 0



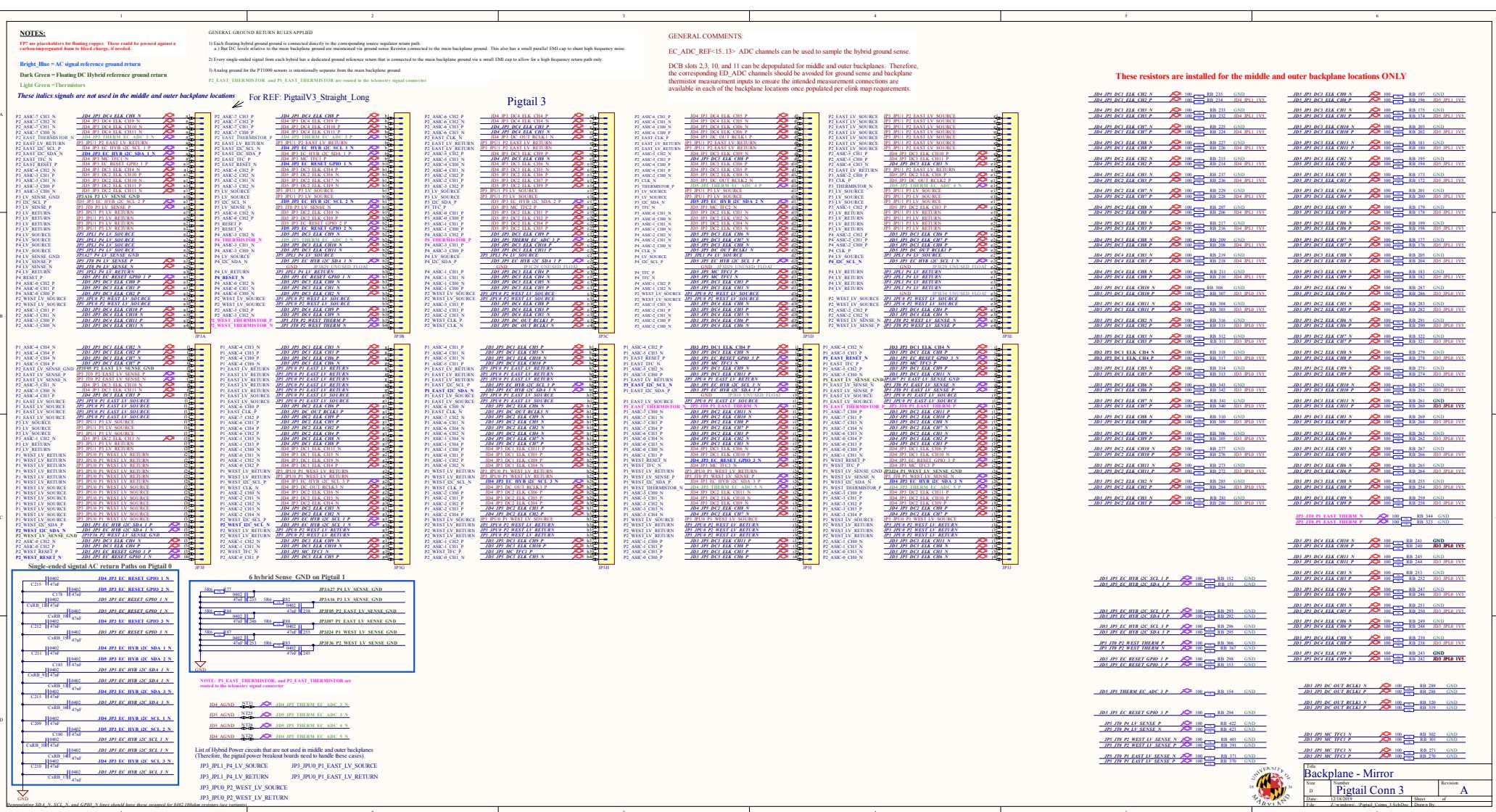
NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector



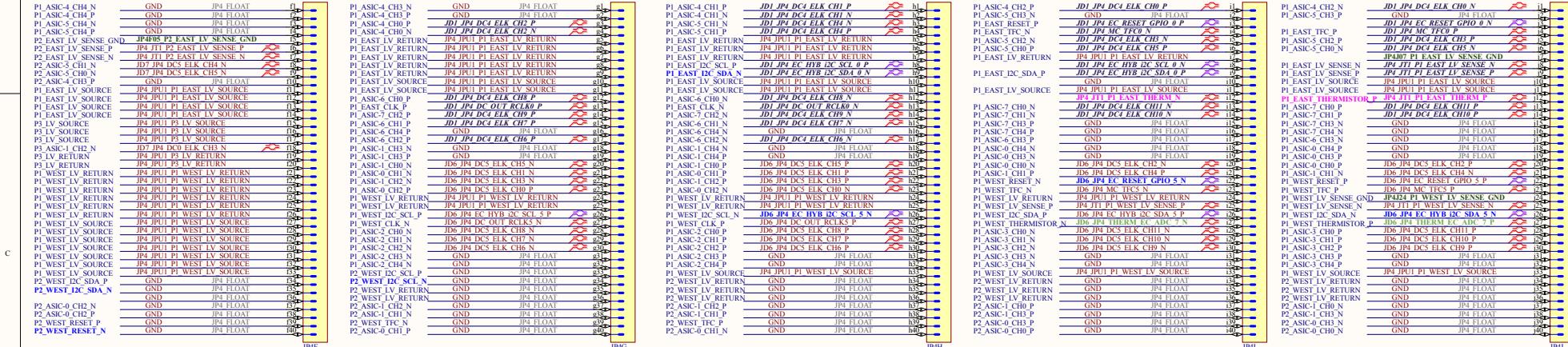
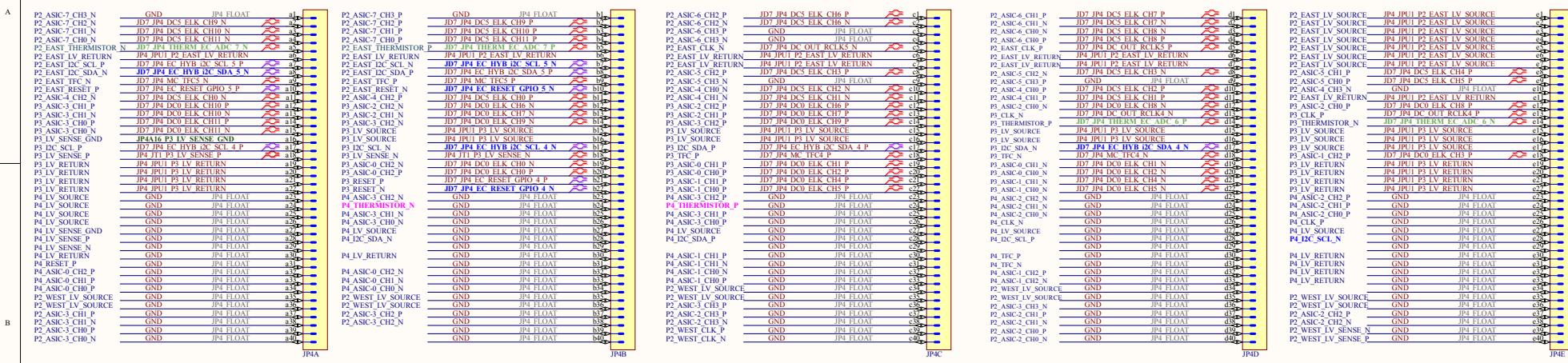
These resistors are installed for the middle and outer backplane locations ONLY



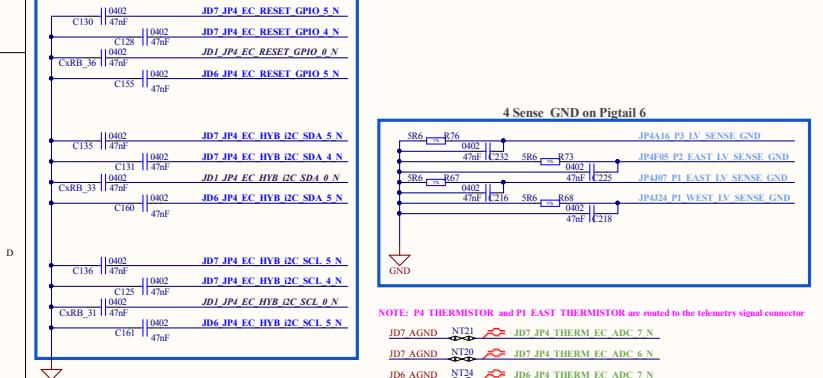
 *Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)*



Pigtail 4



Single-ended signal AC return Paths on Pigtail 6

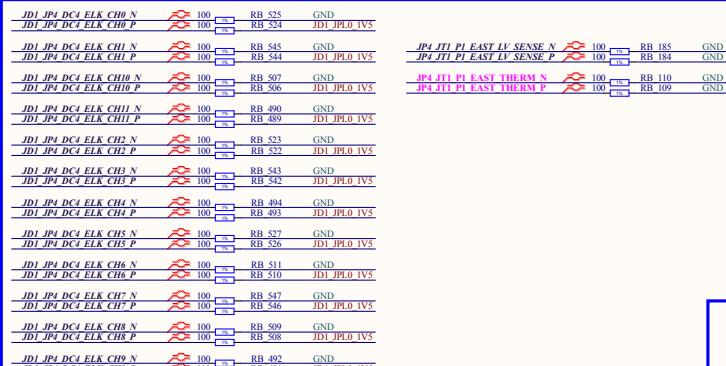


NOTE: P4 THERMISTOR and P1 EAST THERMISTOR are routed to the telemetry signal connector

JD7 AGND	NT21		JD7 JP4 THERM EC ADC 7_N
JD7 AGND	NT20		JD7 JP4 THERM EC ADC 6_N
JD6 AGND	NT24		JD6 JP4 THERM EC ADC 7_N

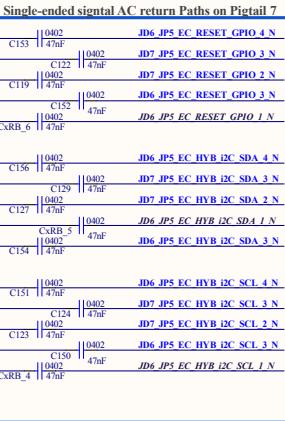
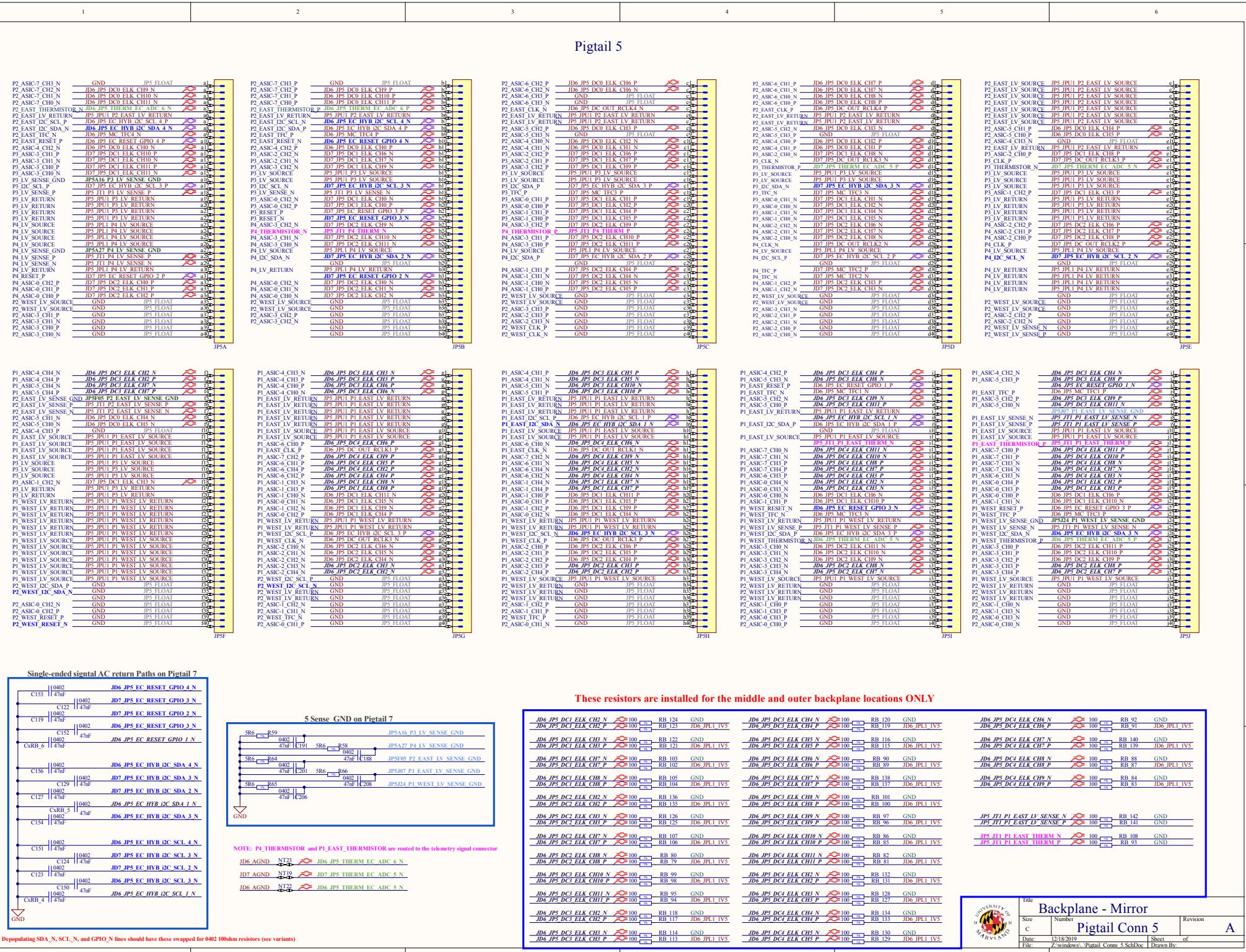
• 88 •

These resistors are installed for the middle and outer backplane locations ONLY



Title Backplane - Mirro

Backplane - M101		
Size	Number	Revision
C	Pigtail Conn 4	



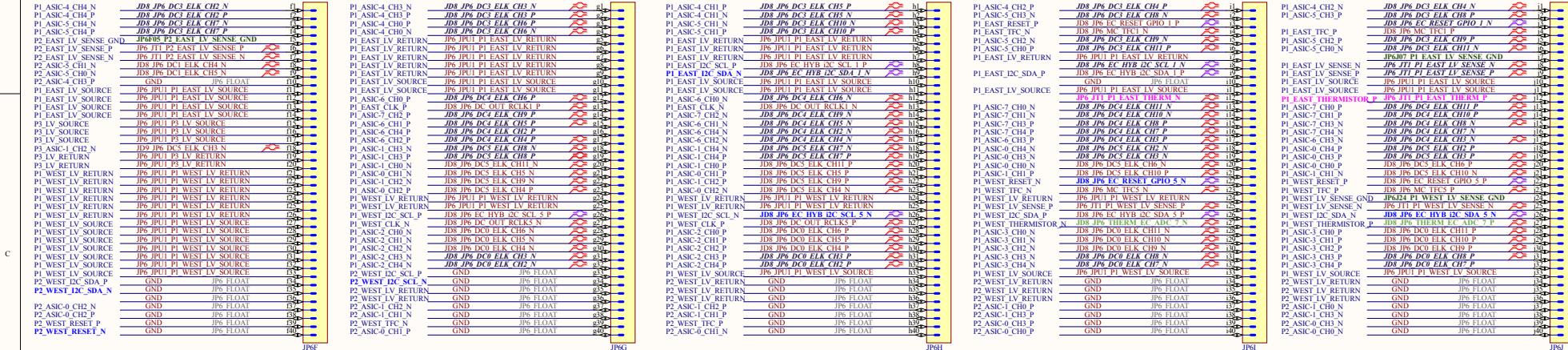
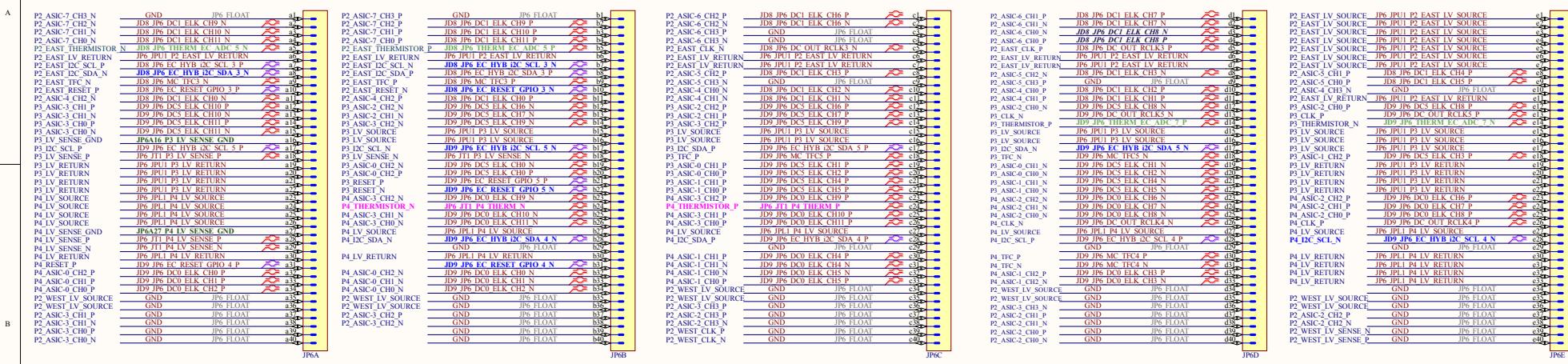
Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)



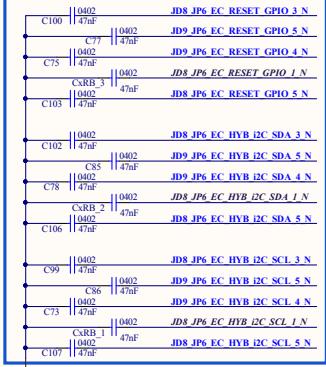
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6

Pigtail 6



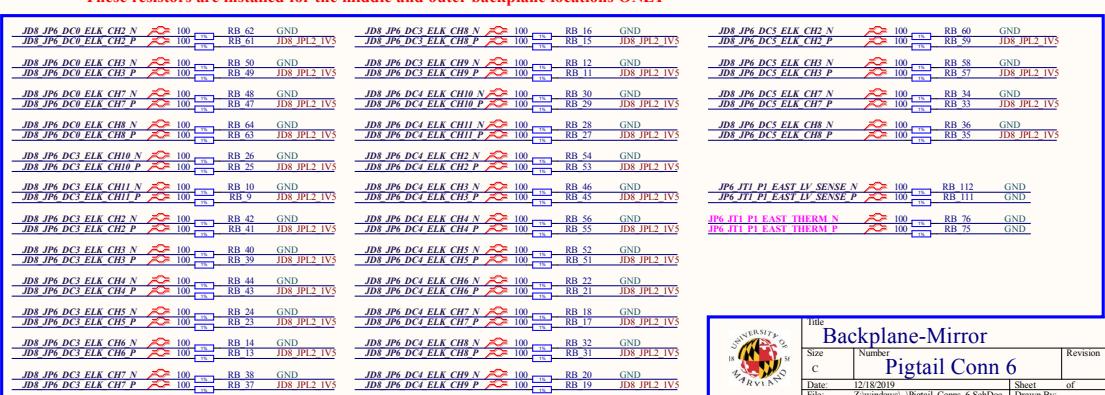
Single-ended signal AC return Paths on Pigtail 0

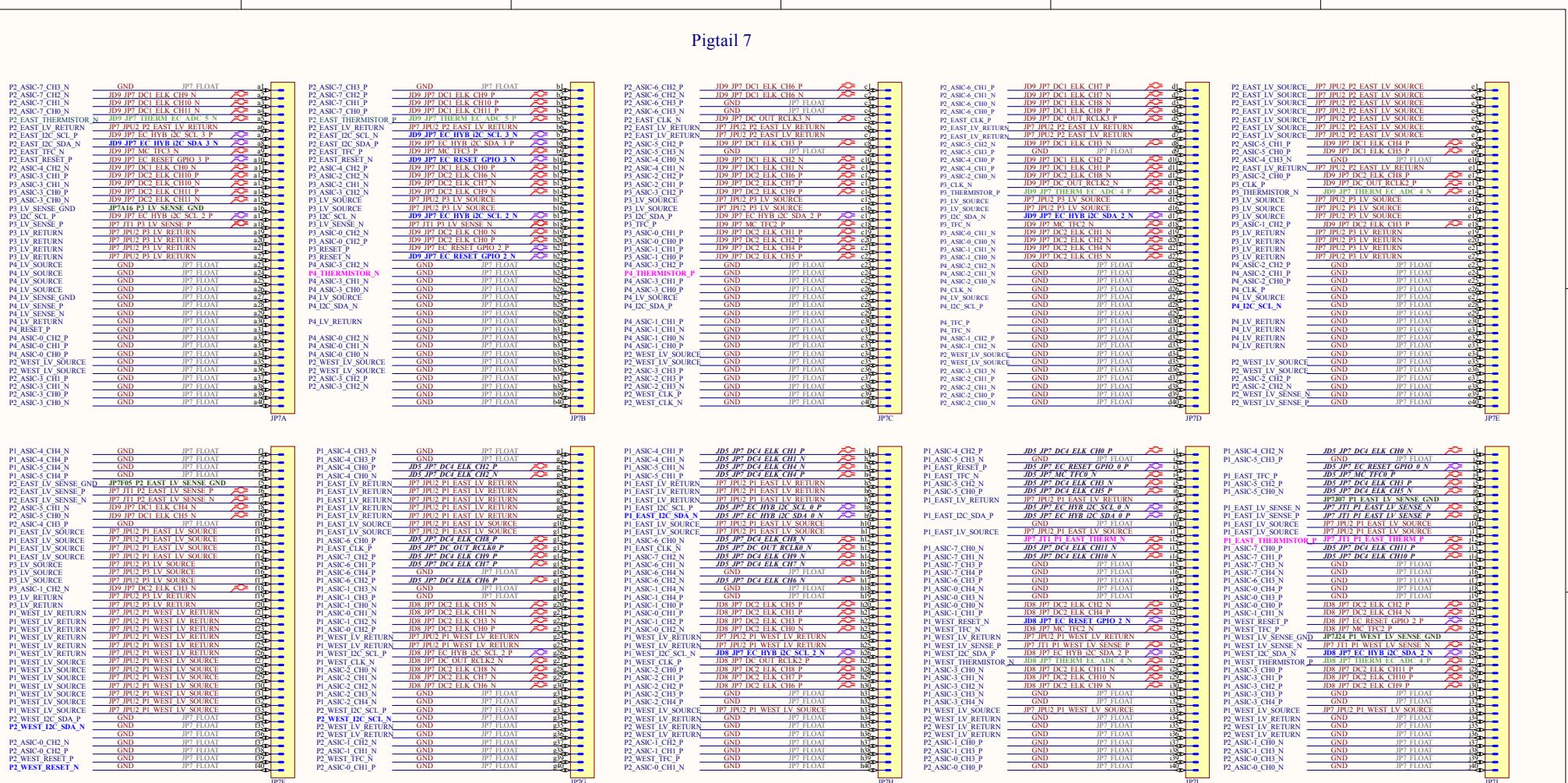


NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

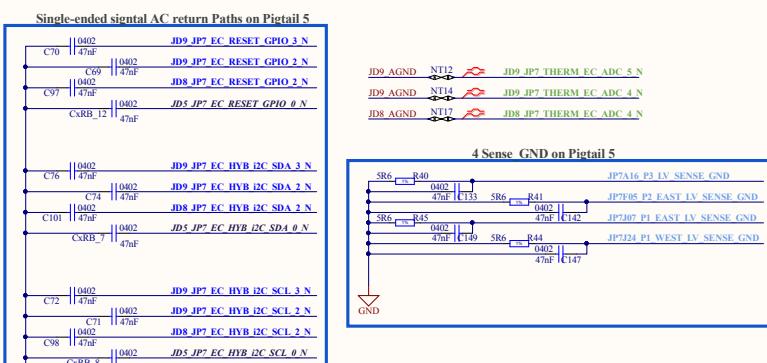
JD8 AGND	NT15		JD8 JP6 THERM FC ADC 5 N
JD9 AGND	NT13		JD9 JP6 THERM FC ADC 7 N

populating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

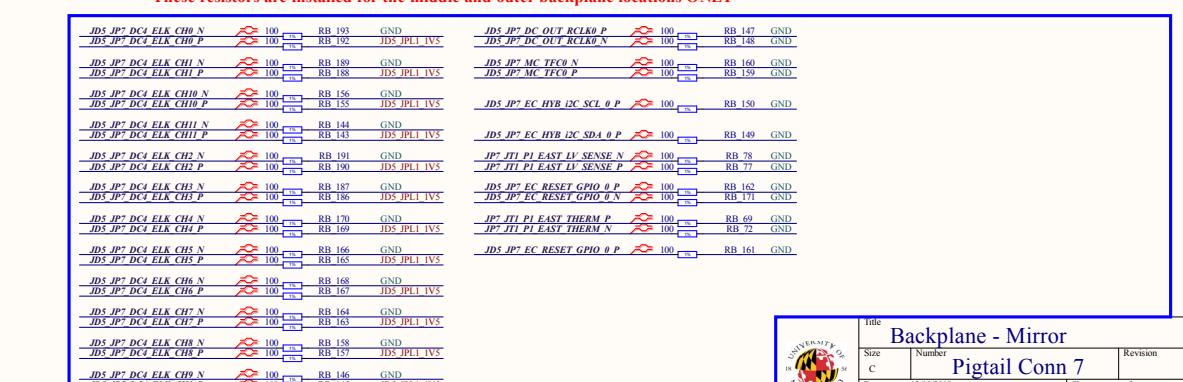




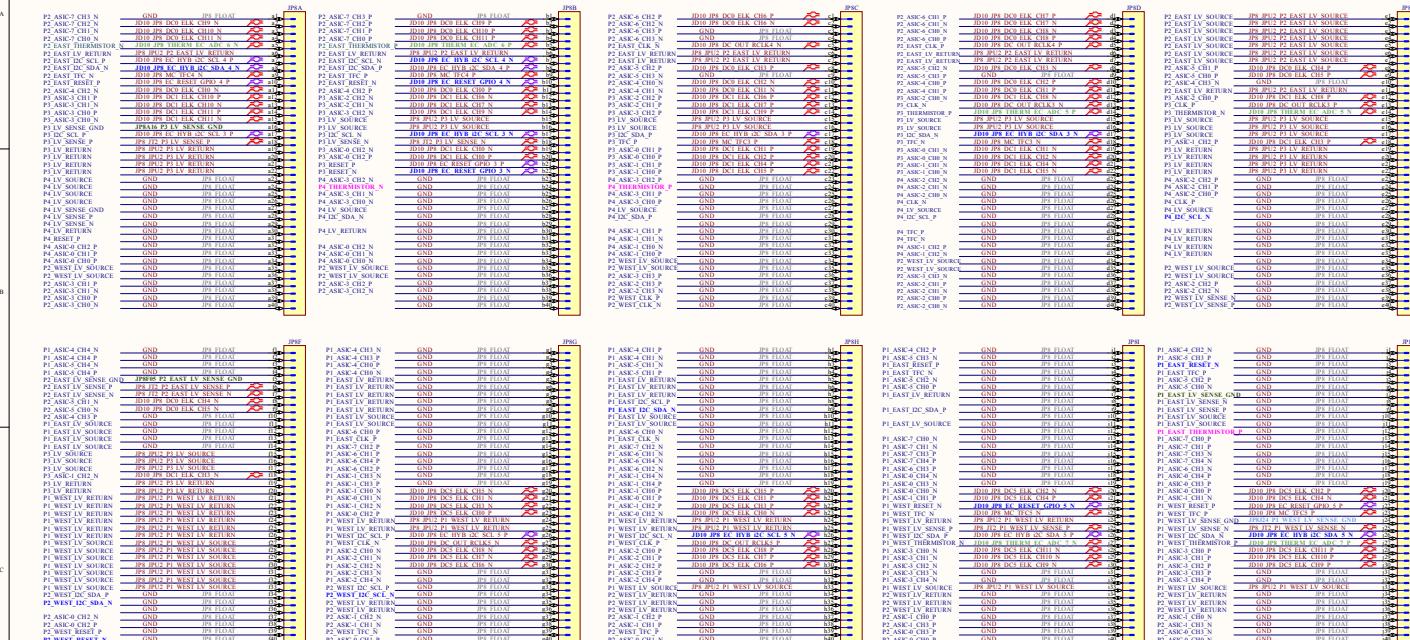
These resistors are installed for the middle and outer backplane locations ONLY



J. Lat. Amer. Stud. 39 (2007). DOI: 10.1017/S0022216X07008300 © Cambridge University Press 2007

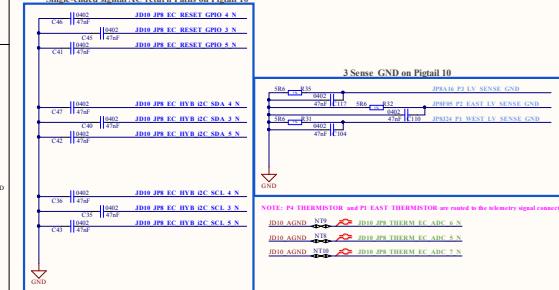


Pigtail 8



**These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtales JP<8 .. 11> are absent)**

Single-ended signal AC return Paths on Pigtail 19



Title
Backplane - Mirror

NOTE: P4 THERMISTOR and P1 EAST THERMISTOR are routed to the telemetry signal connector.

JD10 AGND NT9 JD10 JP8 THERM EC ADC 6 N

JD10 AGND NTB **JD10 JP8 THERM EC ADC S N**

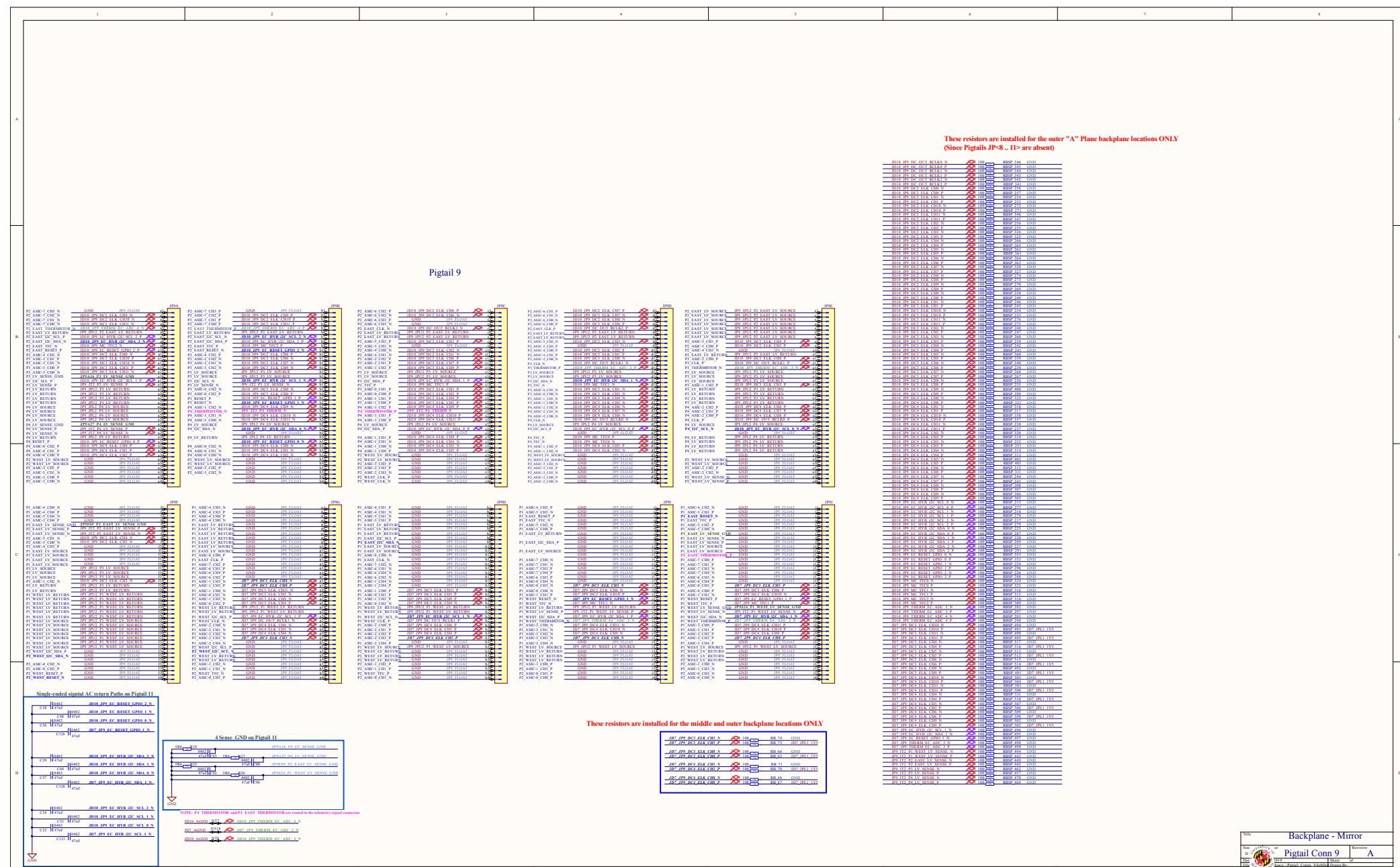
JD10 AGND N100 JD10 JP8 THERM EC ABC 7 N

For more information about the study, please contact Dr. Michael J. Hwang at (310) 206-6500 or via email at mhwang@ucla.edu.

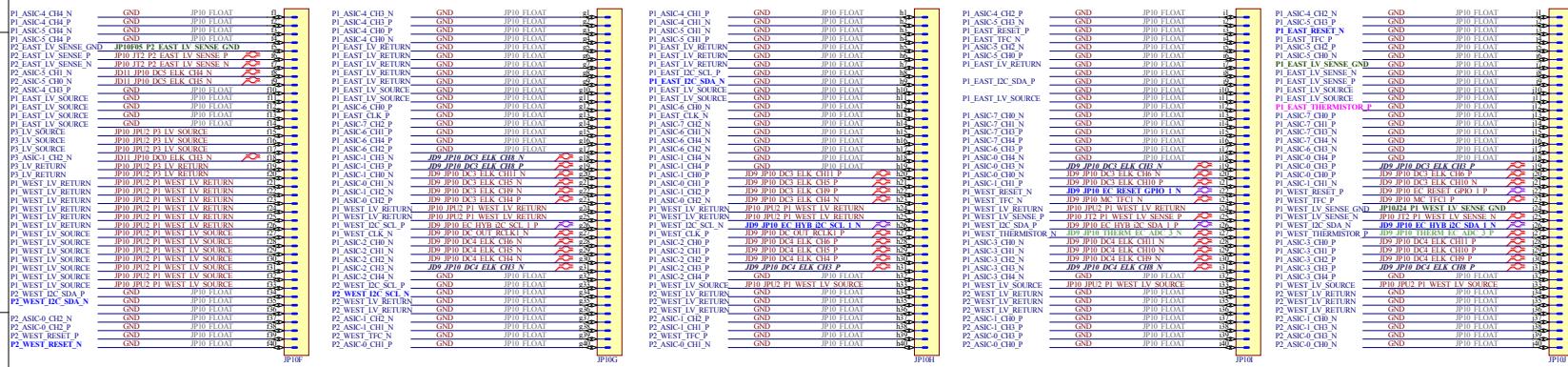
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2

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These resistors are installed for the middle and outer backplane locations ONLY



**These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtales JP<8 .. 11> are absent)**





Backplane - Mirror