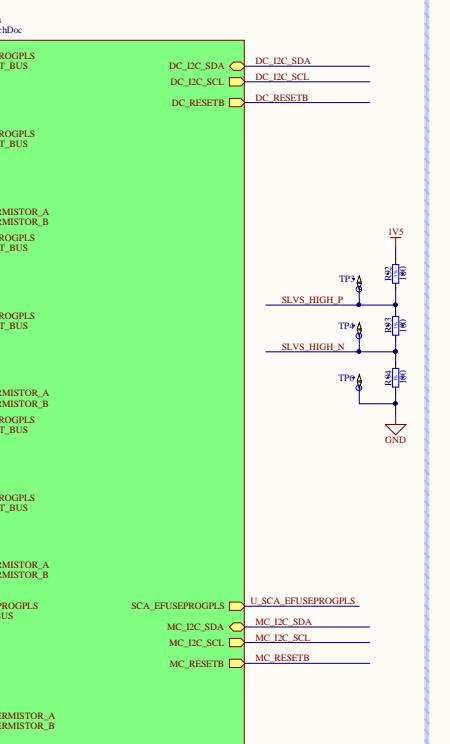
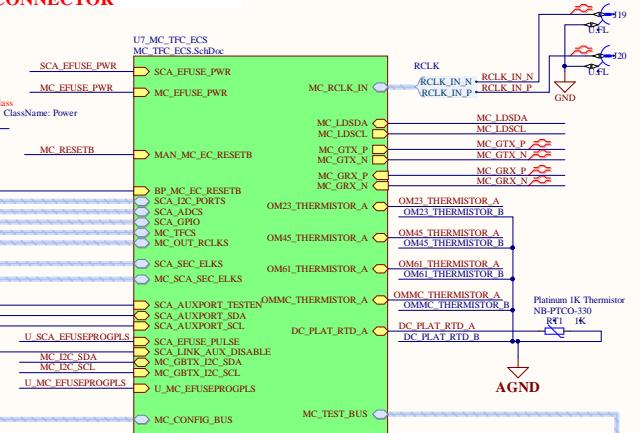
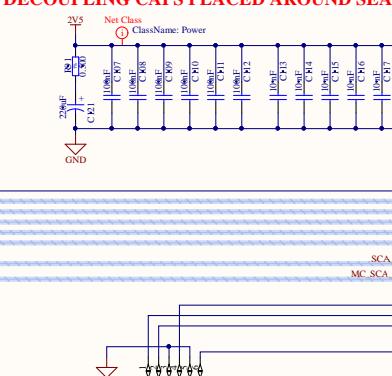
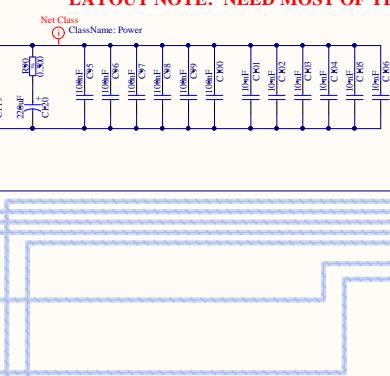
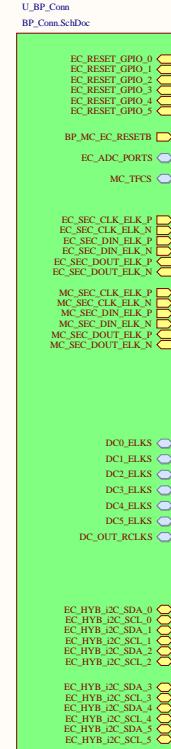


LAYOUT NOTE: NEED MOST OF THESE DECOUPLING CAPS PLACED AROUND SEAM-RA CONNECTOR



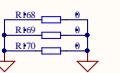
Combined_DC_Mc_PCB_Project.PrjPcb

Title	Data Control Board (DCB) Schematic		
Size	Number	Top Combined DC + MCB Hierarchy	Revision
C	Sheet 0 of 0	A	
Date:	9/16/2019	File:	C:\Users\...\Top_Combined_DC_Mc_PCB_SchDoc\By: Tom O'Bannon

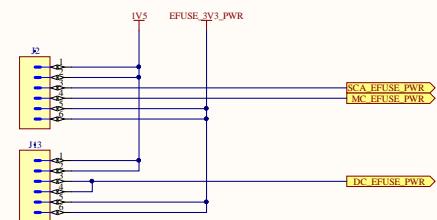
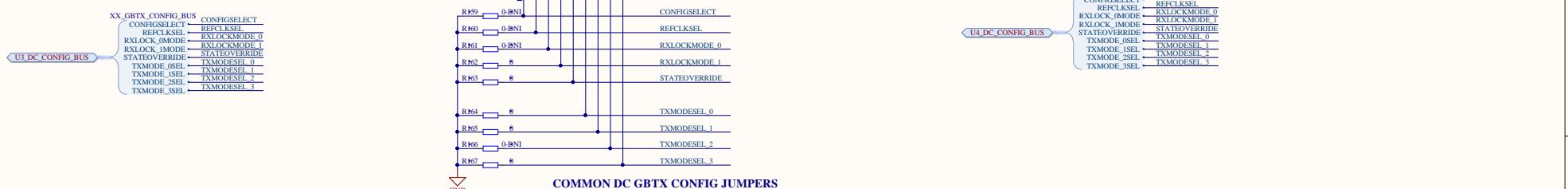
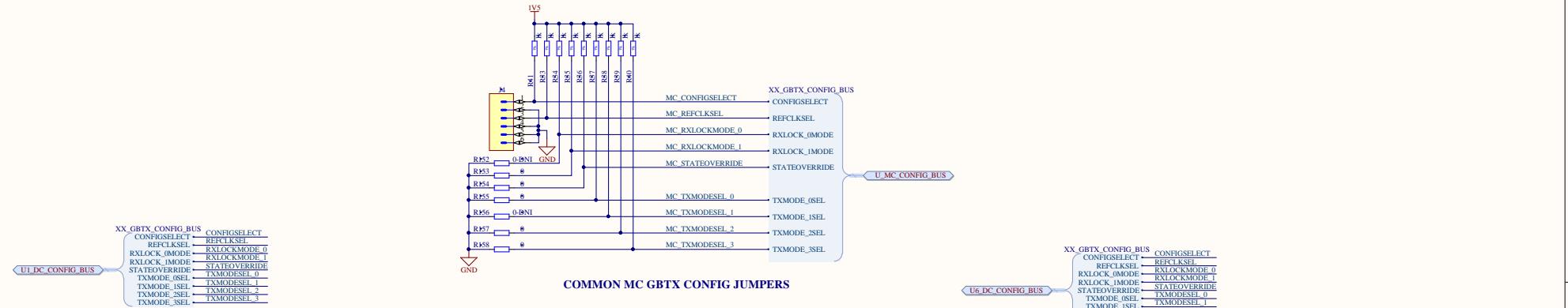
Notes:

- (1) Pinout symmetrical which support either mate orientation.
- (2) Net Class: ClassName: TopLayer--Must be routed on the top side only without using any vias.
- (3) -15mm of OUTER PCB EDGES (+ addl 5 mm for aluminum heat sink plate) ARE ALLOCATED FOR HEAT PIPES.
- (4) Circuit side of the board has 2mm thick aluminum heat sink plate. Pockets will be milled for small decoupling caps (0201 and 0402 only) to be located under the GBT components. Aluminum heat sink plate extends ~5mm beyond each card guide edge of the PCB. IE the PCB is fully supported only via the aluminum heat sink edges when installed in the card cage.

Thermal Spreader Attachment Holes



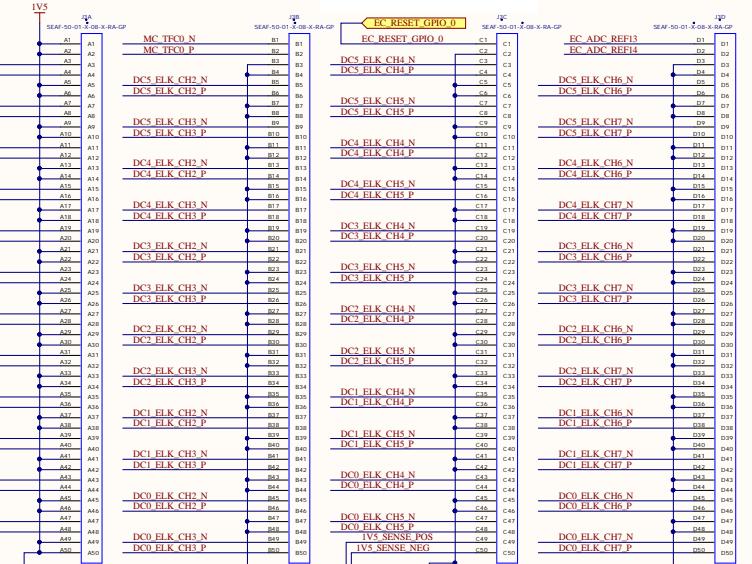
A



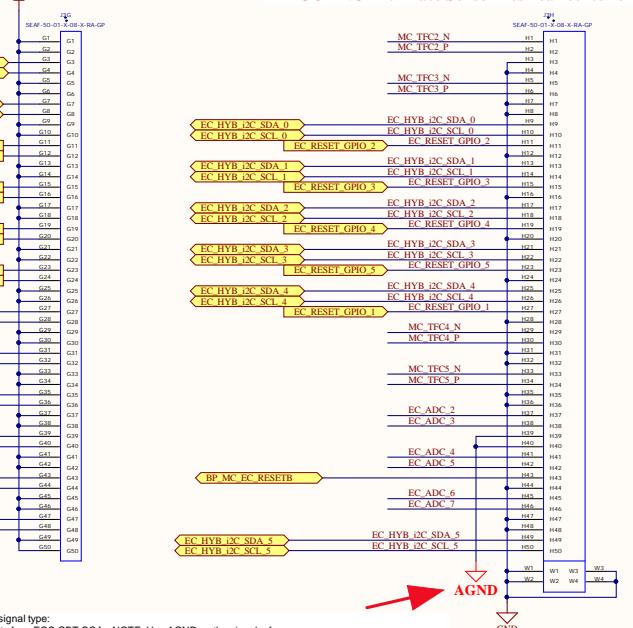
Title Data Control Board (DCB) Schematic		
Size	Number	Revision
C	Config_and_Test_comms.SchDoc	B
Date:	9/16/2019	Sheet 9 of 10
File:	C:\Users\...\Config_and_Test_comms.SchDoc	Drawn By: Tom O'Bannon

LAYOUT NOTE: NEED DECOUPLING CAPS PLACED AROUND SEAM-RA

72 links (6 GBTx-DC x 12)



LAYOUT NOTE: Place Sense lines near center of Board.

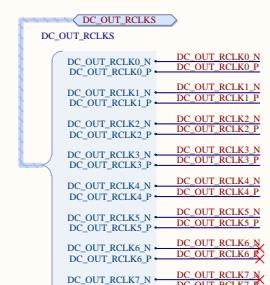
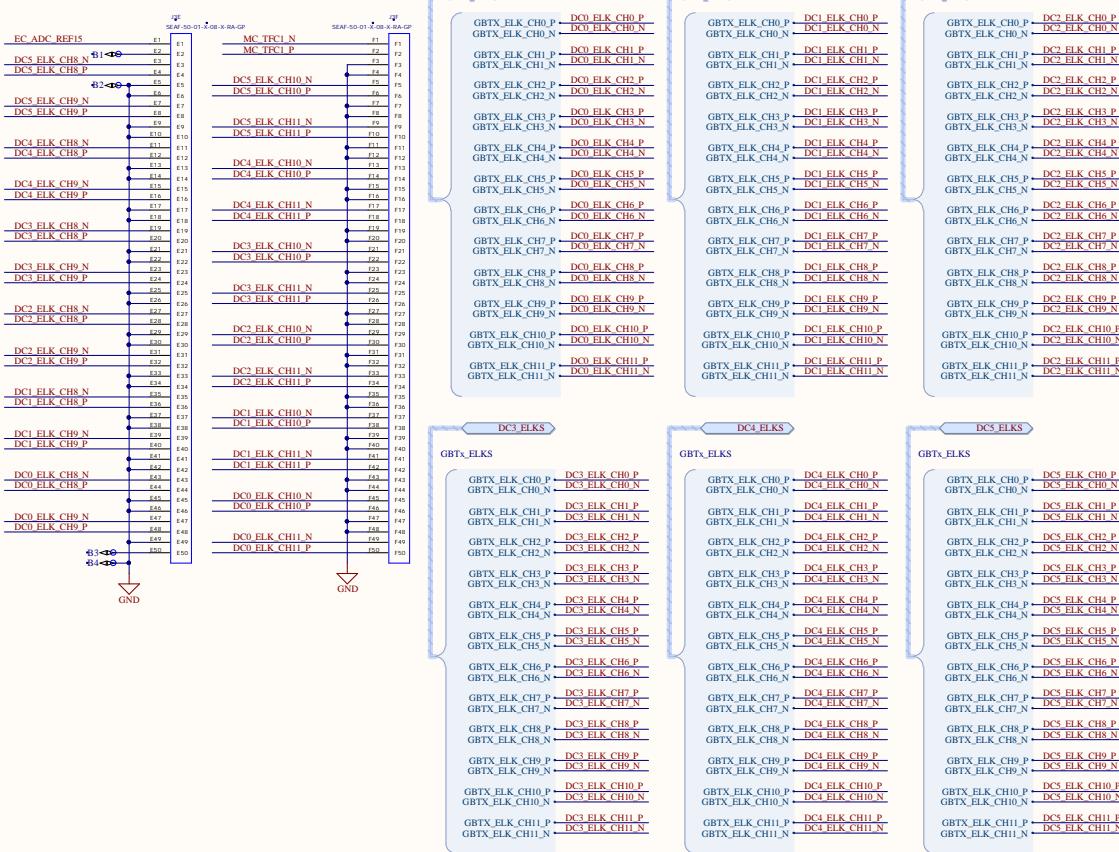


x6 sets of signals for each signal type:

EC_ADC[7:2]: ADC inputs from EGS GBT-SCA --NOTE: Use AGND as the signal reference.
DC_OUT_RCLK[5:0]: GBTx data concentrator reference clock outputs for the hybrids
MC_TFC[5:0]: Master control GBTx TFC for hybrids.
EC_RESET_GPIO[5:0]: ECS generated reset from GBT-SCA (Also available as general digital I/O)
EC_HYB_I2C_SDA[5:0]: ECS generated 12C busses for hybrids

Redundant secondary GBT-SCA control ports:
MC_SEC_ELK: Secondary ECS Elink (DIN, DOUT, and CLK) from GBTx-Master for control of adjacent board GBT-SCA
EC_SEC_ELK: Secondary ECS Elink (DIN, DOUT, and CLK) from adjacent board GBTx-Master for control of GBT-SCA

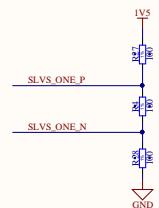
ADC ports for hybrid ground sense measurement:
EC_ADC_xx



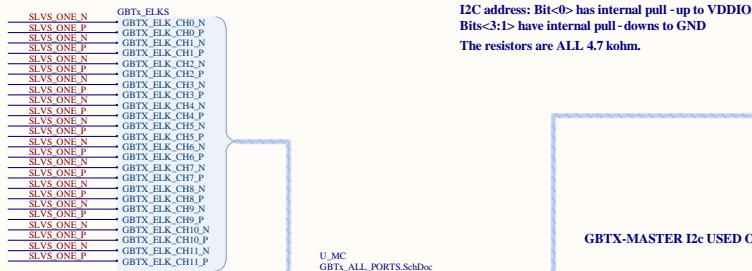
NEW DC SLOT RULES
1) 6 TFC , 6 i2C, 6 ADC, 6 REFCLKs, 6 RESET

Title Data Control Board (DCB) Schematic		
Size	Number	Revision
C	BP.Conn.SchDoc	B
Date: 9/16/2019	Sheet 2 of 10	
File: C:\Users\JPB.Conn.SchDoc	Drawn By: Tom O'Bannon	

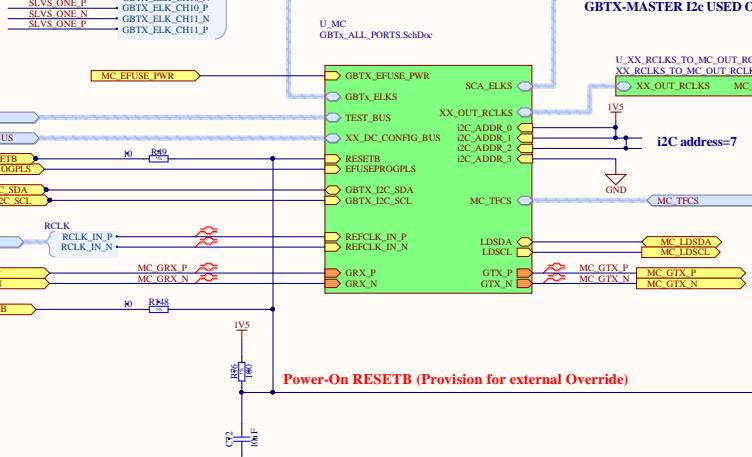
A



B



C



Power-On RESETB (Provision for external Override)

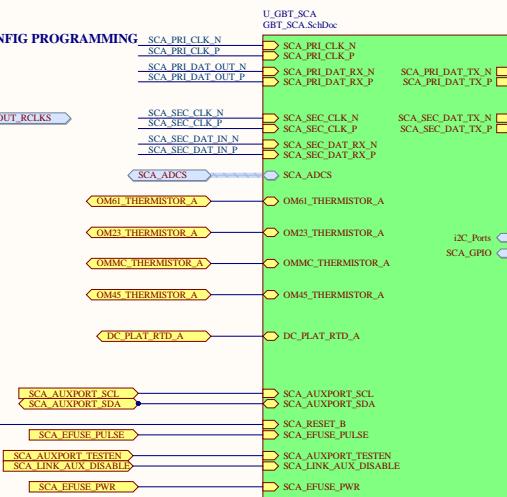
I2C address=7

SCA_ELKs
SCA_PRI_CLK_N
SCA_PRI_CLK_P
SCA_PRI_DAT_IN_N
SCA_PRI_DAT_IN_P
SCA_PRI_DAT_OUT_N
SCA_PRI_DAT_OUT_P
SCA_PRI_DAT_OUT_U
SCA_PRI_DAT_OUT_U_P
SCA_SEC_CLK_N
SCA_SEC_CLK_P
SCA_SEC_DAT_IN_N
SCA_SEC_DAT_IN_P
SCA_SEC_DAT_OUT_N
SCA_SEC_DAT_OUT_P
SCA_SEC_DAT_OUT_U
SCA_SEC_DAT_OUT_U_P

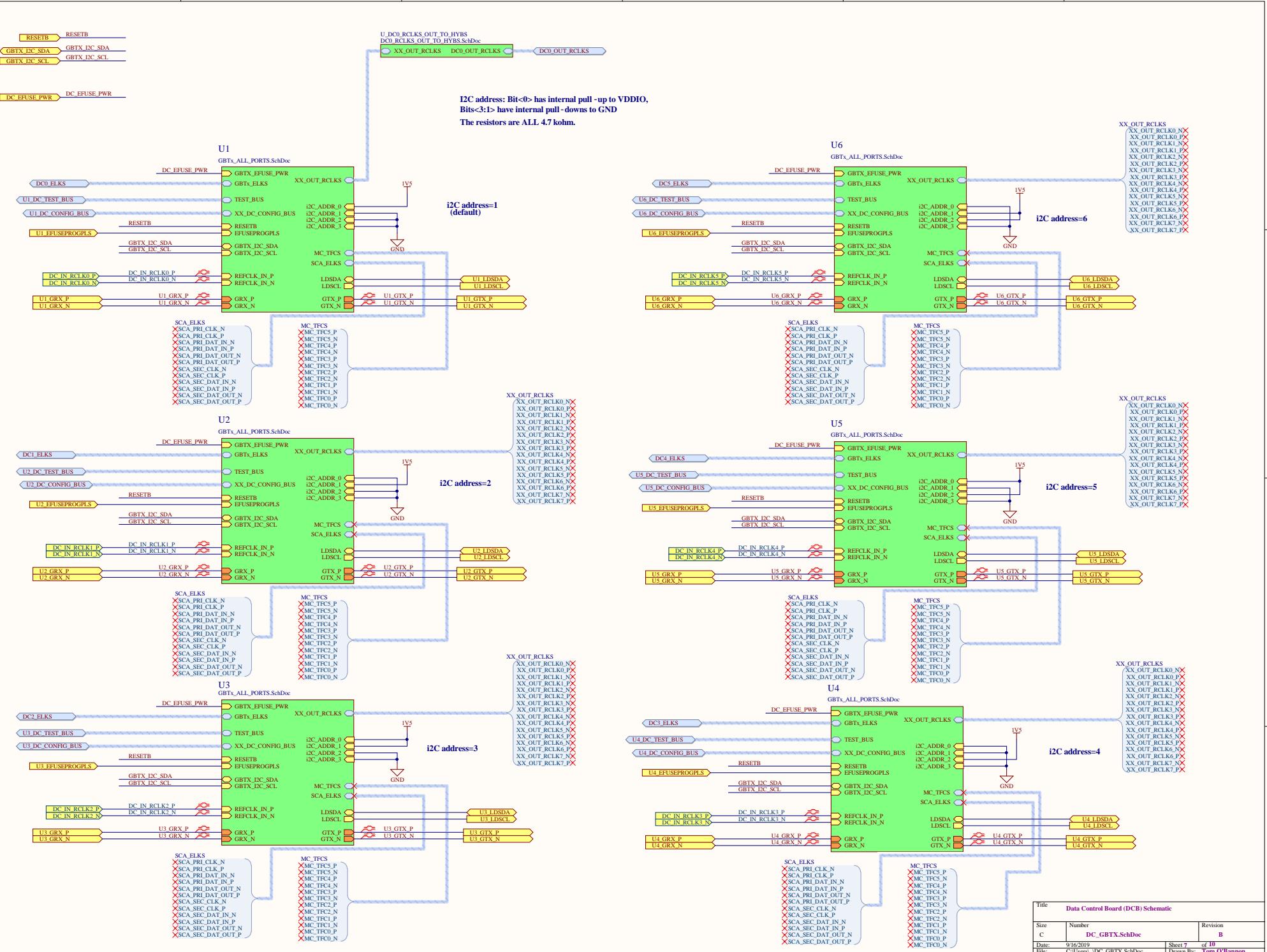
GBTX-MASTER I2C USED ONLY FOR LOCAL CONFIG PROGRAMMING

U_XX_RCLKS_TO_MC_OUT_RCLKS
XX_RCLKS_TO_MC_OUT_RCLKS.SchDoc
XX_OUT_RCLKS MC_OUT_RCLKS
MC_OUT_RCLKS MC_OUT_RCLKS

i2c address=7
GND



Title Data Control Board (DCB) Schematic		
Size	Number	Revision
C	MC + TFC + ECS - Top Level	B
Date: 9/16/2019	Sheet 1 of 10	Drawn By: Tom O'Bannon



Title Data Control Board (DCB) Schematic		
Size	Number	Revision
C	D_GBTx.SchDoc	B
Date: 9/16/2019	Sheet 7 of 10	Drawn By: Tom O'Bannon
File: C:\Users\DC\GBTx.SchDoc		

1 2 3 4 5 6

A

A

B

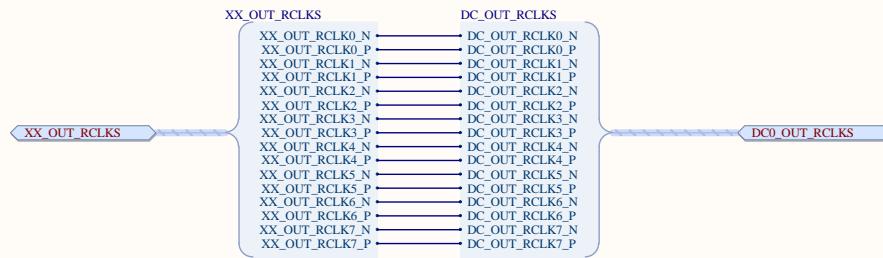
B

C

C

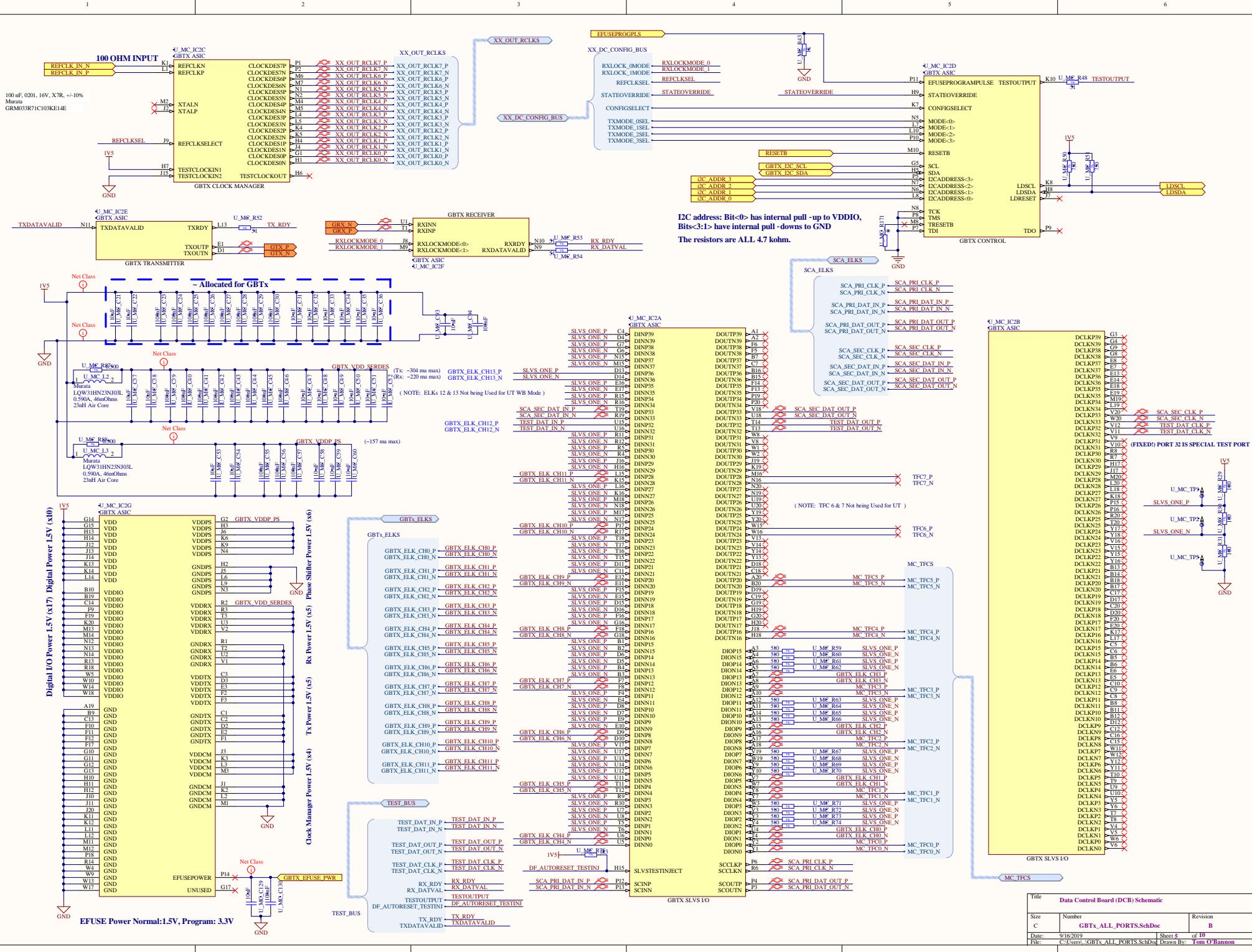
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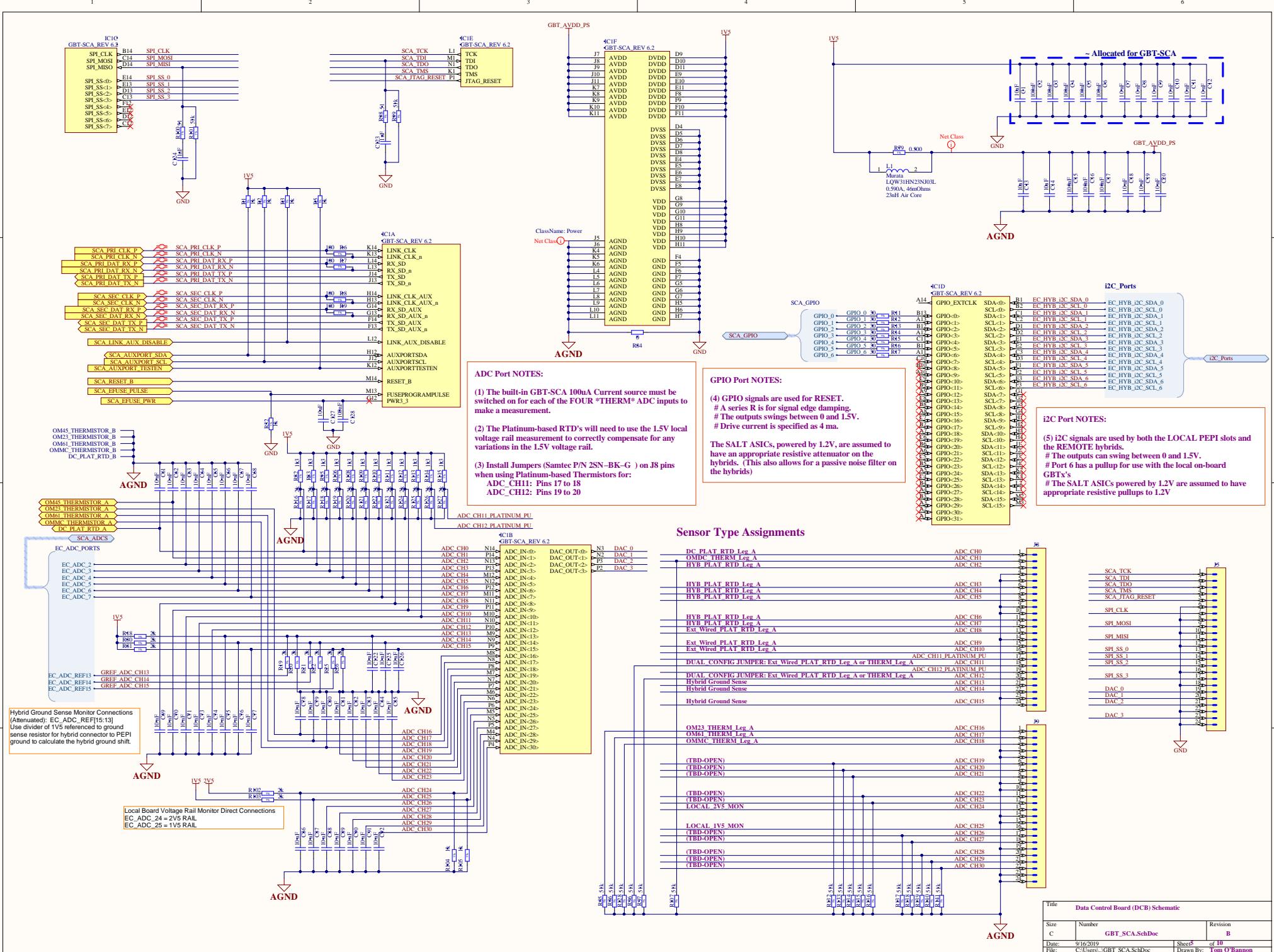
D

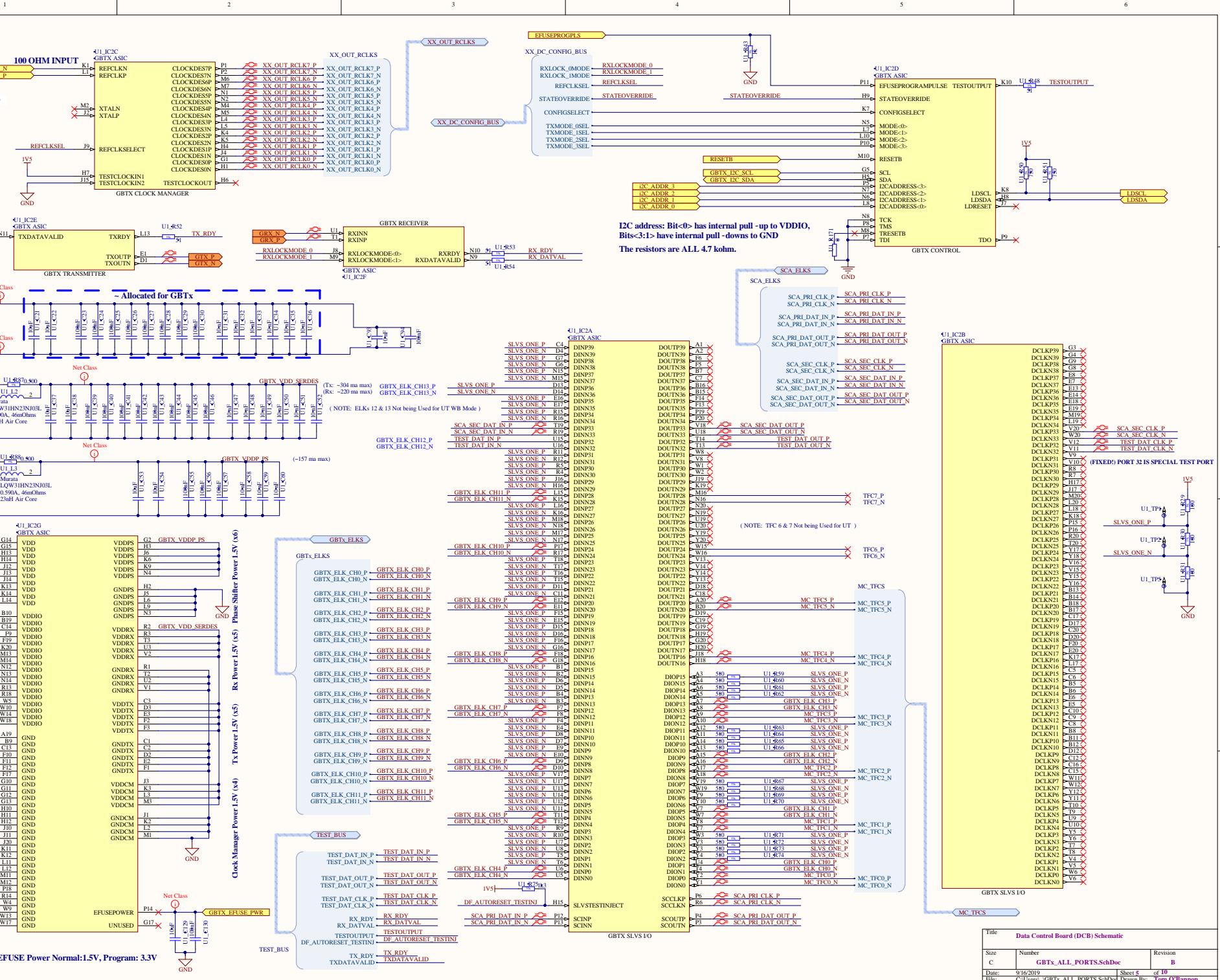


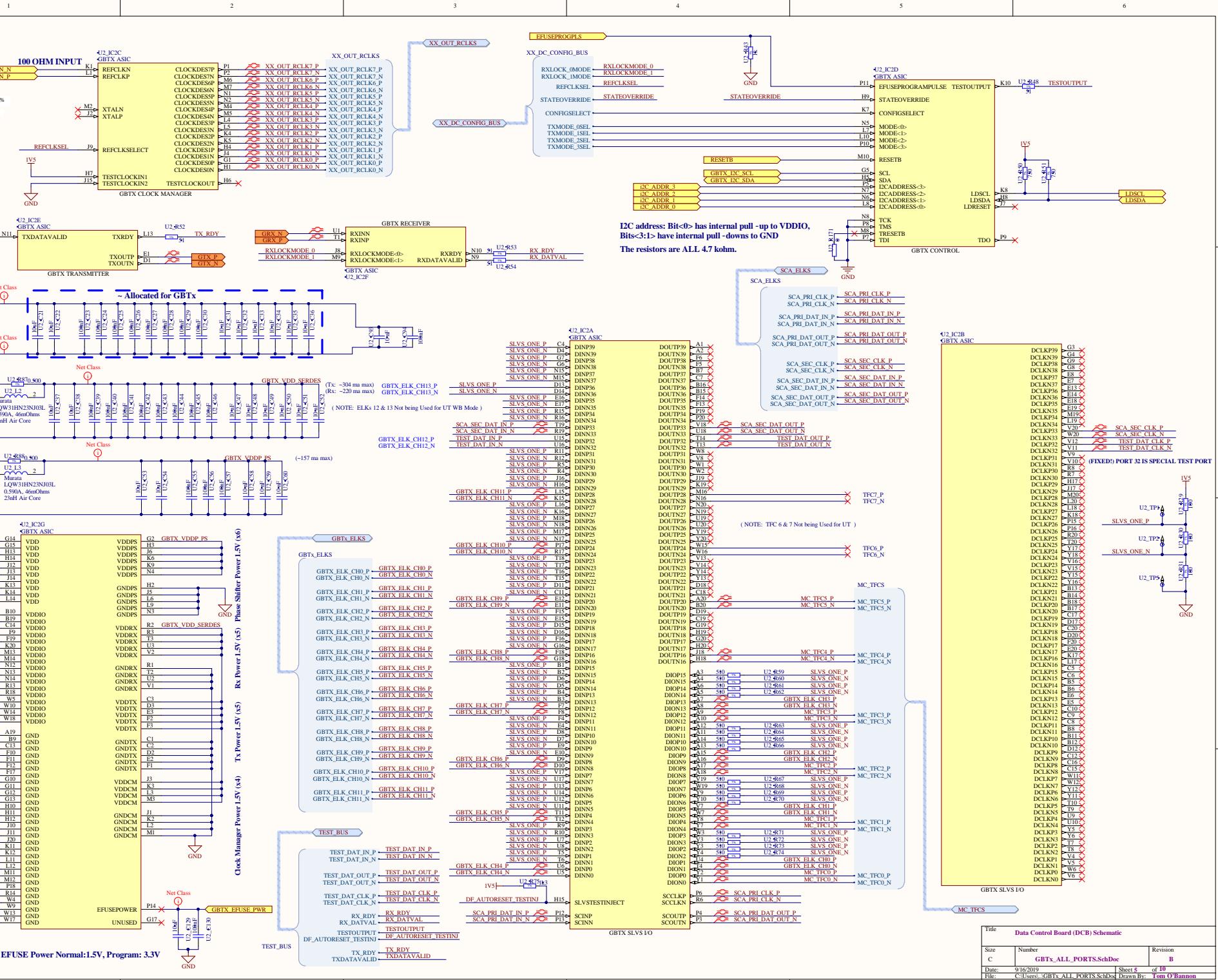
Title Data Control Board (DCB) Schematic		
Size B	Number DC0_RCLKS_OUT_TO_HYBS.SchDoc	Revision B
Date: 9/16/2019	Sheet 8	d0
File: C:\Users\Tom O'Bannon		

1 2 3 4 5 6

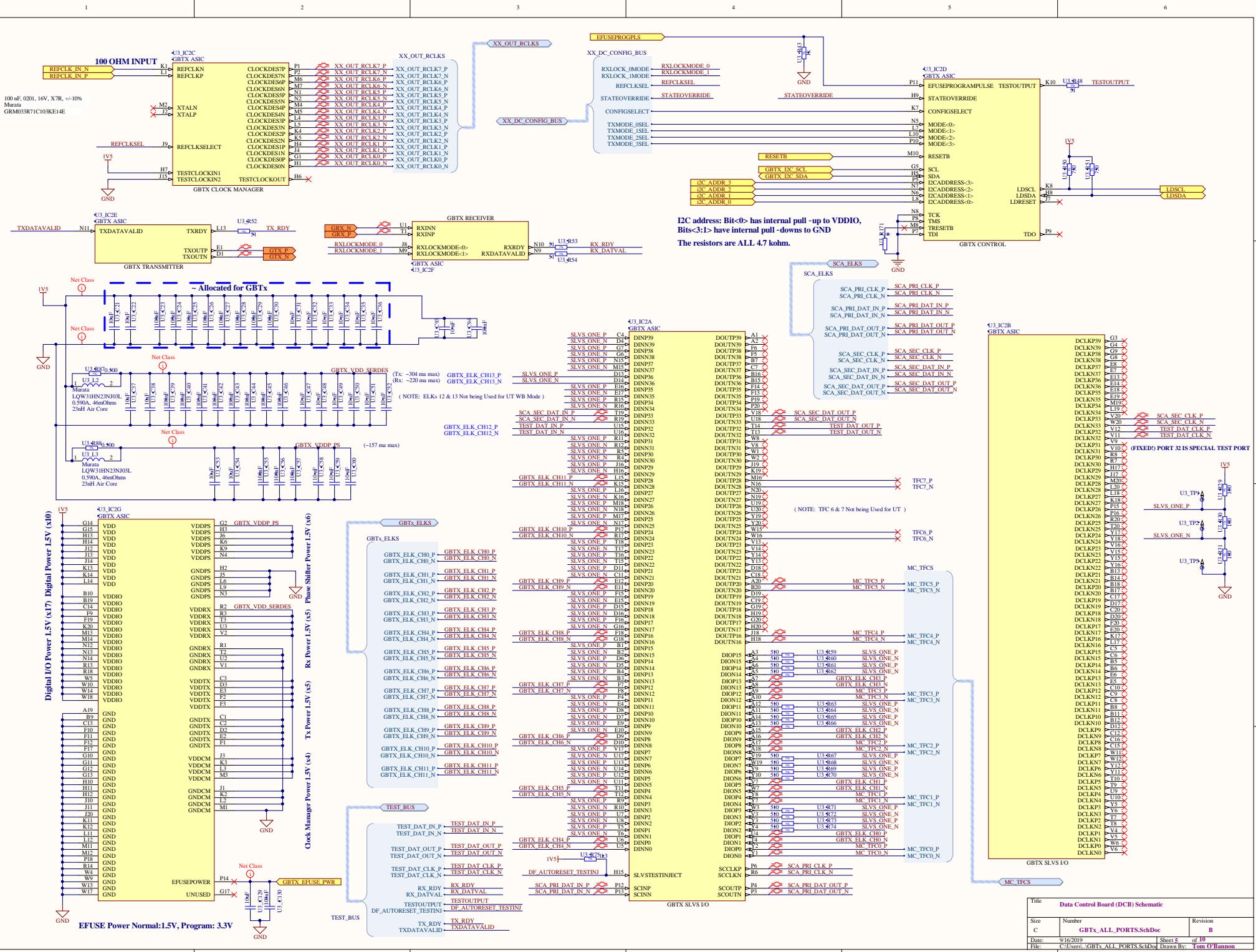




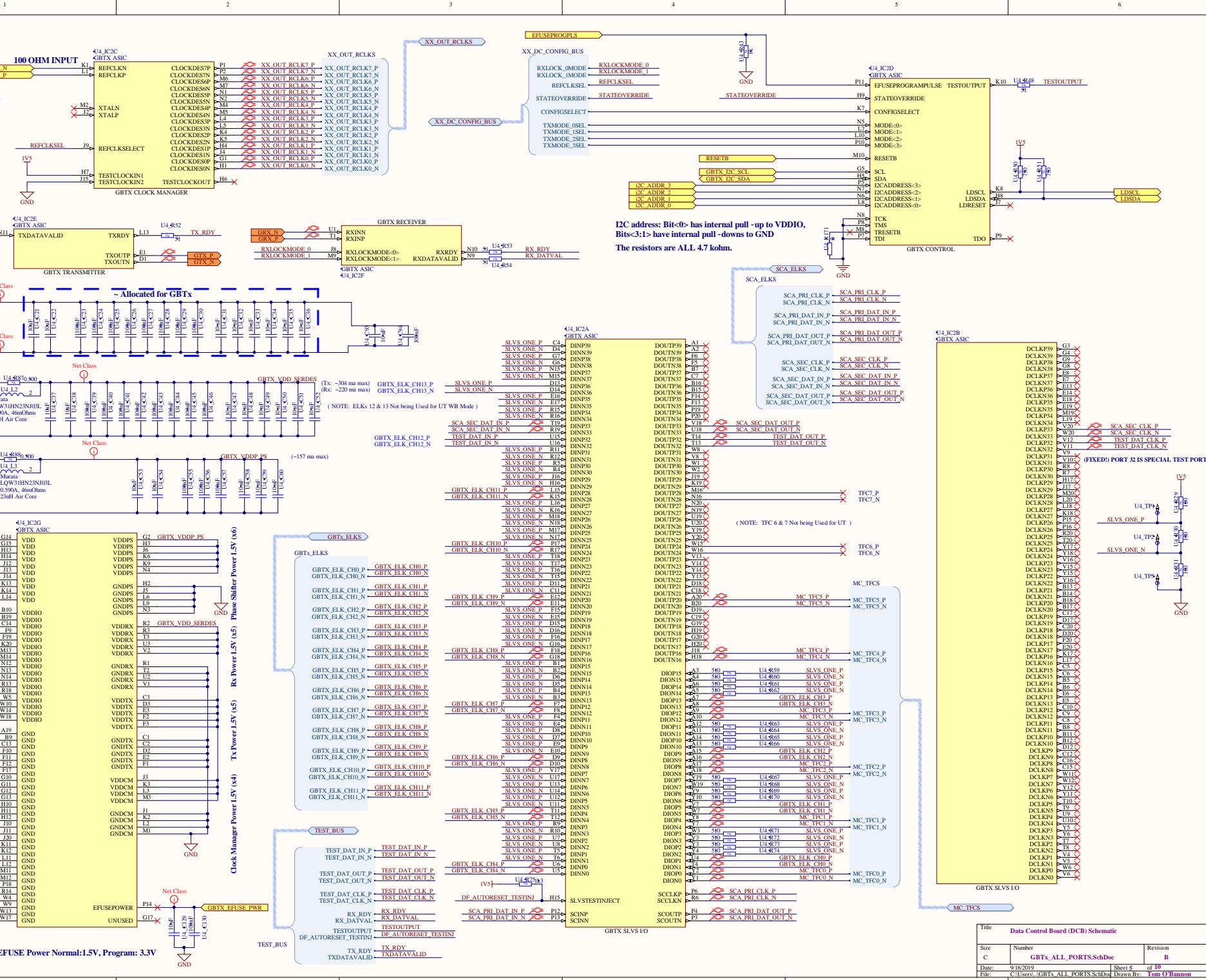




Title: Data Control Board (DCB) Schematic		
Size	Number	Revision
C	GBTx_ALL_PORTS.SchDoc	B
Date: 9/16/2019	Sheet 5 of 10	
File: C:\Users\JGBTx_ALL_PORTS.SchDoc	Drawn By: Tom O'Bannon	

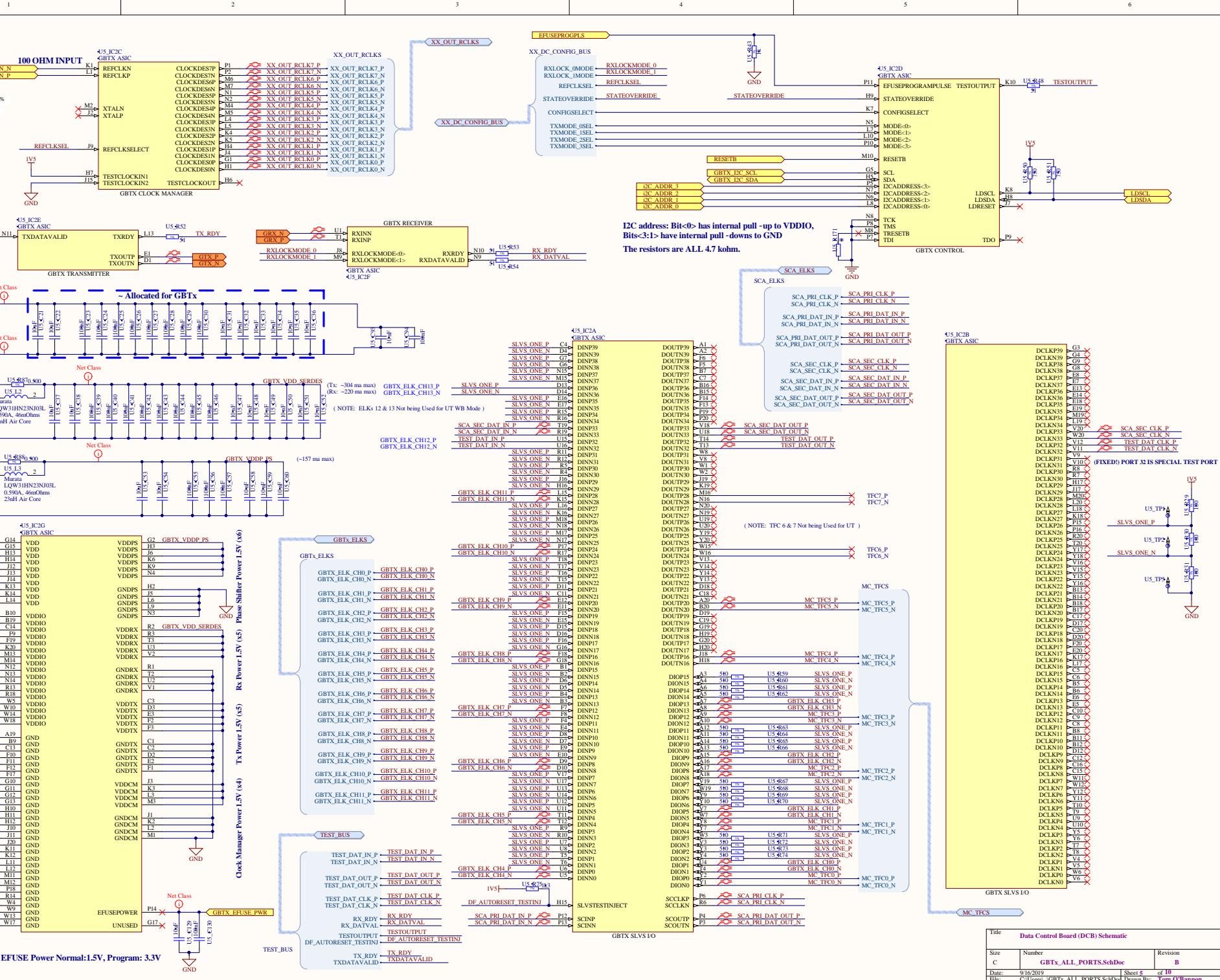


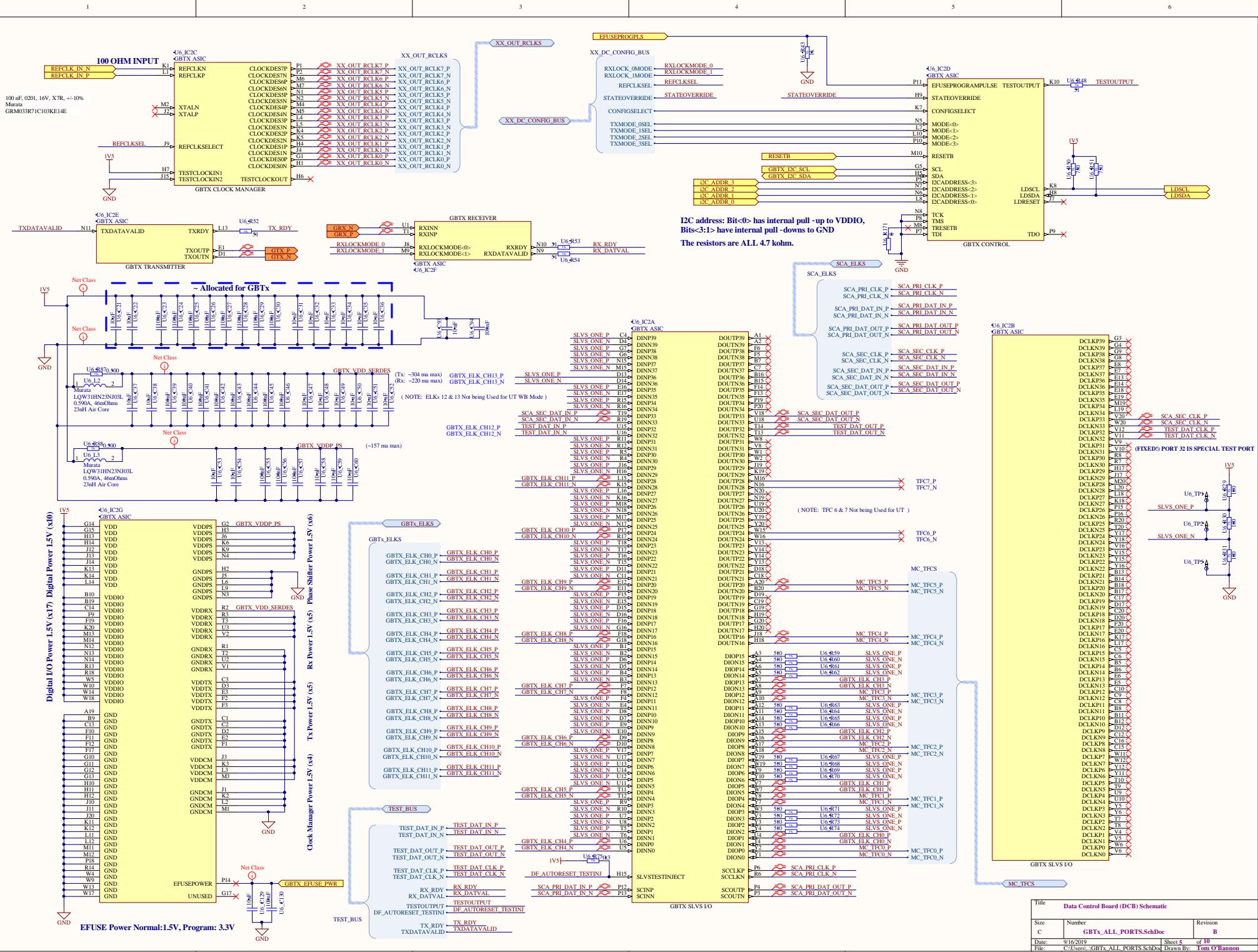
Title Data Control Board (DCB) Schematic
Size C **Number** GBTx_ALL_PORTS.SchDoc **Revision** B
Date 9/16/2019 **Sheet 5 of 10**
File C:\Users\Tom O'Bannon\GBTx_ALL_PORTS.SchDoc **Drawn By** Tom O'Bannon

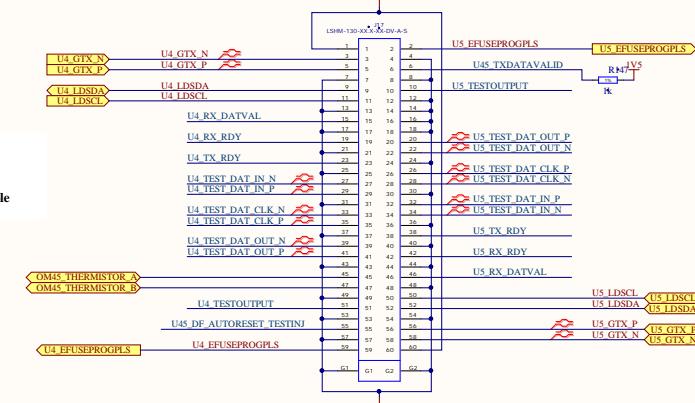
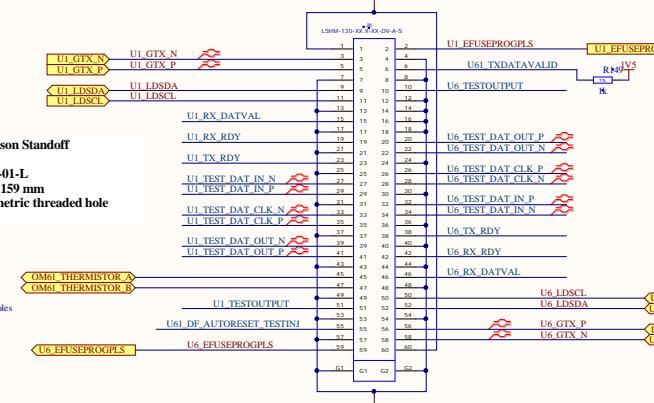
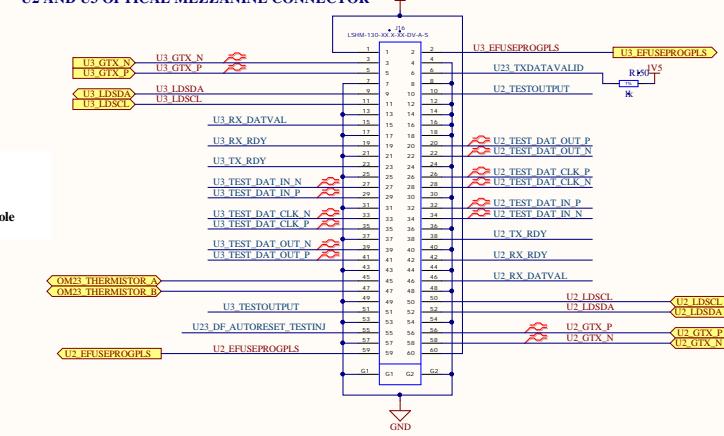
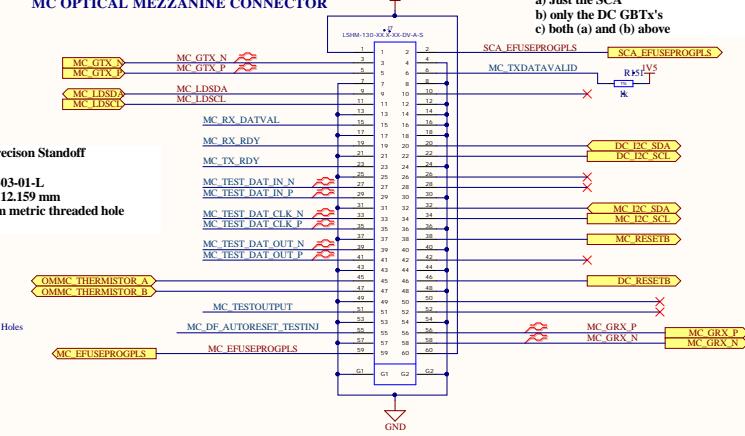


Title Data Control Board (DCB) Schematic

Size	Number	Revision
C	GBTx_ALL_PORTS.SchDoc	B
Date: 9/16/2019	Sheet 5 of 10	
File: C:\Users\...\GBTx_ALL_PORTS.SchDoc	Drawn By: Tom O'Banion	





U4 AND U5 OPTICAL MEZZANINE CONNECTOR 2V5**U1 AND U6 OPTICAL MEZZANINE CONNECTOR 2V5****U2 AND U3 OPTICAL MEZZANINE CONNECTOR 2V5****MC OPTICAL MEZZANINE CONNECTOR**

Title Data Control Board (DCB) Schematic

Size	Number	Revision
C	Opt_IO_Conns.SchDoc	B
Date:	9/16/2019	Sheet 10 of 10
File:	C:\Users\Opt IO Conn SchDoc	Drawn By: Tom O'Bannon

A

A

B

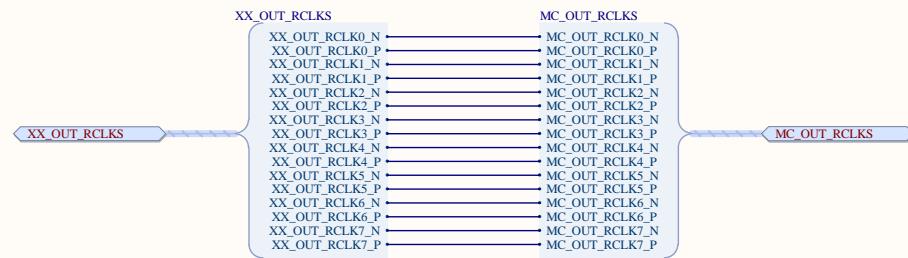
B

C

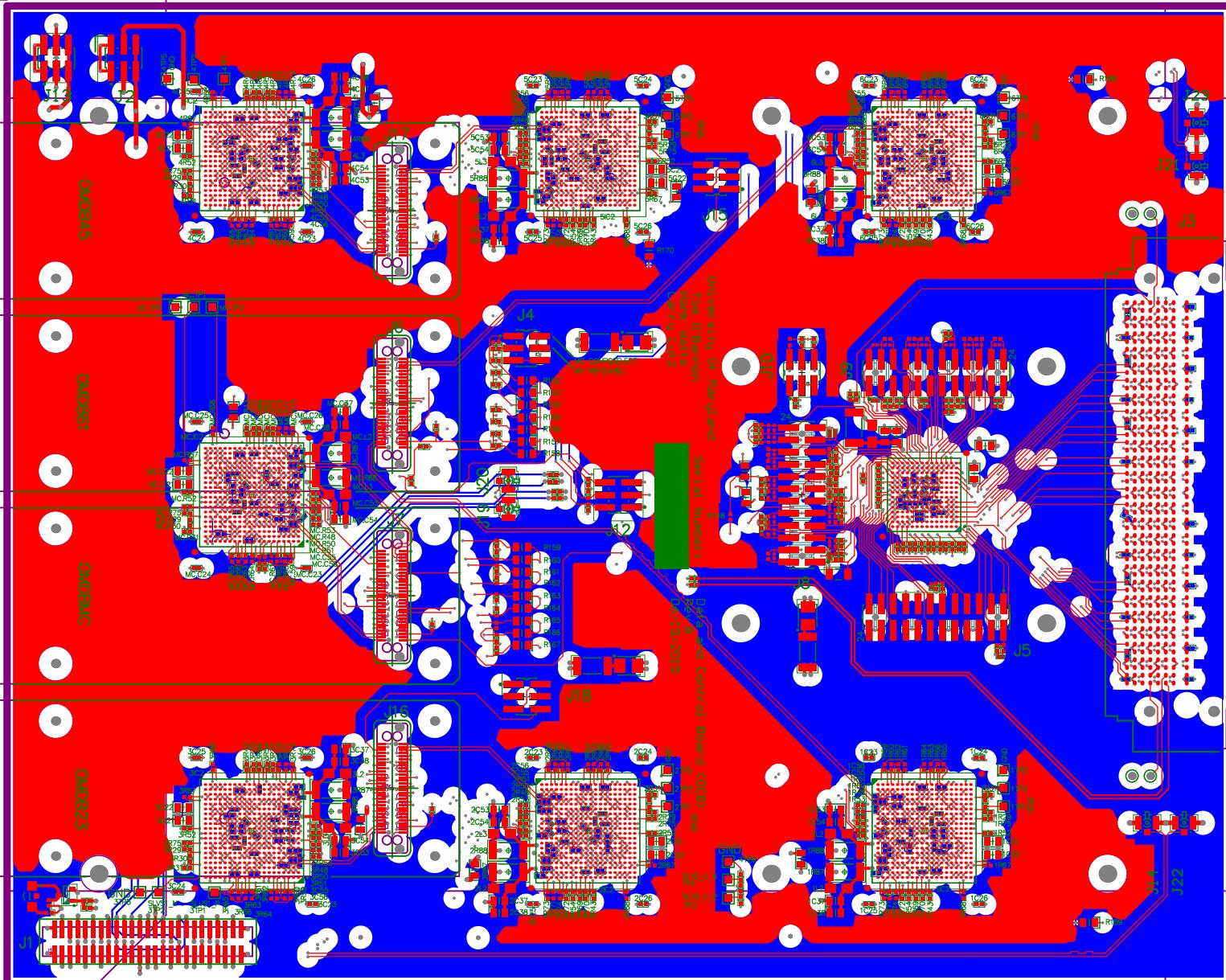
C

D

D



Title		
Size	Number	Revision
B	XX_RCLKS_TO_MC_OUT_RCLKS.SchDoc	B
Date:	9/16/2019	Sheet 6 of 10
File:	C:\Users\XX_RCLKS_TO_MC_OUT_RCLKS.SchDoc	Tom O'Bannon



RECALL: NEED to keep these regions as free as possible of components to allow for a thermal gap pad from Optical Modules.