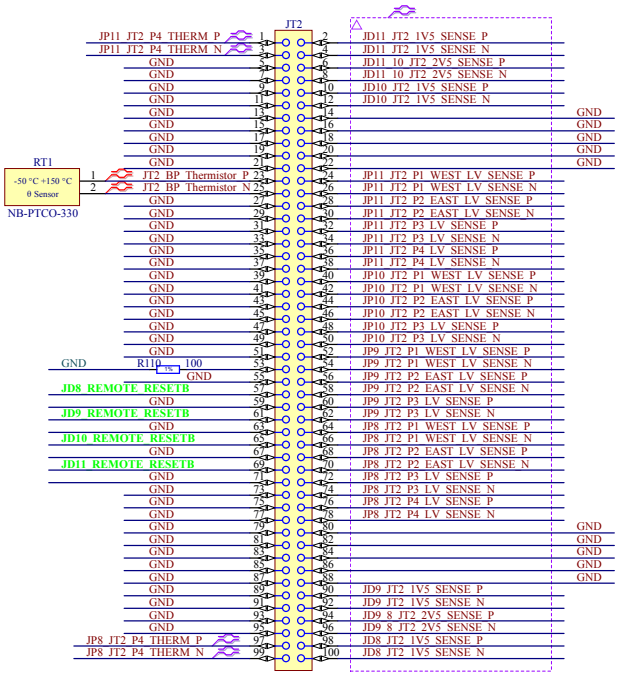
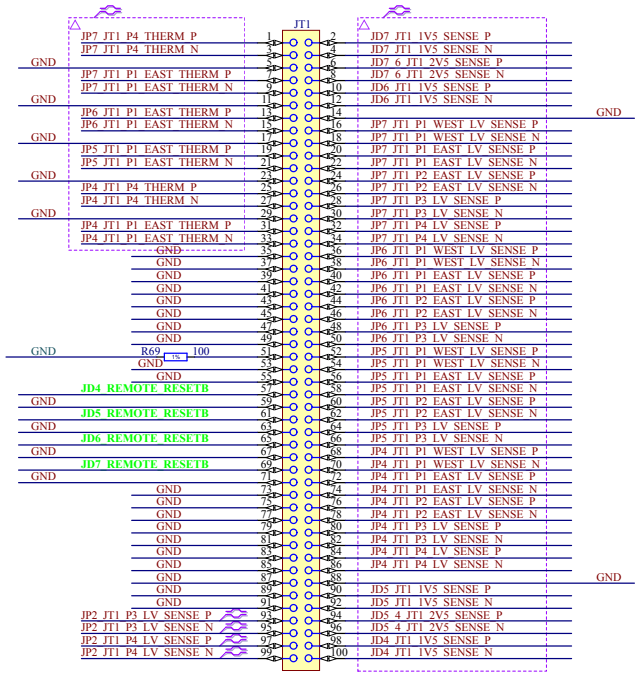
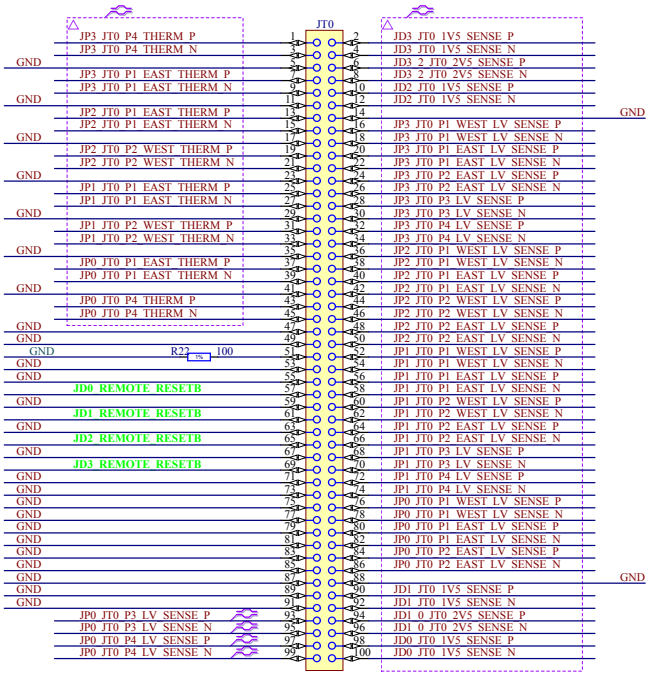






NOTE: The GND connected via the seies 100 Ohm can be used as a remote ground signal reference where needed.

JDx_y_NODE_2V5_SENSE_z is the location where the sense line pair is to be connected to the plane between the two DCB slots sharing this 2V5 rail.
WHERE:
z='P' goes to the 2V5 rail
z='N' goes to the ground plane

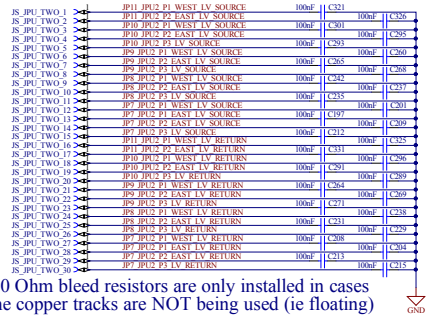
IMPORTANT NOTE: The "GND" pins MUST NOT EVER be connected to any remote ground nodes.

Project/Equipment	PEPI		
Document	*PEPI Backplane True Telemetry IO UpperConns*	Designer M. Franco Sevilla	
TE/MPE		Drawn by M. Franco Sevilla	18/12/2018
		Check by B. Civel	22/02/2019
		Last Mod. B. Civel	5/6/2019
		File Telemetry_IO_UpperConns.SchDoc	
		Print Date 6/20/2019 6:55:55 AM	Sheet 2 of 21
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-03992-V1-0	Size A3	Rev -

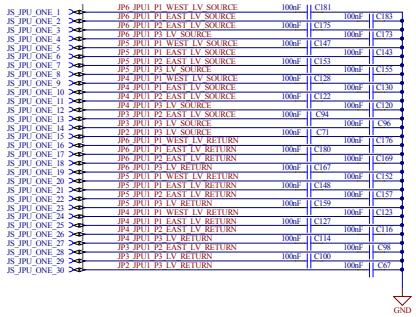
UPPER Power Conns--(All dedicated to pigtail power routes)
JPUx connectors located directly on the Pigtail Power Breakout Board

NOTE: ALL 3 of these contact / pigtail assignment grouping needed to be identical so one PCB design can be used in 3 places on the rear of the backplane

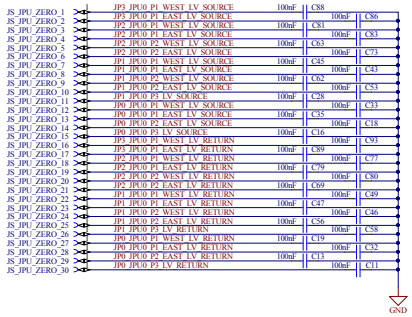
Fed by JPU2 on the Pigtail Power Breakout Brd



Fed by JPU1 on the Pigtail Power Breakout Brd



Fed by JPU0 on the Pigtail Power Breakout Brd

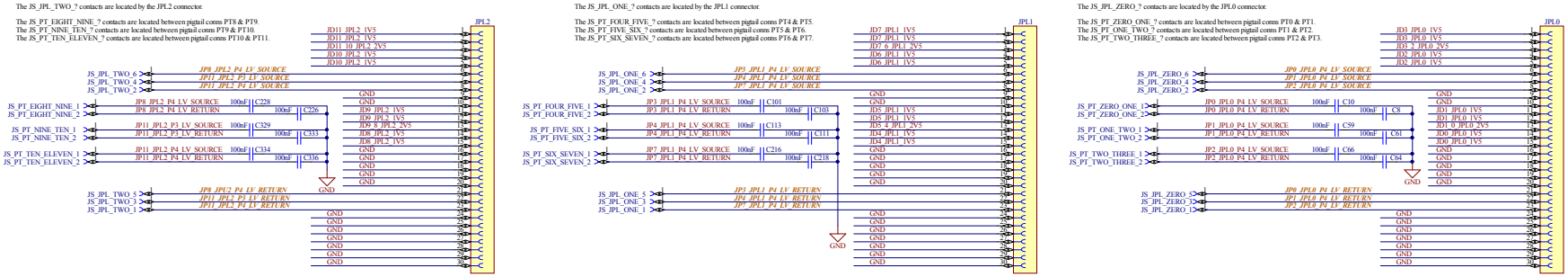


NOTE: These 100 Ohm bleed resistors are only installed in cases where the copper tracks are NOT being used (ie floating)

EACH Power Group receives SOURCE power from a single Maraton Channel.

The Maraton Channel is indirectly connected to system power ground via the ground sense resistor connections (ie one per 4-ASICs)

LOWER Power Conns--(All DCB slot power routes and a few pigtal power routes)



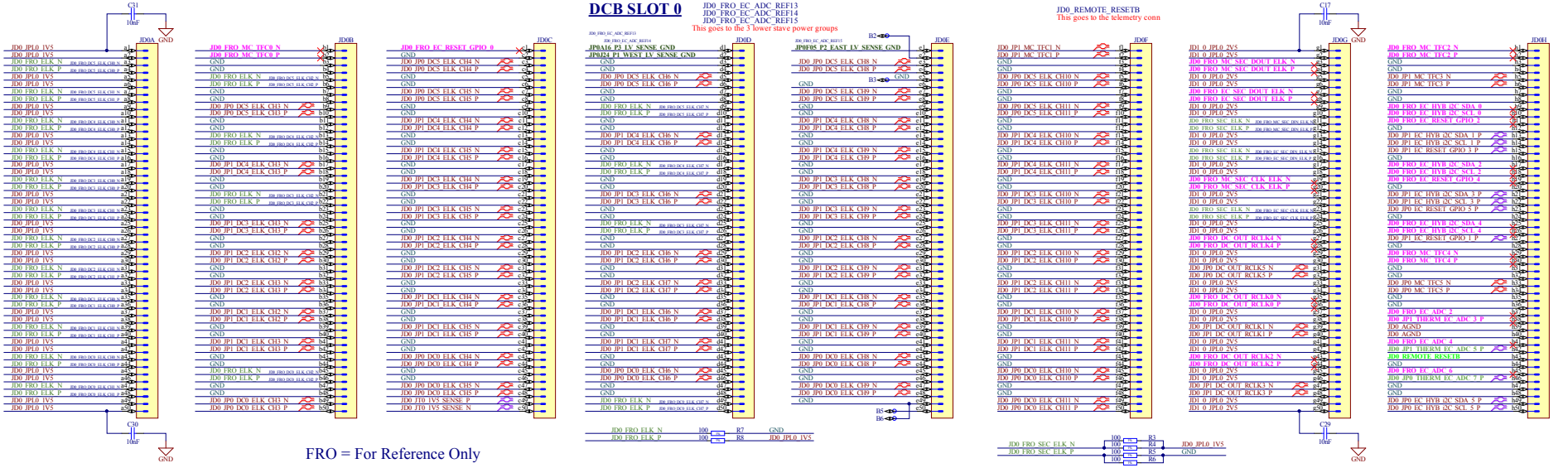
NOTE: (1) The pigtail power lines on JPL2, JPL1, and JPL0 get routed via the individual JS contacts to the PIGTAIL_POWER_Breakout_PCB.

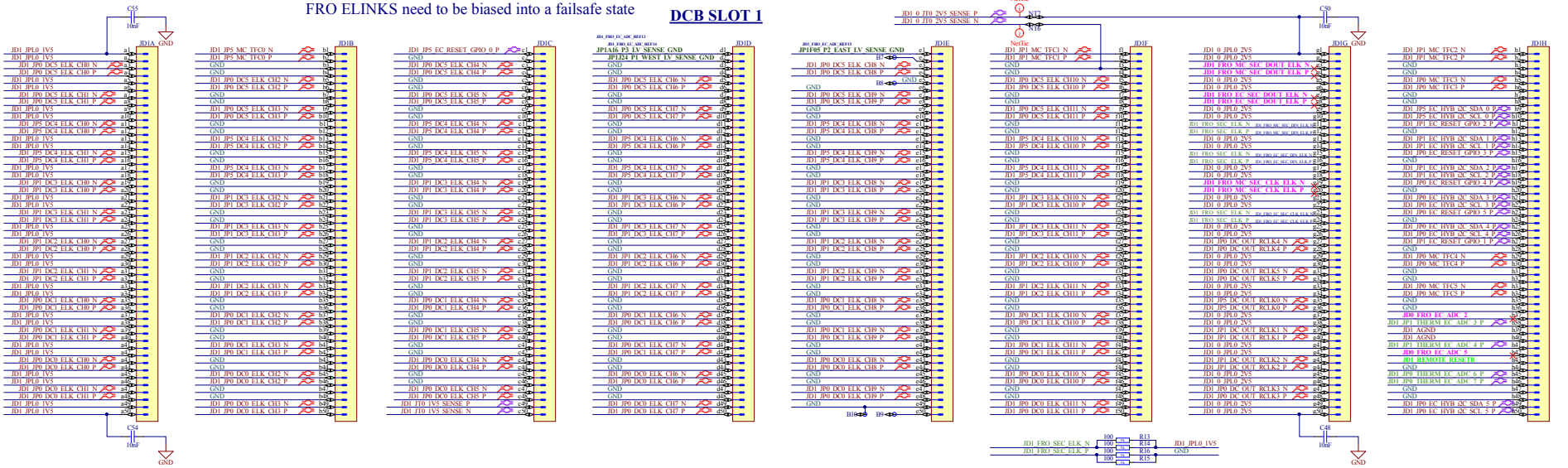
(2) Each DCB slot uses 1 master + 1 slave channel. Both connector pins are labeled '_1V5. Therefore, one is for the Master cable and the second is for the slave cable.

(3) The power group 'returns' being joined together also prevents any unused pigtial and Stave flex cable tracks from being left floating.

(4) The power group 'Source' lines in depopulated 'beta' and 'gamma' BP positions are connected via resistors with designtors R_B? and R_G?, respectively, to the associated power group returns to avoid being left floating.

Project/Equipment	PEPI		
Document	PEPI Backplane True - Power Bank Conns -	Designer M. Franco Sevilla	
		Drawn by M. Franco Sevilla	18/12/2018
		Check by B. Civel	22/02/2019
		Last Mod. B. Civel	5/6/2019
		File: Power_Bank_Conns.SchDoc	
		Print Date 6/20/2019 6:55:55 AM	Sheet 3 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-03992-V1-0	A2 Rev -

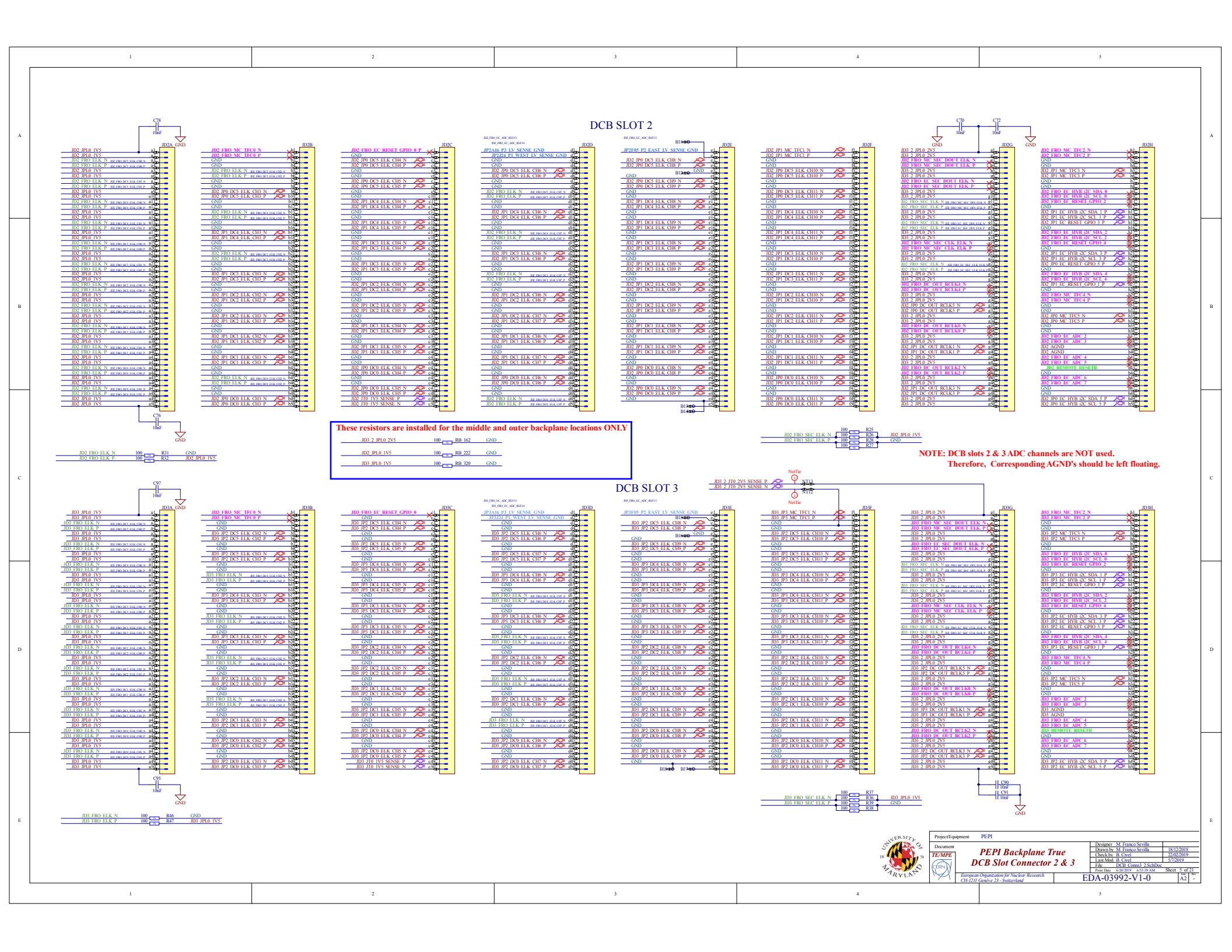


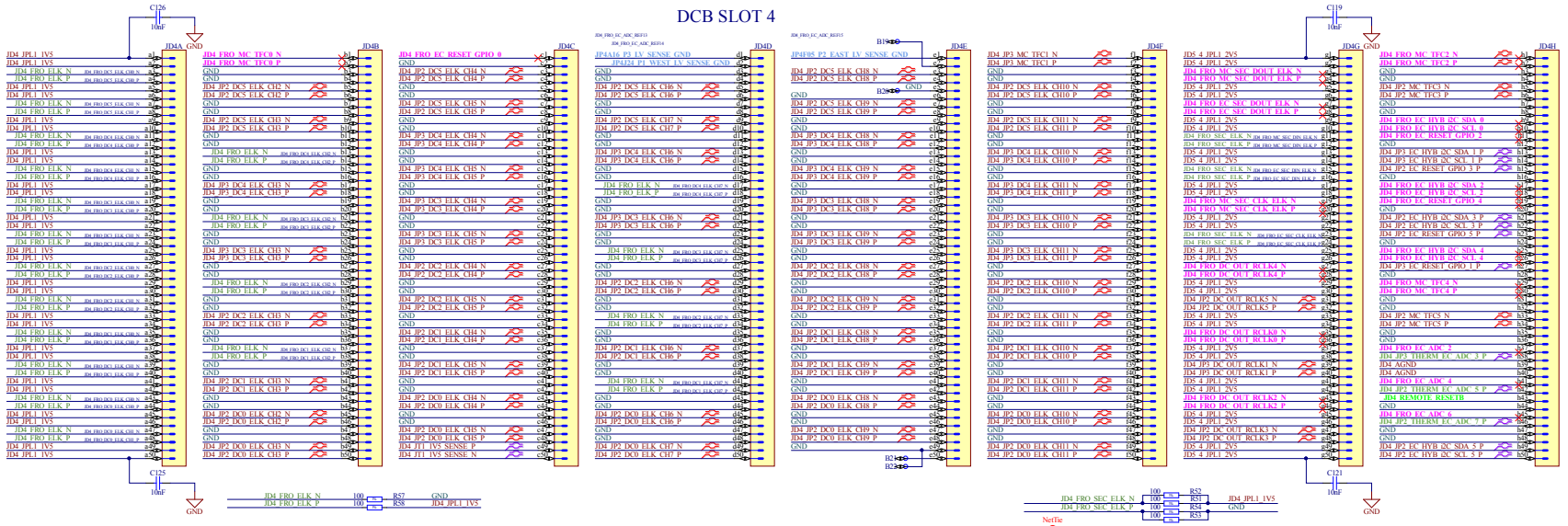


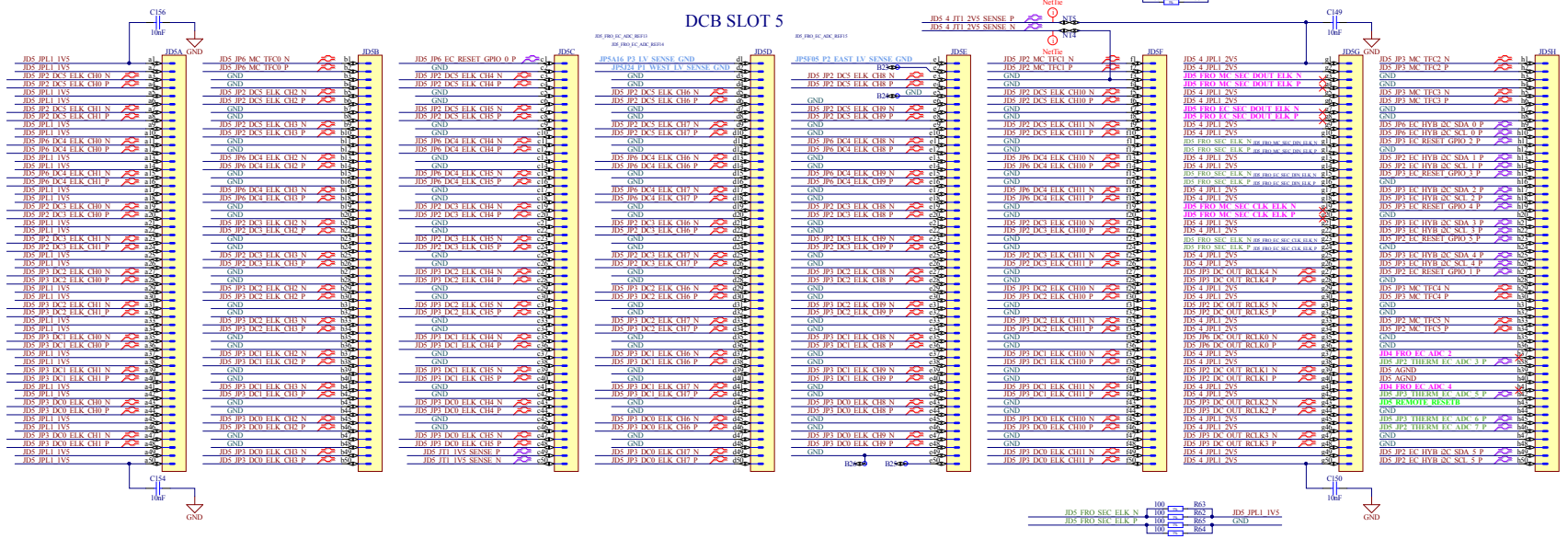
Project/Equipment	PEPI
Document	PEPI Backplane True DCB Slot Connector 0 & 1
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla — 18/12/2018
Check by	B. Cwel — 22/02/2019
Last Mod.	B. Cwel — 5/7/2019
File	DCB_Conn1_0.SchDoc
Print Date	6/20/2019 6:55:57 AM
Sheet	4 of 21
Size	A2
Rev	-

European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland

EDA-03992-V1-0


DCB SLOT 2
These resistors are installed for the middle and outer backplane locations ONLY
JD3_2_JPL0_2V5 100 RB_162 GND
JD2_JPL0_1V5 100 RB_222 GND
JD3_JPL0_1V5 100 RB_320 GND
NOTE: DCB slots 2 & 3 ADC channels are NOT used.
Therefore, Corresponding AGND's should be left floating.
DCB SLOT 3
PEPI
PEPI Backplane True
DCB Slot Connector 2 & 3
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland
EDA-03992-V1-0
Designer M. Franco Sevilla
Drawn by M. Franco Sevilla 18/12/2018
Check.by B. Civel 22/02/2019
Last Mod. B. Civel 5/7/2019
File: DCB_Conn3_2.SchDoc
Print Date 6/20/2019 6:55:59 AM
Sheet 5 of 21
A2

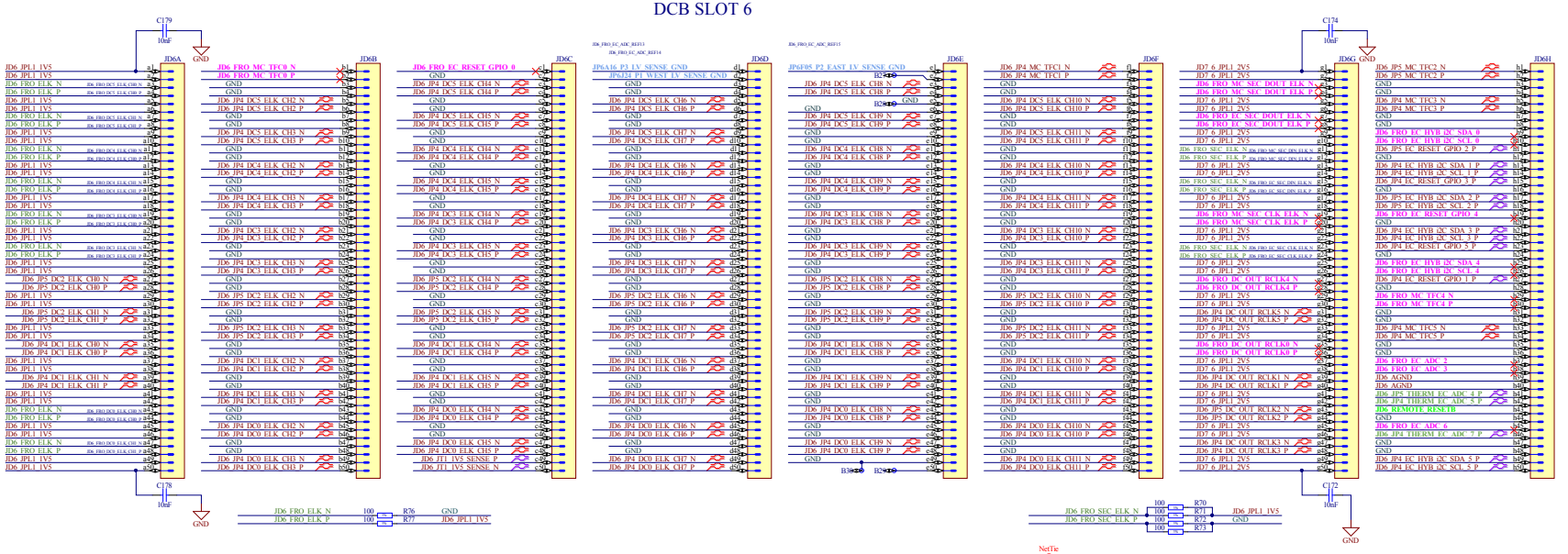




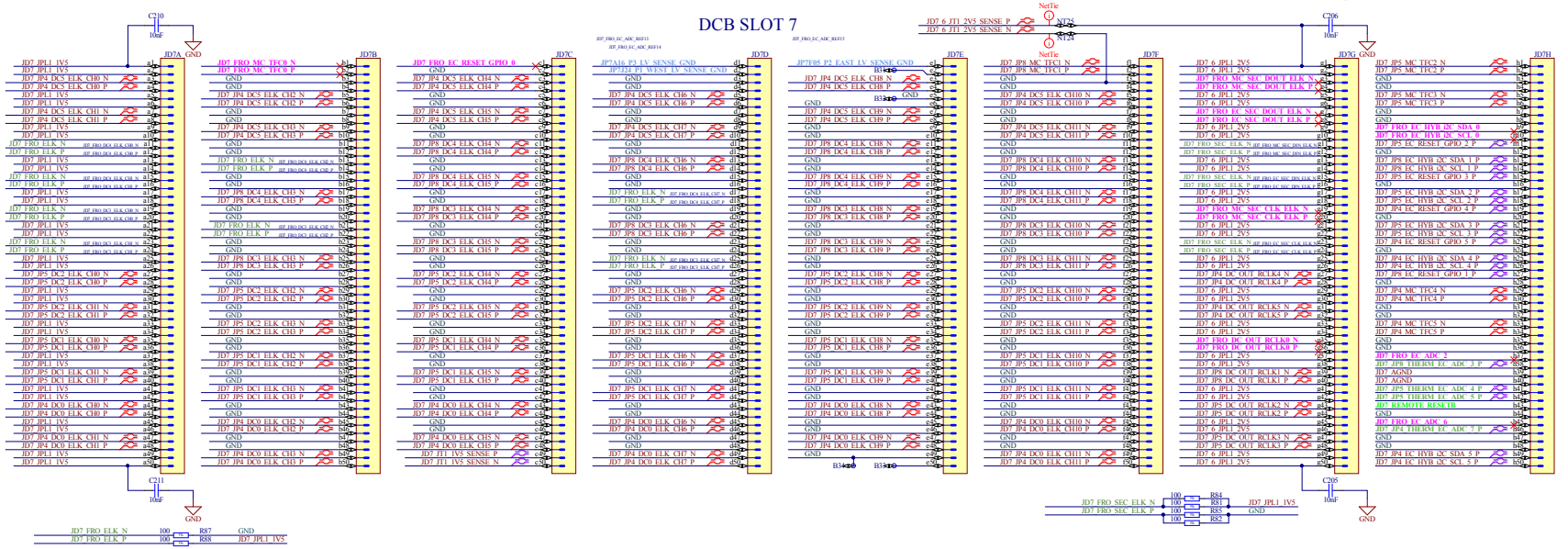
Project/Equipment	PEPI
Document	PEPI Backplane True DCB Slot Connector 4 & 5
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla — 18/12/2018
Check.by	B. Civel — 22/02/2019
Last Mod.	B. Civel — 5/7/2019
File	DCB_Conns5_4.SchDoc
Print Date	6/20/2019 6:56:01 AM — Sheet 6 of 21
	EDA-03992-V1-0 — A2

European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland

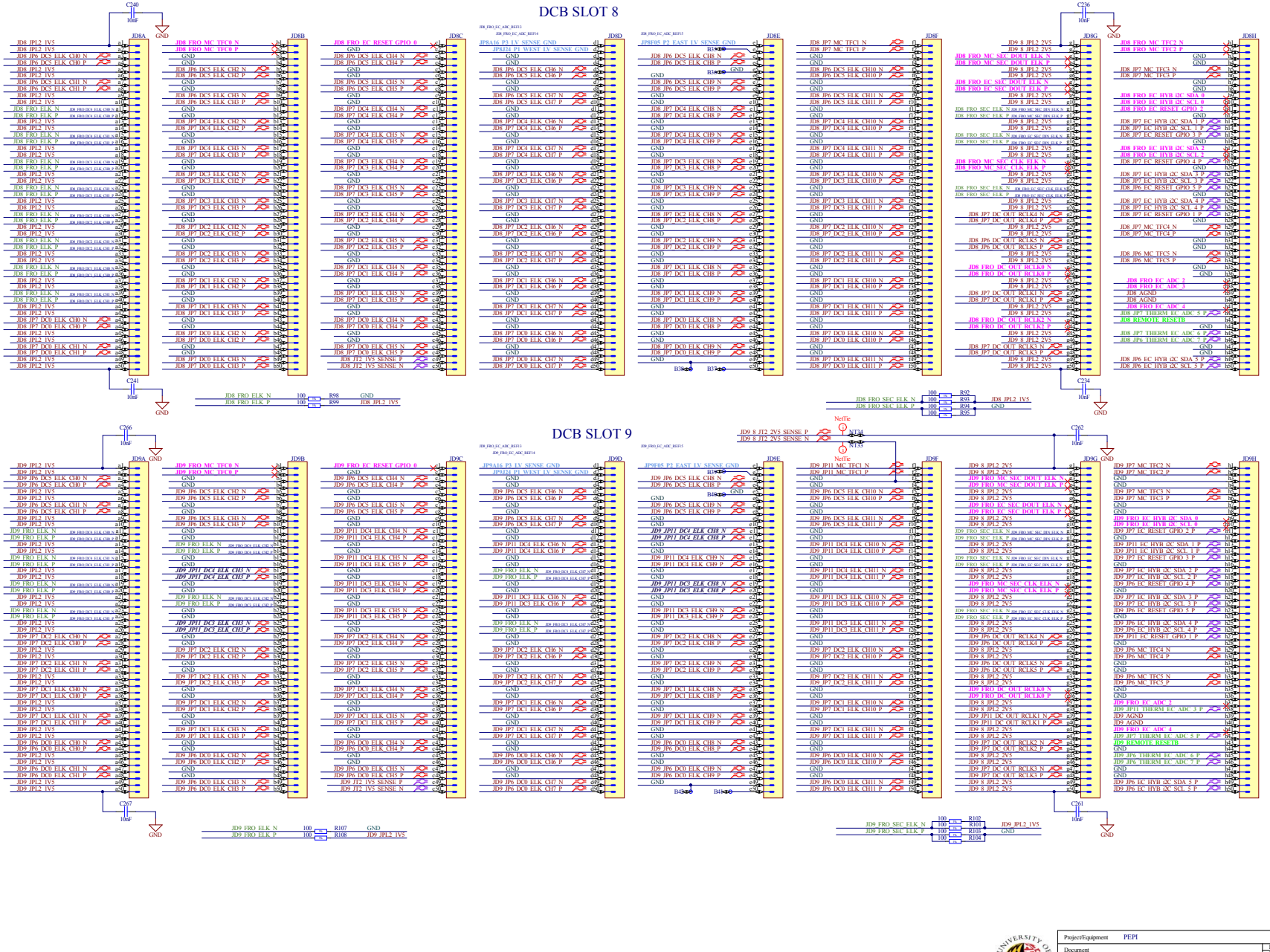
DCB SLOT 6

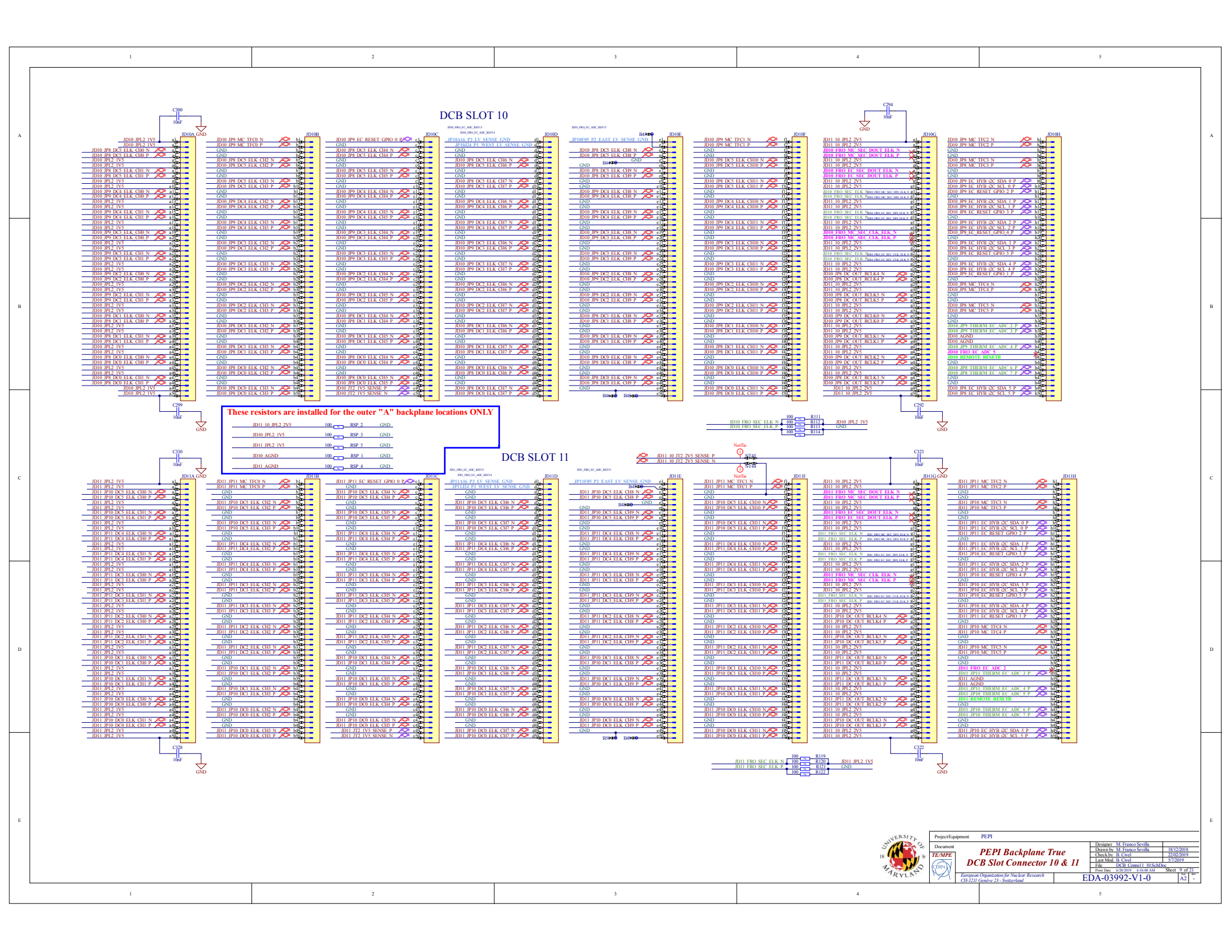


DCB SLOT 7



Project/Equipment	PEPI		
Document	PEPI Backplane True DCB Slot Connector 6 & 7	Designer M. Franco Sevilla	
TE/MPE		Drawn by M. Franco Sevilla	18/12/2018
CERN		Check.by B. Civel	22/02/2019
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Last Mod. B. Civel	5/7/2019
		File: DCB_Conn7_6.SchDoc	
		Print Date: 6/20/2019 6:56:03 AM	Sheet 7 of 21
	EDA-03992-V1-0		Size A2


DCB SLOT 8
DCB SLOT 9
JD8A
JD8B
JD8C
JD8D
JD8E
JD8F
JD8G
JD8H
JD9A
JD9B
JD9C
JD9D
JD9E
JD9F
JD9G
JD9H
C240
C241
C236
C234
C266
C267
C262
C261
10nF
GND
R98
R99
R92
R93
R94
R95
R107
R108
R102
R103
R104
R101
JD8_JPL2_1V5
JD9_JPL2_1V5
JD8_FRO_ELK_N
JD8_FRO_ELK_P
JD8_FRO_SEC_ELK_N
JD8_FRO_SEC_ELK_P
JD9_FRO_ELK_N
JD9_FRO_ELK_P
JD9_FRO_SEC_ELK_N
JD9_FRO_SEC_ELK_P
JD8_JT2_2V5_SENSE_N
JD8_JT2_2V5_SENSE_P
JD9_8_JT2_2V5_SENSE_N
JD9_8_JT2_2V5_SENSE_P
NetTie
XT334
XT133
JPHA16_P3_LV_SENSE_GND
JPH8224_P1_WEST_LV_SENSE_GND
JPH8316_P3_LV_SENSE_GND
JPH8316_P1_WEST_LV_SENSE_GND
JPH8105_P2_EAST_LV_SENSE_GND
JPH8105_P2_EAST_LV_SENSE_GND
JD8_FRO_EC_ADC_H1F13
JD8_FRO_EC_ADC_H1F14
JD8_FRO_EC_ADC_H1F15
JD9_FRO_EC_ADC_H1F13
JD9_FRO_EC_ADC_H1F14
JD9_FRO_EC_ADC_H1F15
Project/Equipment
PEPI
Document
PEPI Backplane True
DCB Slot Connector 8 & 9
TE/MPE
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland
Designer M. Franco Sevilla
Drawn by M. Franco Sevilla
Check by B. Civel
Last Mod. B. Civel
File DCB_Conn9_8.SchDoc
Print Date 6/20/2019 6:50:06 AM
18/12/2018
22/02/2019
5/7/2019
Sheet 8 of 21
EDA-03992-V1-0
A2


DCB SLOT 10
DCB SLOT 11
These resistors are installed for the outer "A" backplane locations ONLY
JD11_10_JPL2_2V5 100 RSP_2 GND
JD10_JPL2_1V5 100 RSP_3 GND
JD11_JPL2_1V5 100 RSP_5 GND
JD10_AGND 100 RSP_1 GND
JD11_AGND 100 RSP_4 GND
JD10A GND
JD10B
JD10C
JD10D
JD10E
JD10F
JD10G
JD10H
JD11A GND
JD11B
JD11C
JD11D
JD11E
JD11F
JD11G GND
JD11H
C299 10nF
C200 10nF
C292 10nF
C294 10nF
C328 10nF
C330 10nF
C322 10nF
C323 10nF
R111 100
R112 100
R113 100
R114 100
R119 100
R120 100
R121 100
R123 100
NetTie
NT45
NT44
Project/Equipment PEPI
Document TE/MPE
PEPI Backplane True DCB Slot Connector 10 & 11
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland
EDA-03992-V1-0
Designer M. Franco Sevilla
Drawn by M. Franco Sevilla 18/12/2018
Check.by B. Civel 22/02/2019
Last Mod. B. Civel 5/7/2019
File: DCB_Comm11_10.SchDoc
Print Date 6/20/2019 6:56:08 AM
Sheet 9 of 21
Size A2
Rev -

NOTES:

FP? are placeholders for floating copper. These could be pressed against a carbon-impregnated foam to bleed charge, if needed.

Bright_Blue = AC signal reference ground return

Dark Green = Floating DC Hybrid reference ground return

Light Green =Thermistors

Fuscia = Telemetry Thermistors for connections External to PEPI

These italics signals are not used in the middle and outer backplane locations

GENERAL GROUND RETURN RULES APPLIED

1) Each floating hybrid ground ground is connected directly to the corresponding source regulator return path.
a.) But DC levels relative to the main backplane ground are maintained via ground sense Resistor connected to the main backplane ground. This also has a small parallel EMI cap to shunt high frequency noise.

2) Every single-ended signal from each hybrid has a dedicated ground reference return that is connected to the main backplane ground via a small EMI cap to allow for a high frequency return path only.

3) Analog ground for the PT1000 sensors is intentionally separate from the main backplane ground.

For REF: PigtailV3_Straight_Long

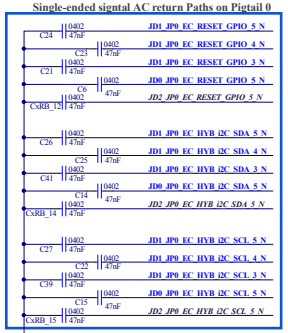
Pigtail 0

GENERAL COMMENTS:

EC_ADC_REF<15..13> ADC channels can be used to sample the hybrid ground sense.

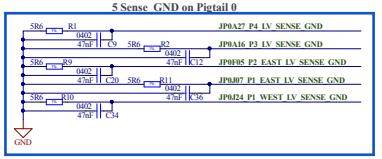
DCB slots 2,3, 10, and 11 can be depopulated for middle and outer backplanes. Therefore, the corresponding ED_ADC channels should be avoided for ground sense and backplane thermistor measurement inputs to ensure the intended measurement connections are available in each of the backplane locations once populated per elink map requirements.

Single-ended signtal AC return Paths on Pigtail 0



Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

5 Sense GND on Pigtail 0



NOTE: P4 THERMISTOR and P1 EAST_THERMISTOR are routed to the telemetry signal connector

JD1_AGND — JD1_JP0_THERM_EC_ADC_7_N

JD1_AGND — JD1_JP0_THERM_EC_ADC_6_N

JD0_AGND — JD0_JP0_THERM_EC_ADC_7_N

List of Hybrid Power circuits that are not used in middle and outer backplanes (Therefore, the pigtail power breakout boards need to handle these cases)

JP0_JPU0_P1_EAST_LV_SOURCE
JP0_JPU0_P1_EAST_LV_RETURN

These resistors are installed for the middle and outer backplane locations ONLY

Project/Equipment	PEPI
Document	PEPI Backplane True - Pigtail Conn 0 -
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla — 18/12/2018
Checked by	B. Civel — 22/02/2019
Last Mod.	B. Civel — 5/6/2019
File	Pigtail_Conns_0.SchDoc
Print Date	6/20/2019 8:56:10 AM — Sheet 10 of 21
Size	A2
Rev	-

European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland

EDA-03992-V1-0

NOTES:

FP? are placeholders for floating copper. These could be pressed against a carbon-impregnated foam to bleed charge, if needed.

Bright_Blue = AC signal reference ground return

Dark Green = Floating DC Hybrid reference ground return

Light Green =Thermistors

These italics signals are not used in the middle and outer backplane locations

GENERAL GROUND RETURN RULES APPLIED

1) Each floating hybrid ground ground is connected directly to the corresponding source regulator return path.
a.) Ban DC levels relative to the main backplane ground are maintained via ground sense Resistor connected to the main backplane ground. This also has a small parallel EMI cap to shunt high frequency noise.

2) Every single-ended signal from each hybrid has a dedicated ground reference return that is connected to the main backplane ground via a small EMI cap to allow for a high frequency return path only.

3) Analog ground for the PT1000 sensors is intentionally separate from the main backplane ground.

P2_EAST_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

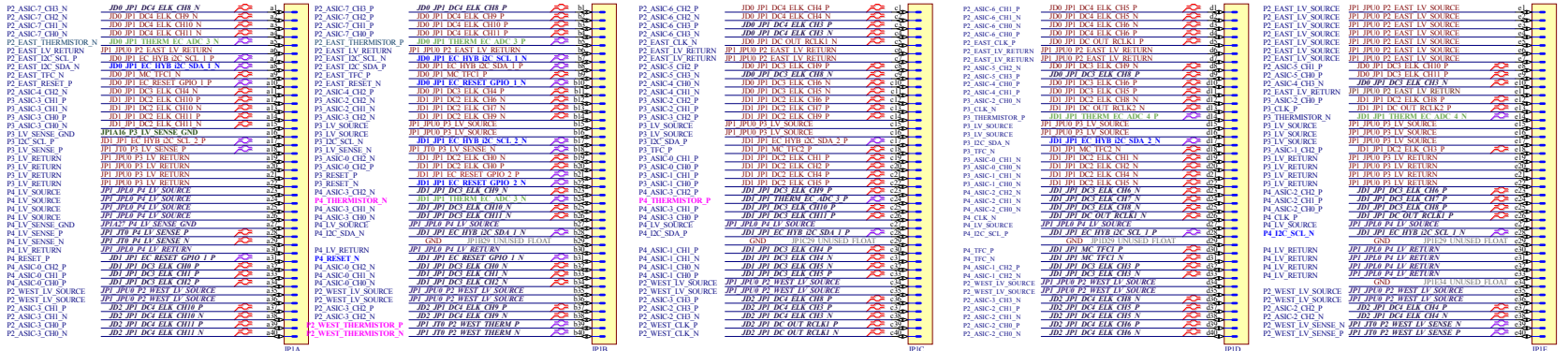
Pigtail 1

For REF: PigtailV3_Straight_Long

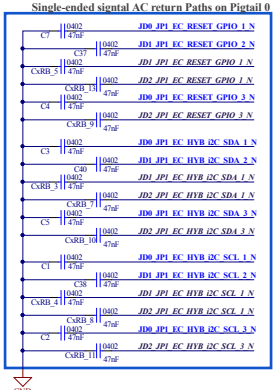
GENERAL COMMENTS:

EC_ADC_REF<15..13> ADC channels can be used to sample the hybrid ground sense.

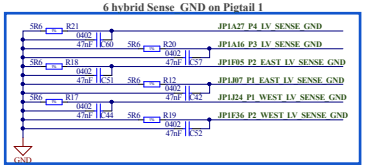
DCB slots 2,3, 10, and 11 can be depopulated for middle and outer backplanes. Therefore, the corresponding ED_ADC channels should be avoided for ground sense and backplane thermistor measurement inputs to ensure the intended measurement connections are available in each of the backplane locations once populated per elink map requirements.



Single-ended signtal AC return Paths on Pigtail 0



6 hybrid Sense GND on Pigtail 1



NOTE: P1_EAST_THERMISTOR, and P2_EAST_THERMISTOR are routed to the telemetry signal connector

List of Hybrid Power circuits that are not used in middle and outer backplanes (Therefore, the pigtail power breakout boards need to handle these cases)

JP1_JPU0_P4_LV_SOURCE

JP1_JPU0_P1_EAST_LV_SOURCE

JP1_JPU0_P4_LV_RETURN

JP1_JPU0_P1_EAST_LV_RETURN

JP1_JPU0_P2_WEST_LV_SOURCE

JP1_JPU0_P2_WEST_LV_RETURN

These resistors are installed for the middle and outer backplane locations ONLY

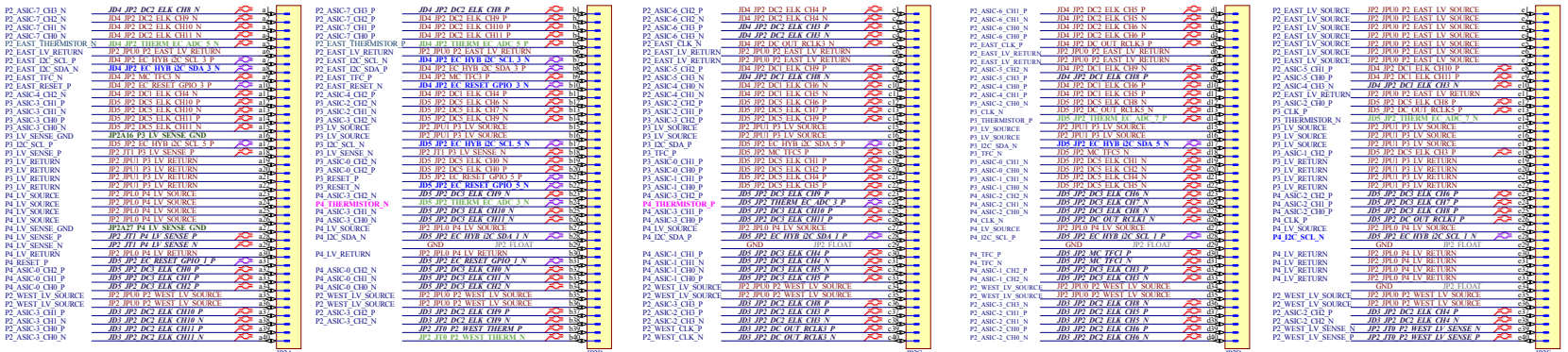
Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

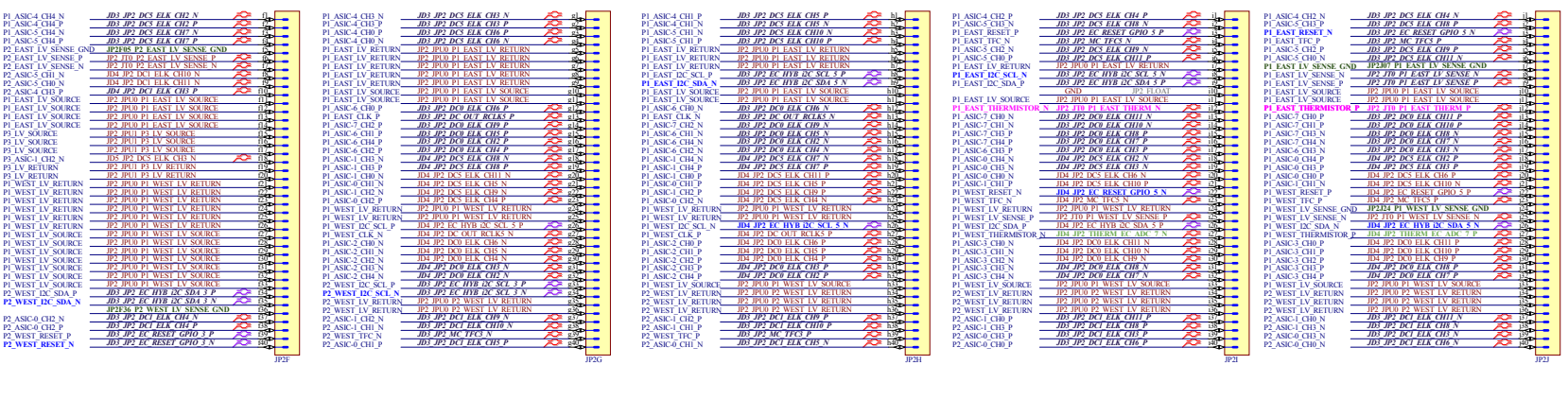
Project/Equipment	PEPI
Document	PEPI Backplane True - Pigtail Conn 1 -
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla
Check.by	B. Civel
Last Mod.	B. Civel
File:	Pigtail_Conns_1.SchDoc
Print Date:	6/20/2019 8:56:12 AM
Date	18/12/2018
	22/02/2019
	5/6/2019
Sheet	11 of 21
Size	A2
Rev	-

European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland

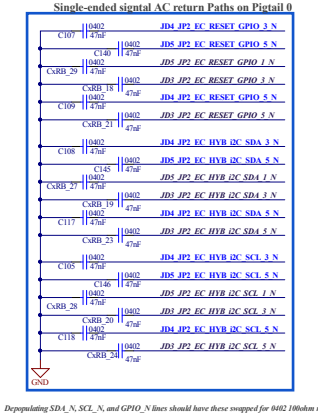
EDA-03992-V1-0

Pigtail 2

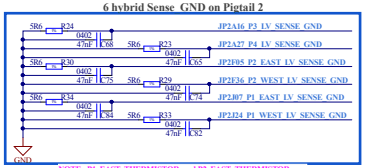




Single-ended signtal AC return Paths on Pigtail 0



6 hybrid Sense GND on Pigtail 2



NOTE: P1_EAST_THERMISTOR_ and P2_EAST_THERMISTOR are routed to the telemetry signal connector

List of Hybrid Power circuits that are not used in middle and outer backplanes (Therefore, the pigtail power breakout boards need to handle these cases)

JP1_JPL0_P4_LV_RETURN JP1_JPU0_P1_EAST_LV_RETURN

JP1_JPL0_P4_LV_RETURN JP1_JPU0_P1_EAST_LV_RETURN

JP1_JPU0_P2_WEST_LV_SOURCE

JP1_JPU0_P2_WEST_LV_RETURN

These resistors are installed for the middle and outer backplane locations ONLY

Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

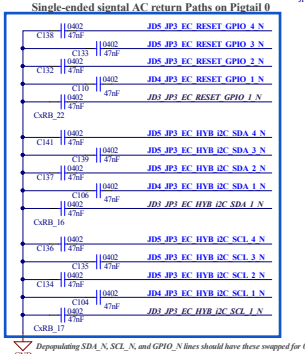
Project/Equipment	PEPI
Document	PEPI Backplane True - Pigtail Conn 2 -
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla — 18/12/2018
Check by	B. Civel — 22/02/2019
Last Mod.	B. Civel — 5/6/2019
File	Pigtail_Conns_2.SchDoc
Print Date	6/20/2019 8:56:14 AM
Sheet	12 of 21
Size	A2
Rev	-

European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland

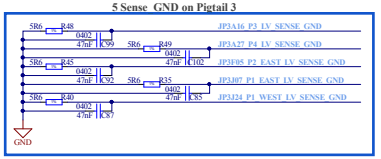
EDA-03992-V1-0

Pigtail 3

Single-ended signtal AC return Paths on Pigtail 0

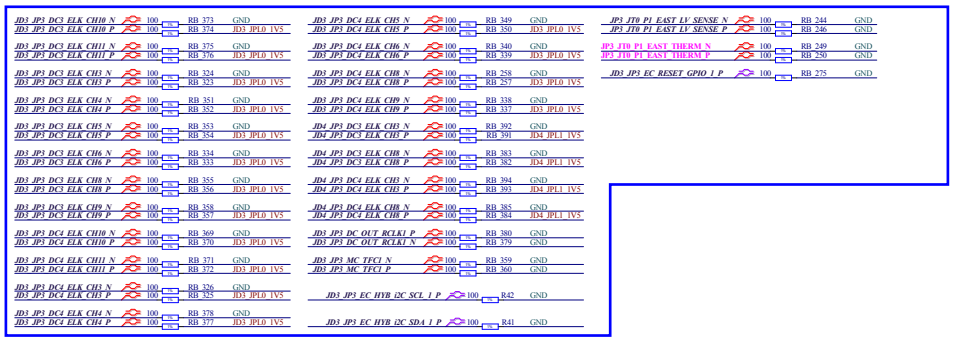


5 Sense_GND on Pigtail 3



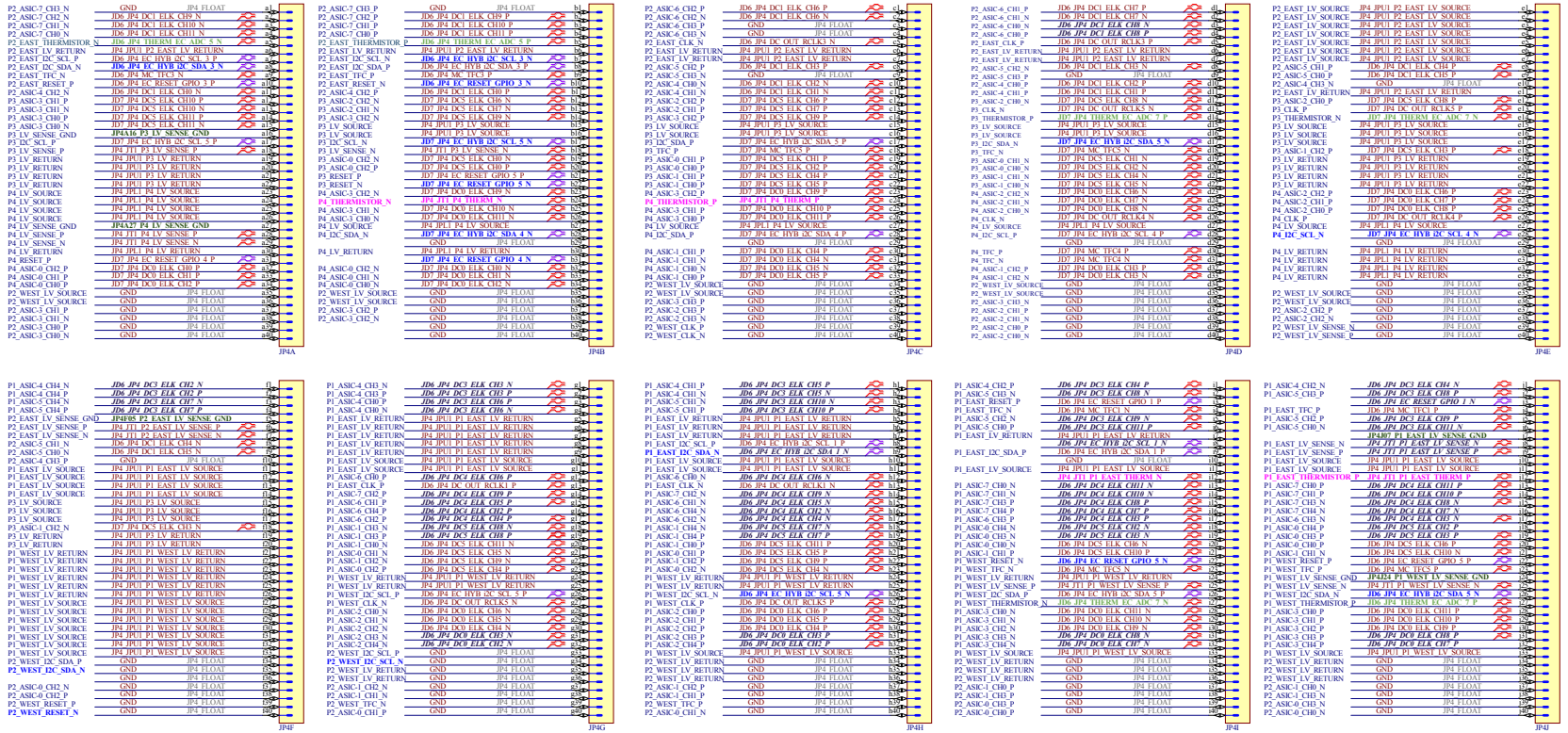
NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

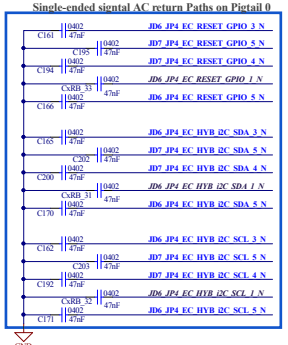
These resistors are installed for the middle and outer backplane locations ONLY



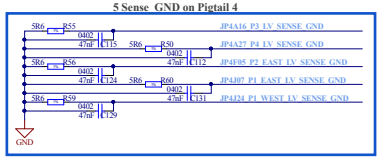
Project/Equipment	PEPI		
Document	PEPI Backplane True - Pigtail Conn 3 -		
TE/MPE		Designer M_Franco Sevilla	
CERN		Drawn by M_Franco Sevilla	18/12/2018
		Check.by B_Civel	22/02/2019
		Last Mod. B_Civel	5/6/2019
		File Pigtail_Conn_3.SchDoc	
		Print Date 6/20/2019 8:56:17 AM	Sheet 13 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-03992-V1-0	Rev -
			Size A2

Pigtail 4

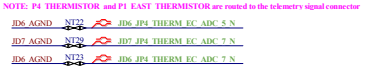




Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)



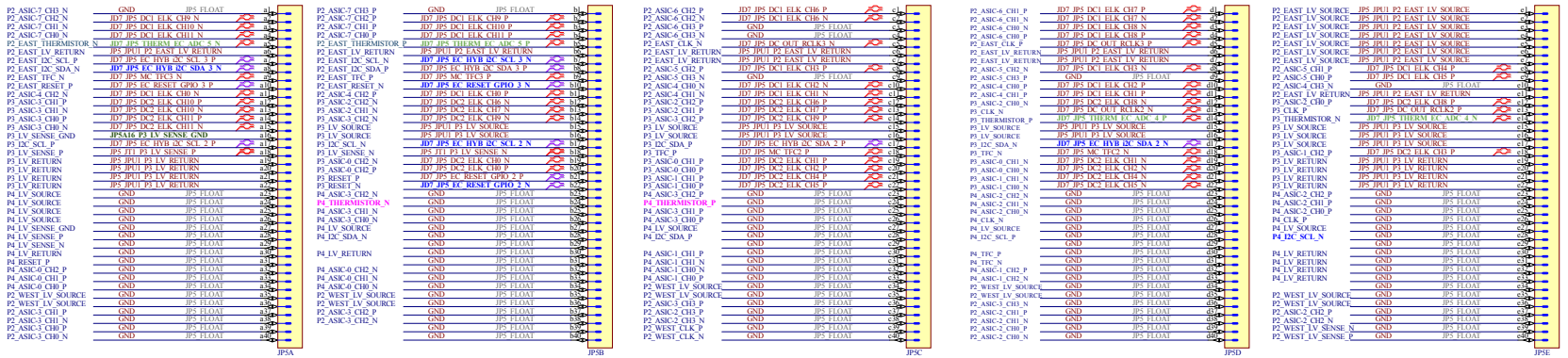
NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

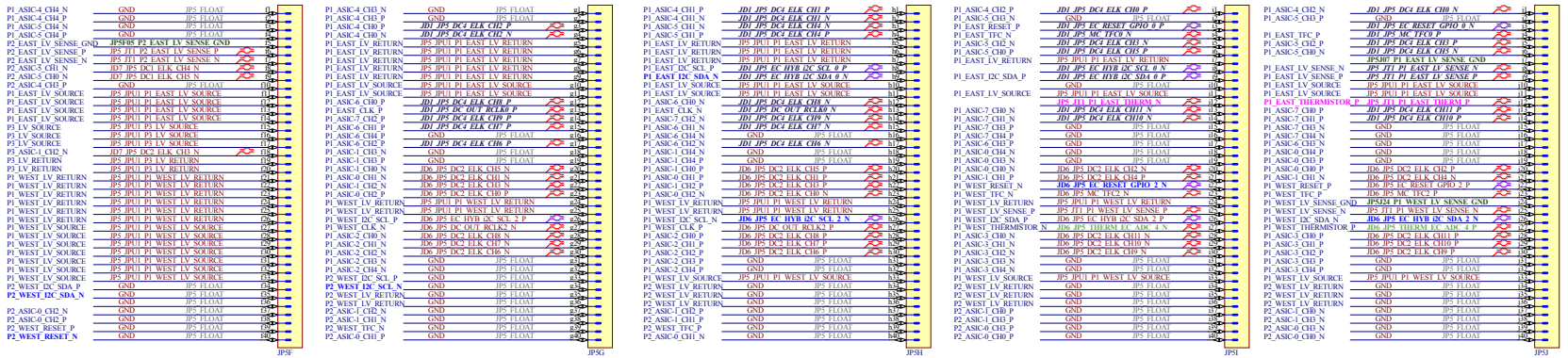


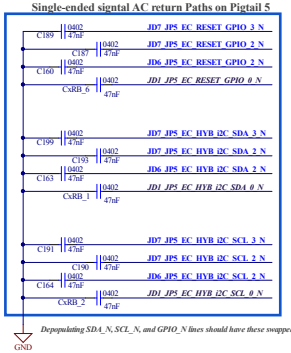
These resistors are installed for the middle and outer backplane locations ONLY

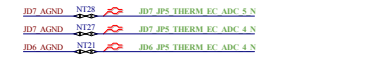
Project/Equipment	PEPI
Document	PEPI Backplane True - Pigtail Conn 4 -
TE/MPE	
Designer M. Franco Sevilla	
Drawn by M. Franco Sevilla	18/12/2018
Check by B. Civel	22/02/2019
Last Mod. B. Civel	5/6/2019
File: Pigtail_Conns_4.SchDoc	
Print Date 6/20/2019 8:56:19 AM	Sheet 14 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland	EDA-03992-V1-0
	Size A2

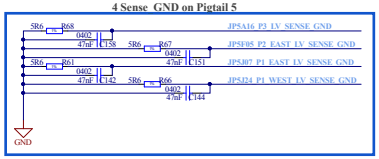
Pigtail 5







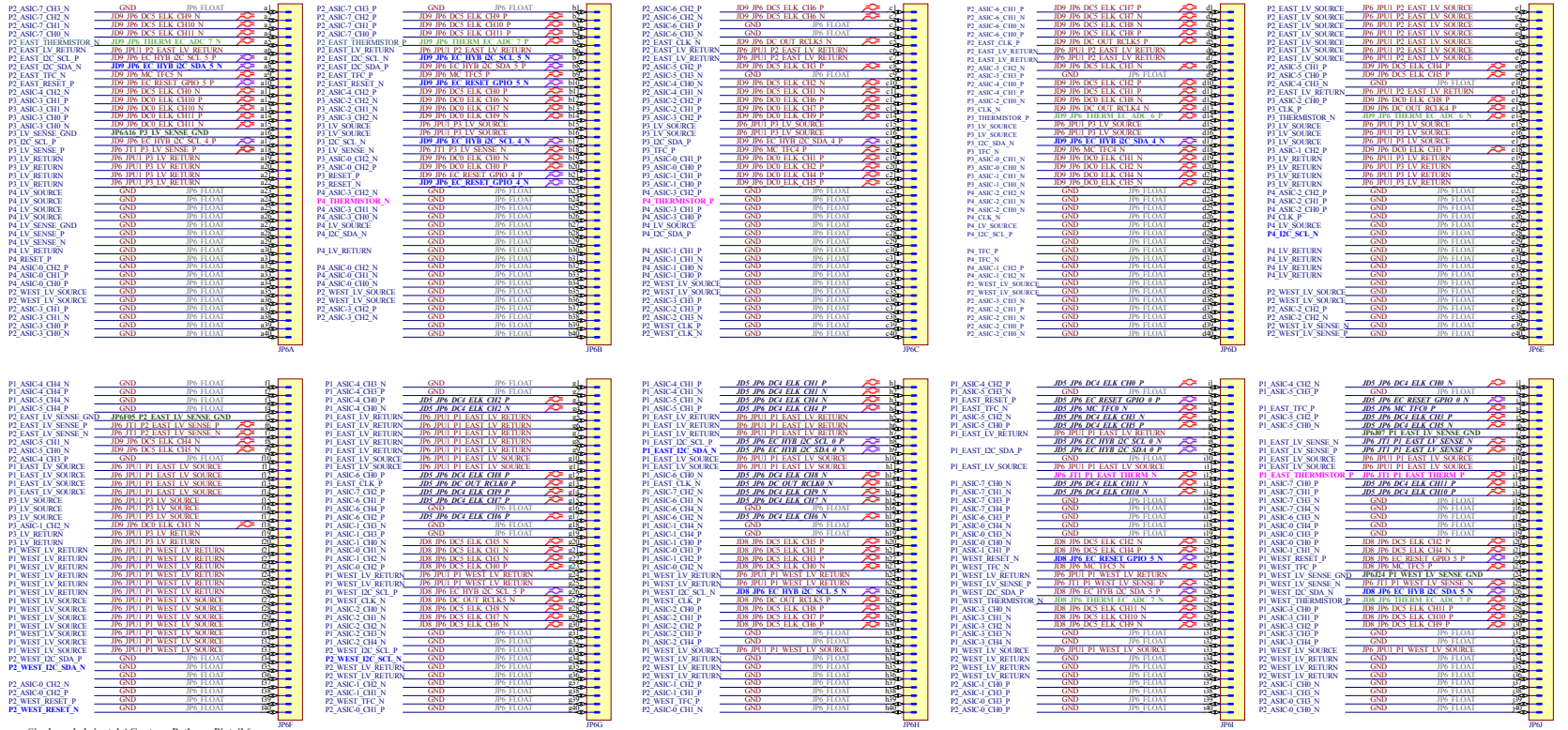


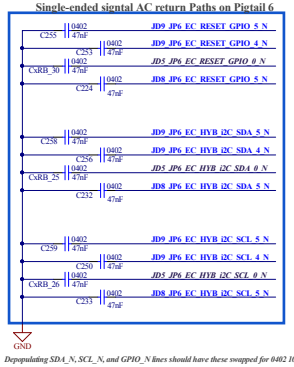


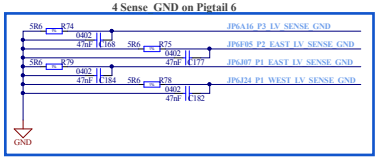
These resistors are installed for the middle and outer backplane locations ONLY

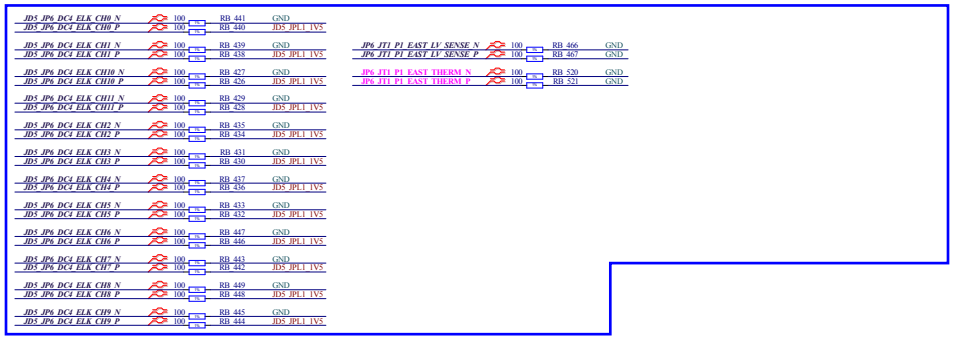
Project/Equipment PEPI
Document
TE/MPE
PEPI Backplane True - Pigtail Conn 5 -
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland
Designer M. Franco Sevilla
Drawn by M. Franco Sevilla 18/12/2018
Check.by B. Civel 22/02/2019
Last Mod. B. Civel 5/6/2019
File: Pigtail_Conn_5.SchDoc
Print Date 6/20/2019 6:56:20 AM Sheet 15 of 21
EDA-03992-V1-0 A2

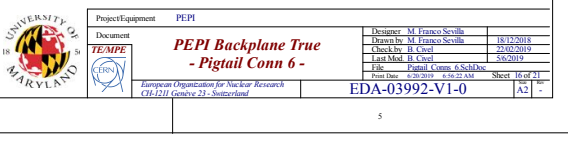
Pigtail 6









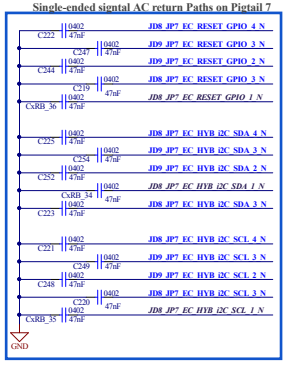


Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

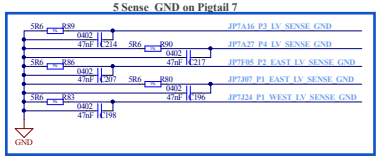
These resistors are installed for the middle and outer backplane locations ONLY

NOTE: P4 THERMISTOR and P1 EAST THERMISTOR are routed to the telemetry signal connector

Pigtail 7

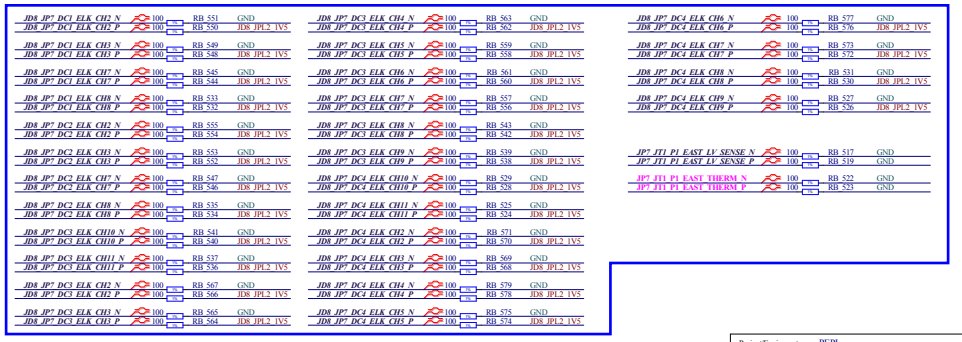


Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)



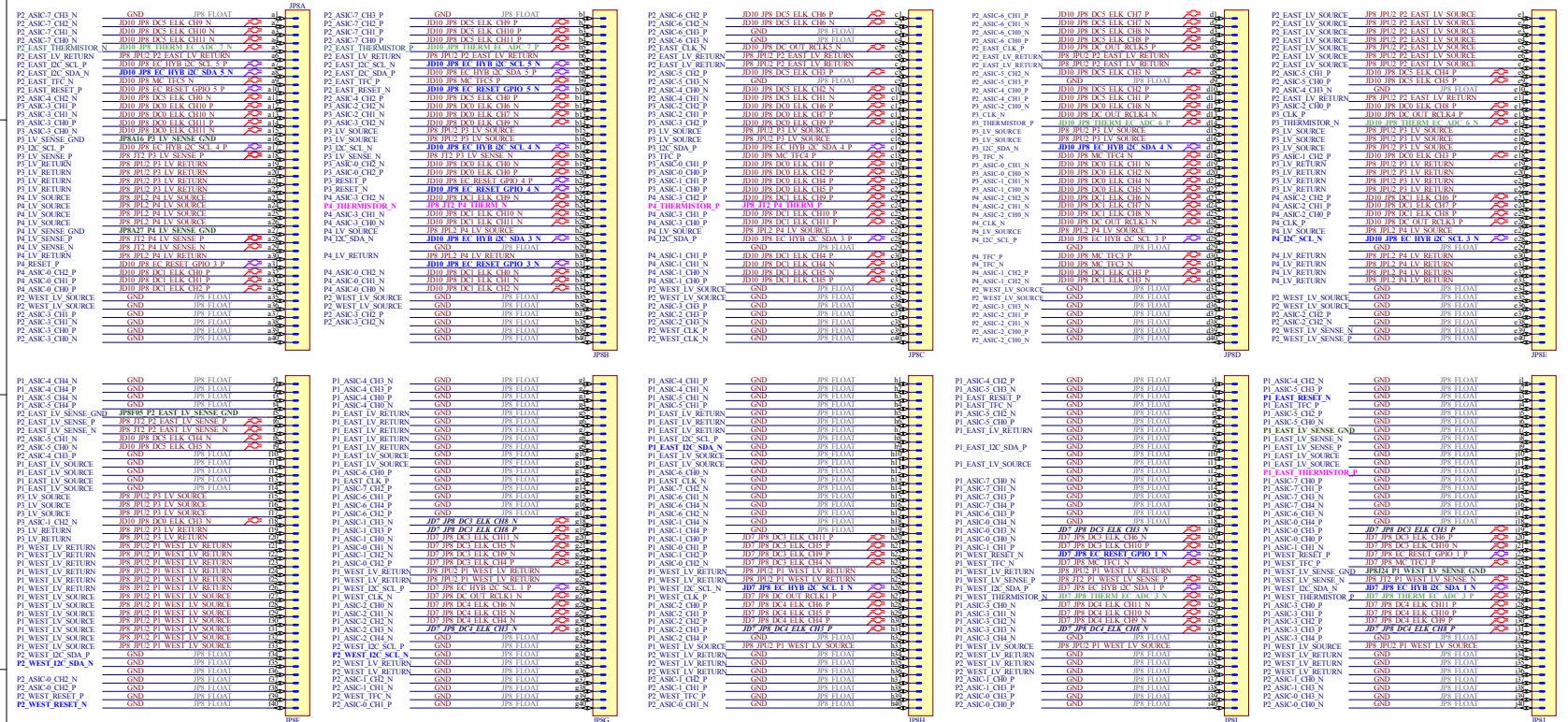
NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

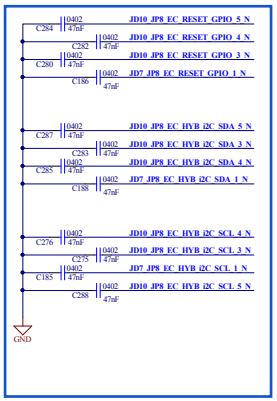
These resistors are installed for the middle and outer backplane locations ONLY



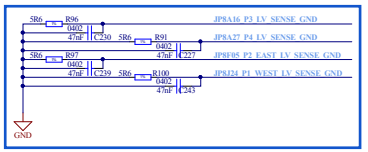
Project/Equipment	PEPI		
Document	PEPI Backplane True - Pigtail Conn 7 -		
TE/MPE		Designer M. Franco Sevilla	
CERN		Drawn by M. Franco Sevilla	18/12/2018
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		Check.by B. Civel	22/02/2019
		Last Mod. B. Civel	5/6/2019
		File: Pigtail_Conn_7.SchDoc	
		Print Date 6/20/2019 8:56:34 AM	Sheet 17 of 21
	EDA-03992-V1-0		A2 -

Pigtail 8





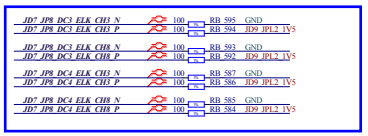
Single-ended signtal AC return Paths on Pigtail 8

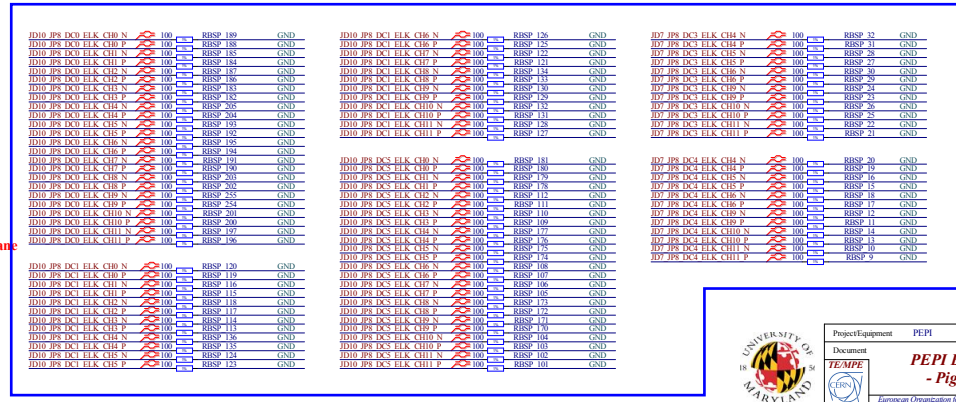


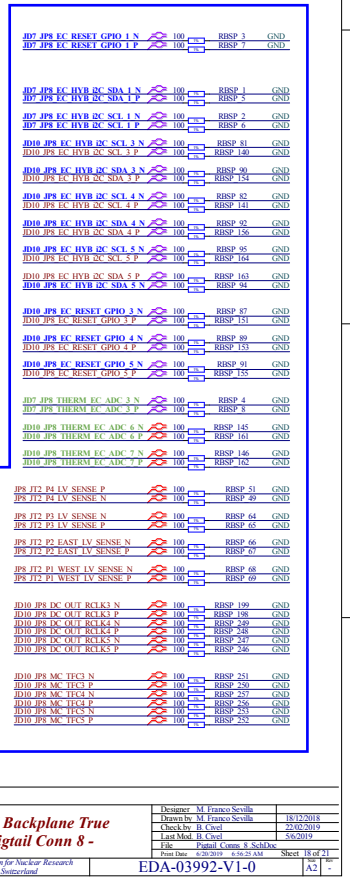
4 Sense_GND on Pigtail 8

These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)

These resistors are installed for the middle and outer backplane locations ONLY

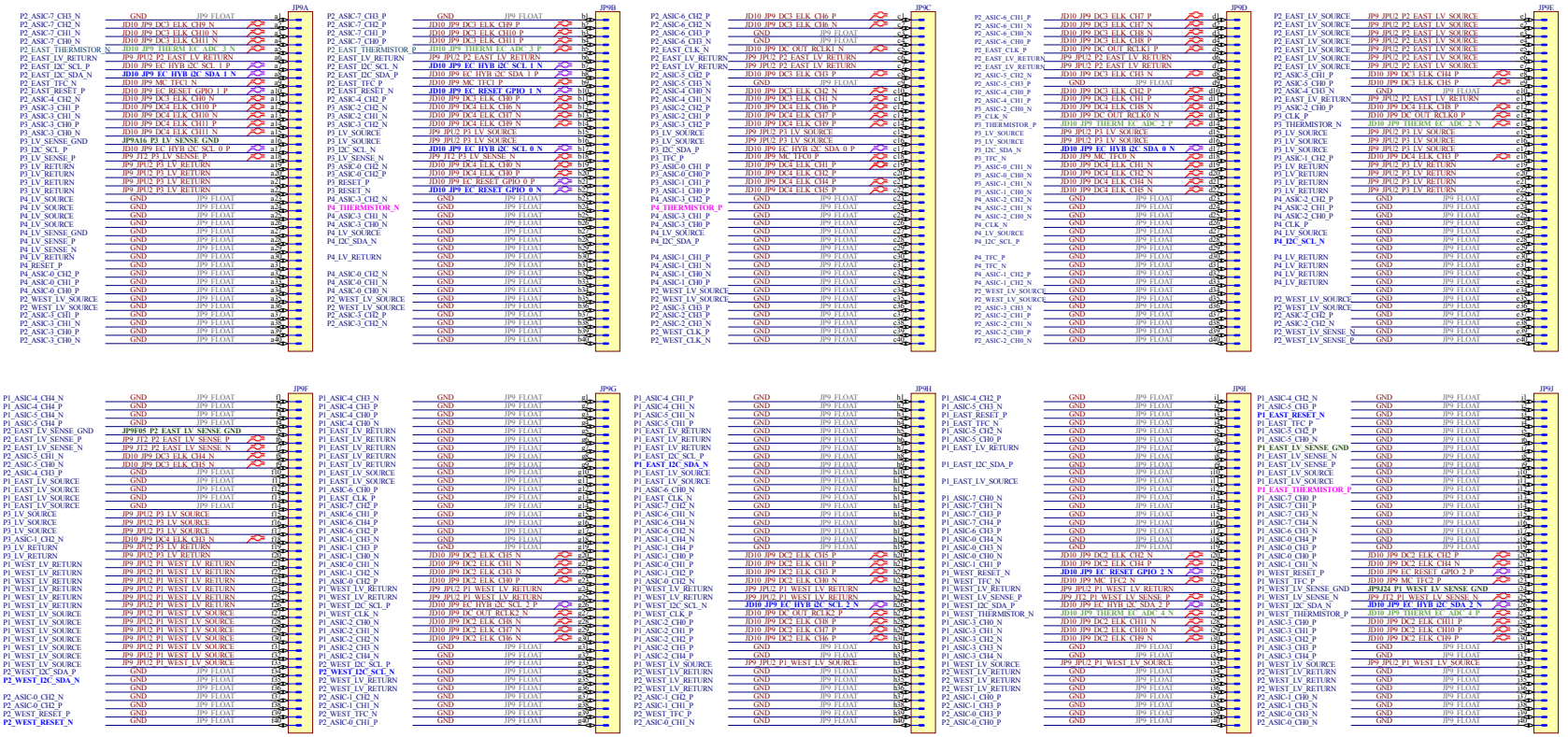




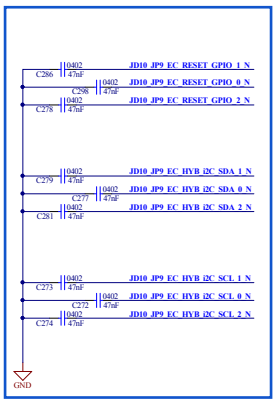


Project/Equipment	PEPI		
Document	*PEPI Backplane True - Pigtail Conn 8 -*		
TE/MPE		Designer M. Franco Sevilla	
		Drawn by M. Franco Sevilla	18/12/2018
		Check.by B. Civel	22/02/2019
		Last Mod. B. Civel	5/6/2019
		File: Pigtail_Conns_8_SchDoc	
		Print Date 6/20/2019 6:56:25 AM	Sheet 18 of 21
European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland		EDA-03992-V1-0	Size A2 / Rev -

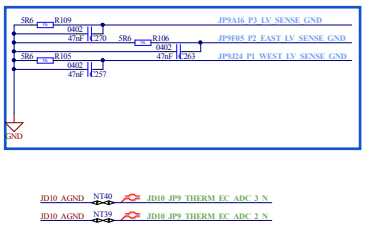
Pigtail 9



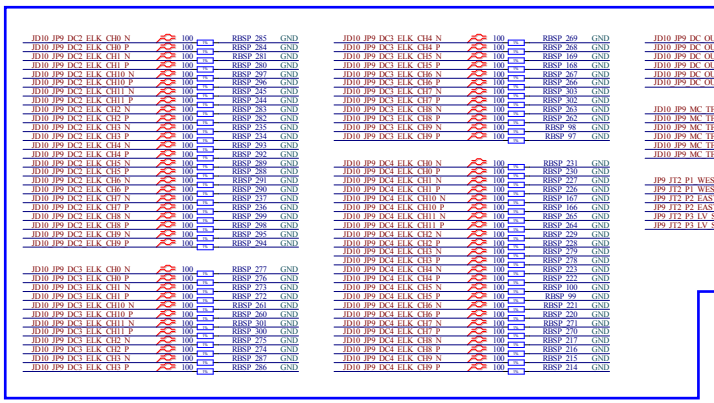
Single-ended signtal AC return Paths on Pigtail 9



3 Sense_GND on Pigtail 9



These resistors are installed for the outer "A" Plane backplane locations ONLY (Since Pigtails JP<8 .. 11> are absent)

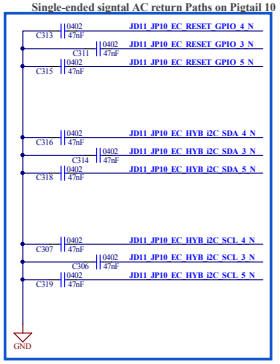


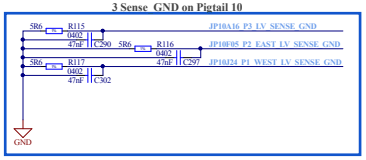
Project/Equipment	PEPI
Document	PEPI Backplane True - Pigtail Conn 9 -
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla — 18/12/2018
Check.by	B. Civel — 22/02/2019
Last Mod.	B. Civel — 5/6/2019
File	Pigtail_Conns_9.SchDoc
Print Date	6/20/2019 — 6:56:28 AM — Sheet 19 of 21
Size	A2
Rev	-
	EDA-03992-V1-0

European Organization for Nuclear Research CH-1211 Geneva 23 - Switzerland

Pigtail 10

These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)





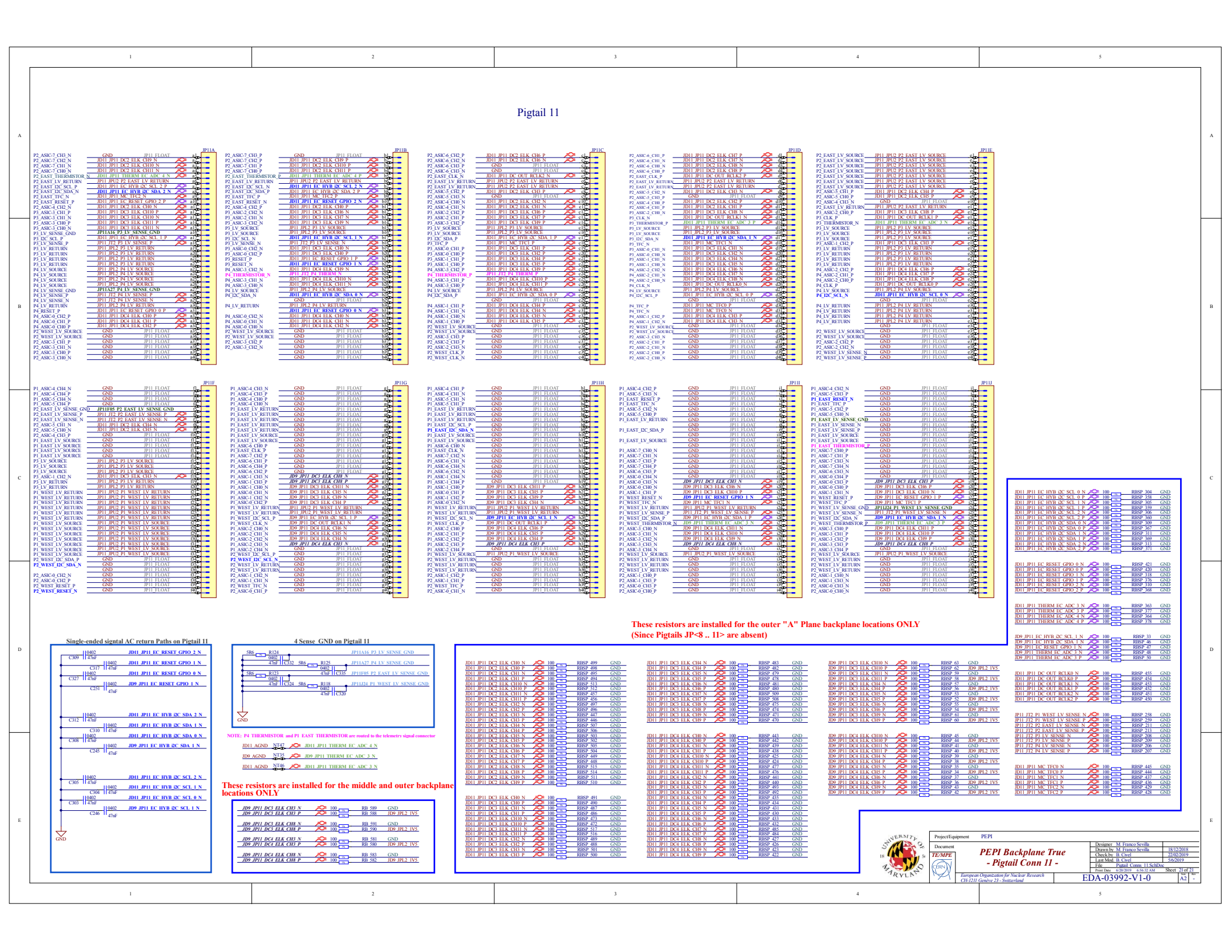
NOTE: P4 THERMISTOR and P1 EAST THERMISTOR are routed to the telemetry signal connector

JD11_AGND_NT49 — JD11_JP10_THERM_EC_ADC_6_N
JD11_AGND_NT48 — JD11_JP10_THERM_EC_ADC_5_N
JD11_AGND_NT50 — JD11_JP10_THERM_EC_ADC_7_N

Project/Equipment	PEPI
Document	PEPI Backplane True - Pigtail Conn 10 -
Designer	M. Franco Sevilla
Drawn by	M. Franco Sevilla — 18/12/2018
Check.by	B. Civel — 22/02/2019
Last Mod.	B. Civel — 5/6/2019
File	Pigtail_Conns_10.SchDoc
Print Date	6/20/2019 6:56:30 AM — Sheet 20 of 21
	EDA-03992-V1-0 — Size A2 — Rev -

TE/MPE — European Organization for Nuclear Research, CH-1211 Geneva 23 - Switzerland

Pigtail 11


JP11A
JP11B
JP11C
JP11D
JP11E
JP11F
JP11G
JP11H
JP11I
Single-ended signtal AC return Paths on Pigtail 11
4 Sense GND on Pigtail 11
NOTE: P4 THERMISTOR and P1 EAST THERMISTOR are routed to the telemetry signal connector
These resistors are installed for the middle and outer backplane locations ONLY
These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)
PEPI Backplane True
- Pigtail Conn 11 -
EDA-03992-V1-0
Designer M. Franco Sevilla
Drawn by M. Franco Sevilla
Checked by B. Civel
Last Mod. B. Civel
File: Pigtail_Conns_11.SchDoc
Sheet 21 of 21