

A

A

B

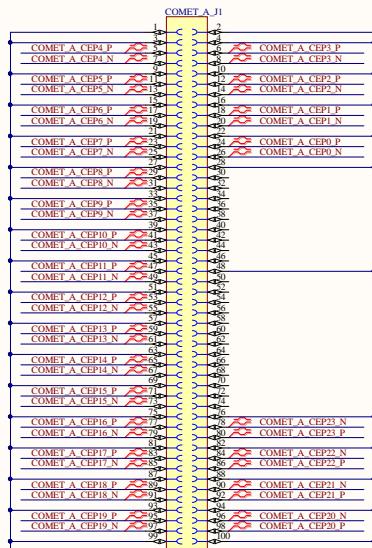
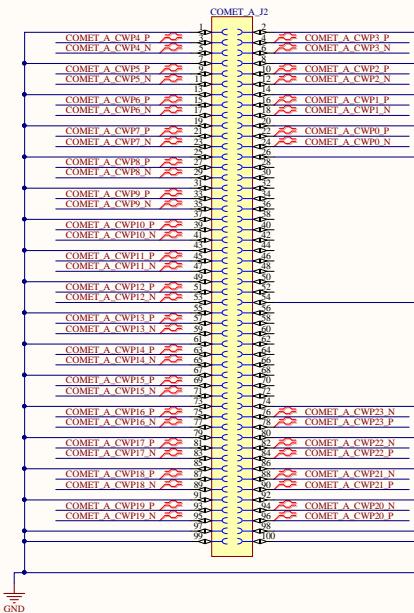
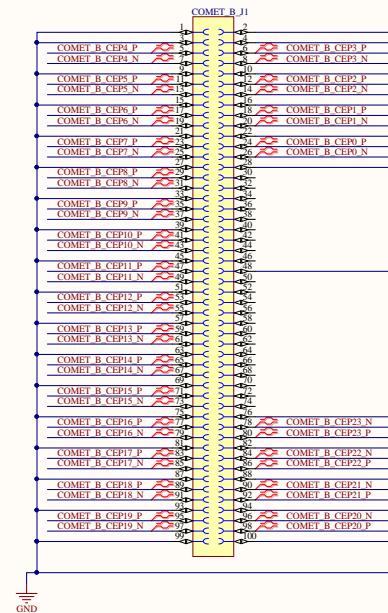
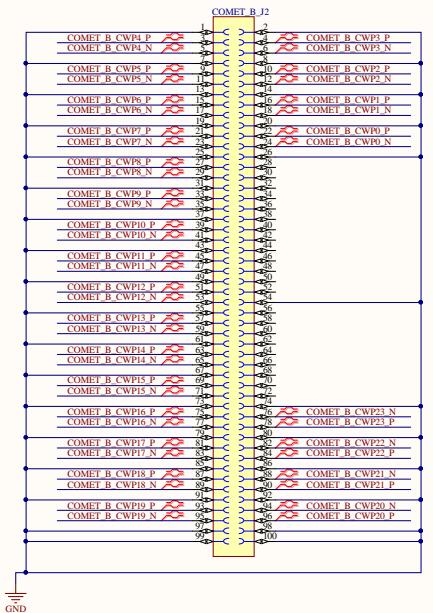
B

C

C

D

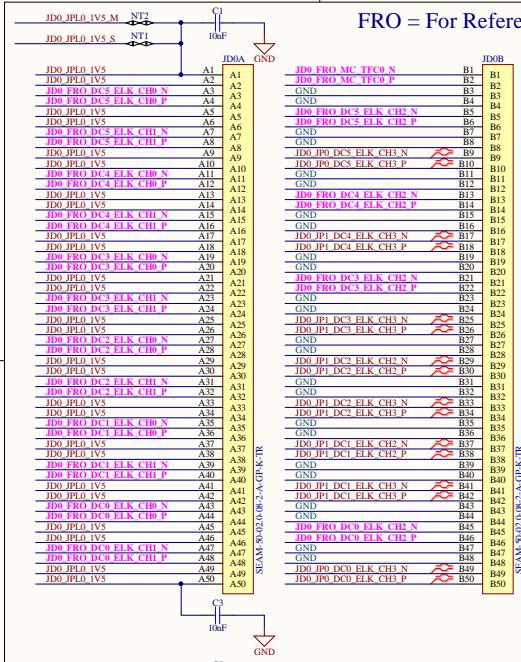
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ST_CONN_EAST: COMET 'A'**ST_CONN_WEST: COMET 'A'****ST_CONN_EAST: COMET 'B'****ST_CONN_WEST: COMET 'B'**

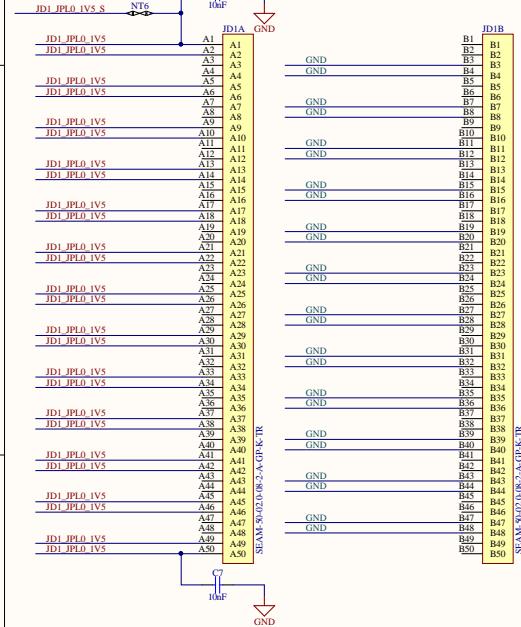
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Size	Number	Revision
C		
Date:	7/23/2018	Sheet of
File:	C:\Users...\COMET\TestSupport.SchDoc	Drawn By:

FRO = For Reference Only

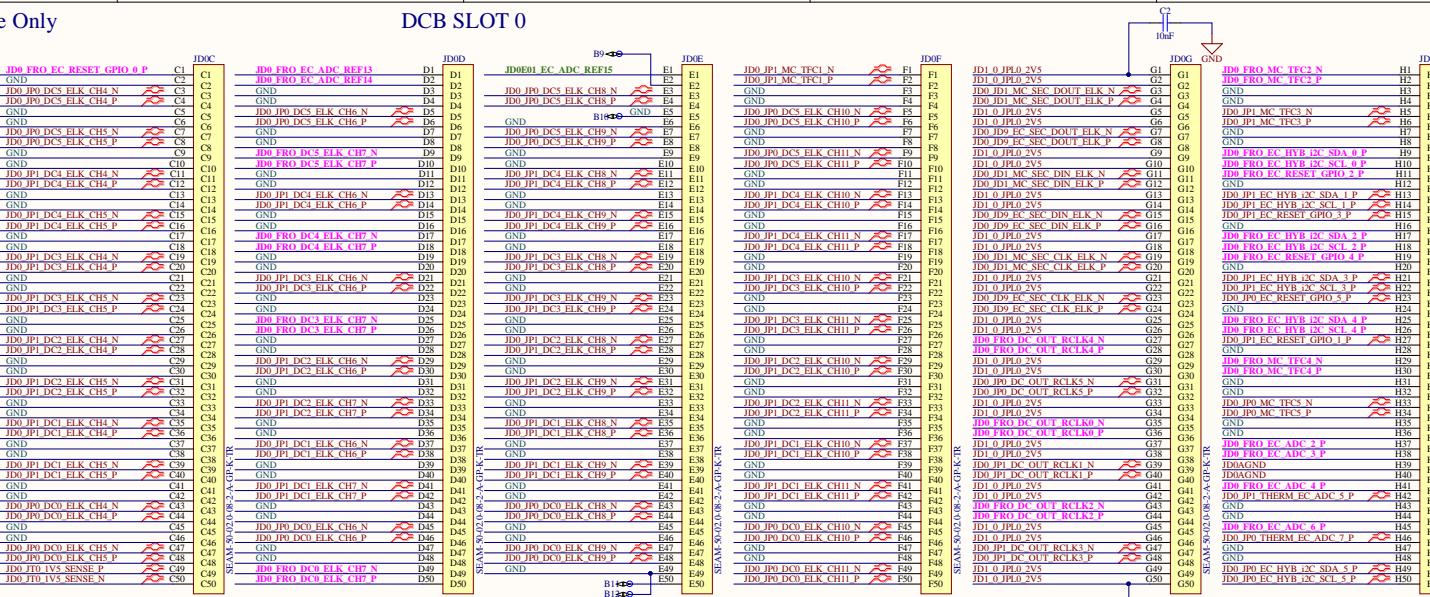
DCB SLOT 0



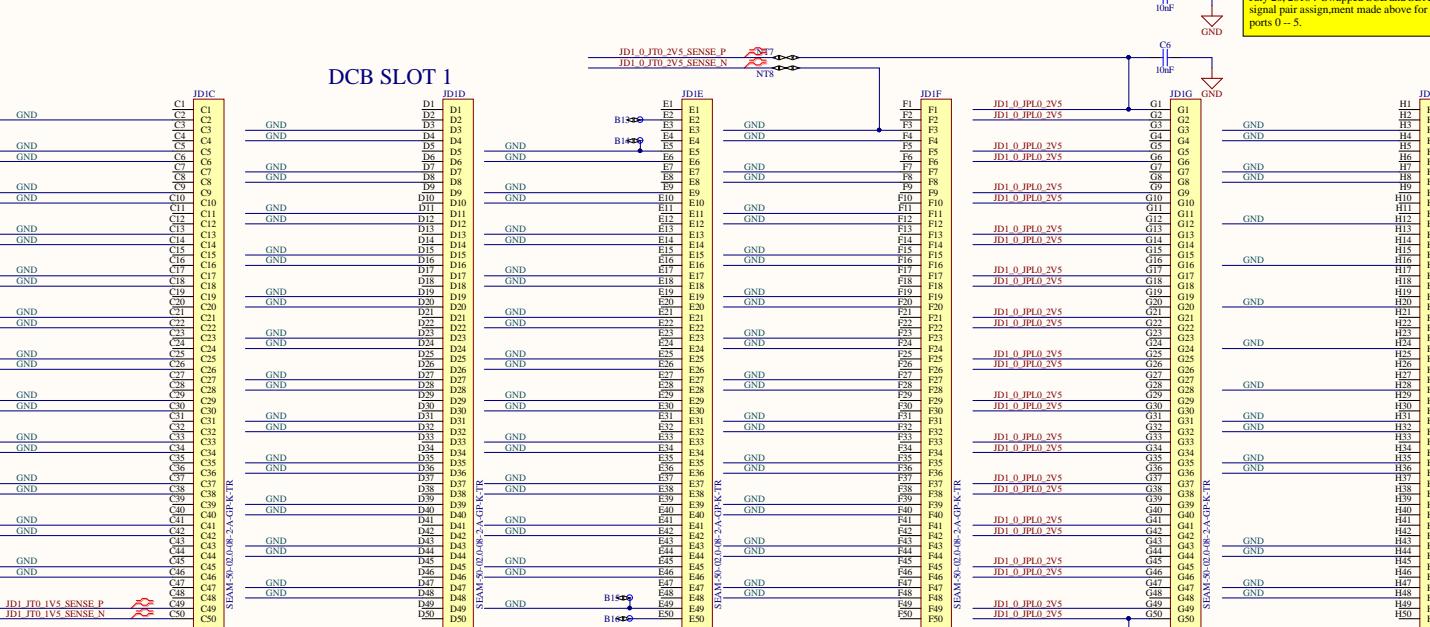
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SIAM-S90/02/08-B-GPK-KR



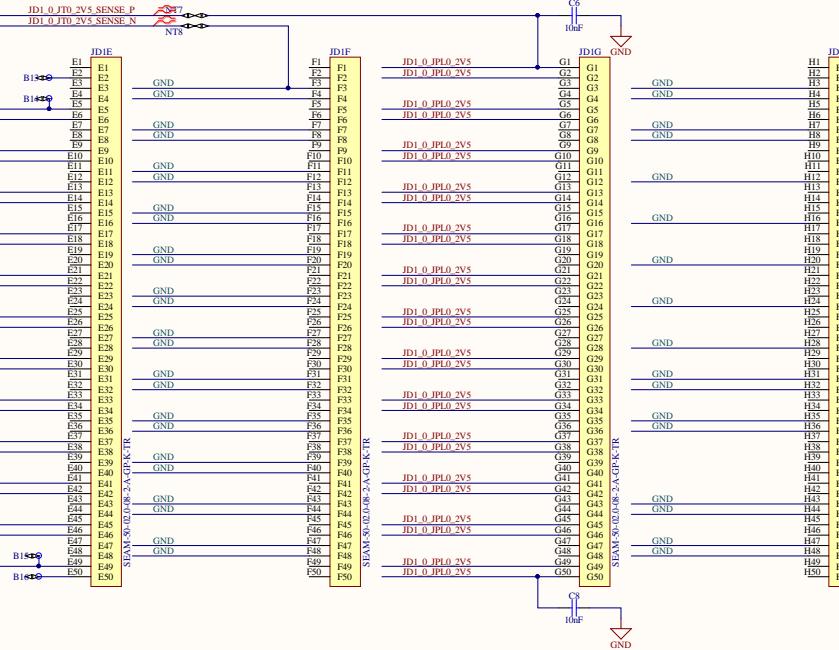
SIAM-S90/02/08-B-GPK-KR



SIAM-S90/02/08-C-GPK-KR

July 20, 2018 : Swapped SCL and SDA signal pair assignment made above for ports 0 - 5.

DCB SLOT 1



SIAM-S90/02/08-C-GPK-KR

Pathfinder Backplane		
c	Number	Revision
DCB Slot Connector	A	
Date:	7/23/2018	Sheet of
File:	C:\Users\JDC\Comms\1.SchDoc	Drawn By:

1

2

3

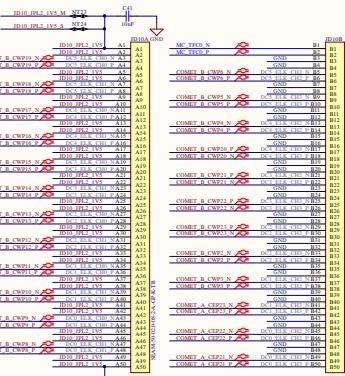
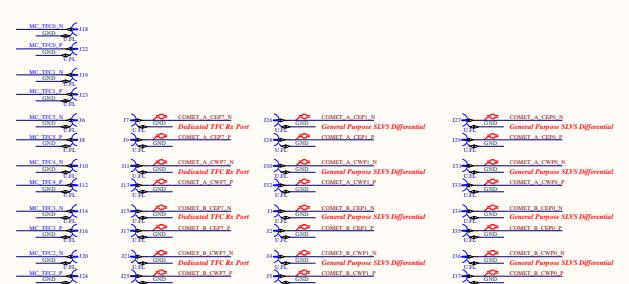
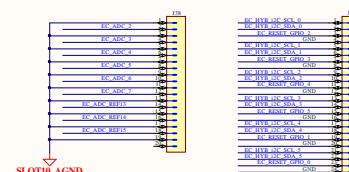
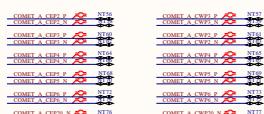
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5

6

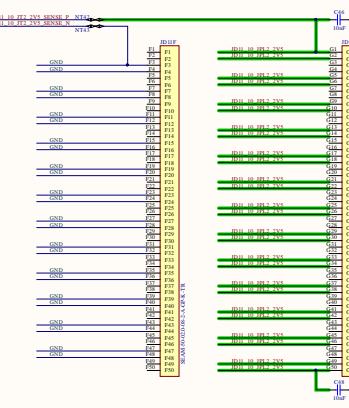
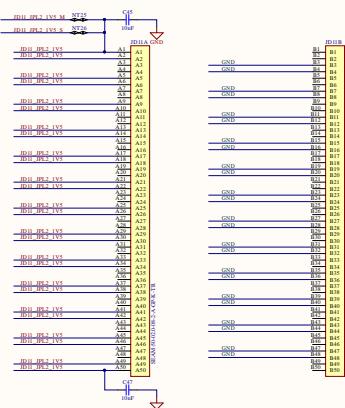
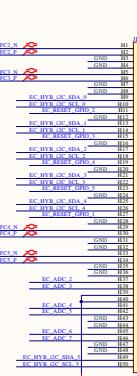
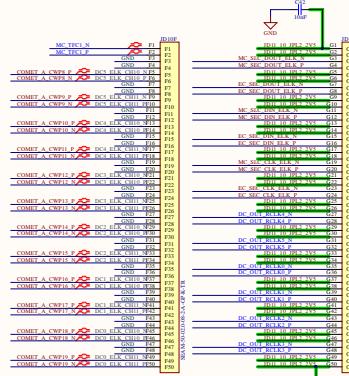
7

8



DCB SLOT 10--SPECIAL DCB TEST SLOT (FULL DCB)

DCB SLOT 11

Pathfinder Backplane
DCB Slot Connector A

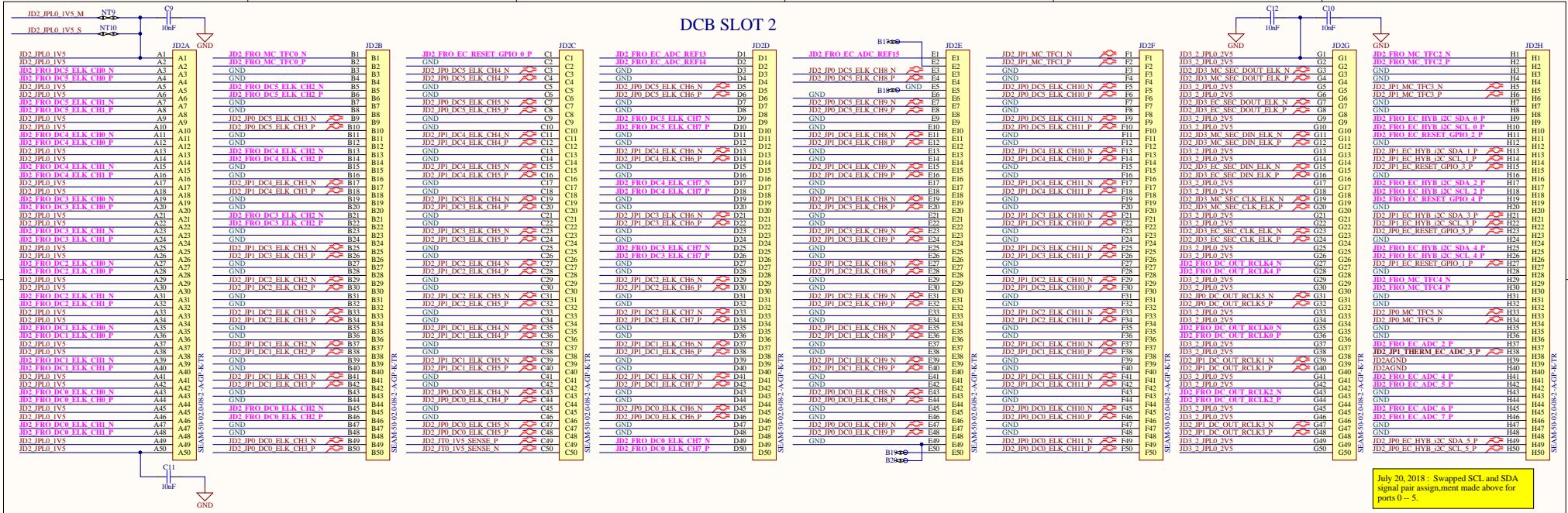
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Line State Number Revision

1 Open 10-0000000000000000 A

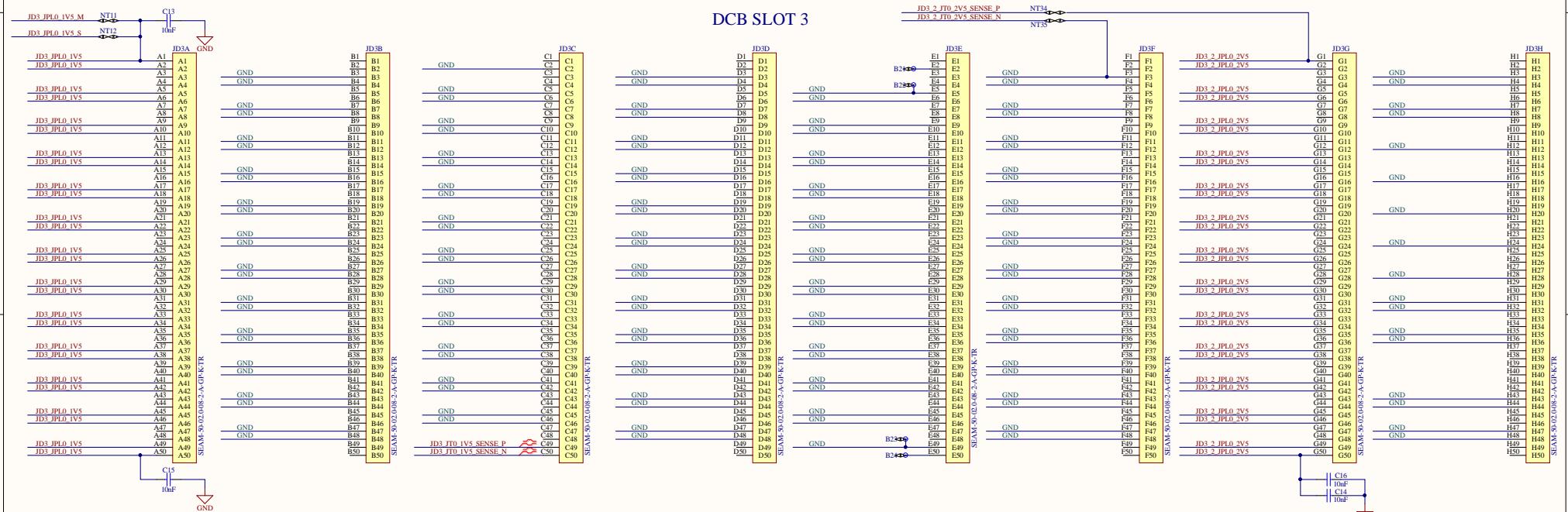
Line State Number Revision

DCB SLOT 2

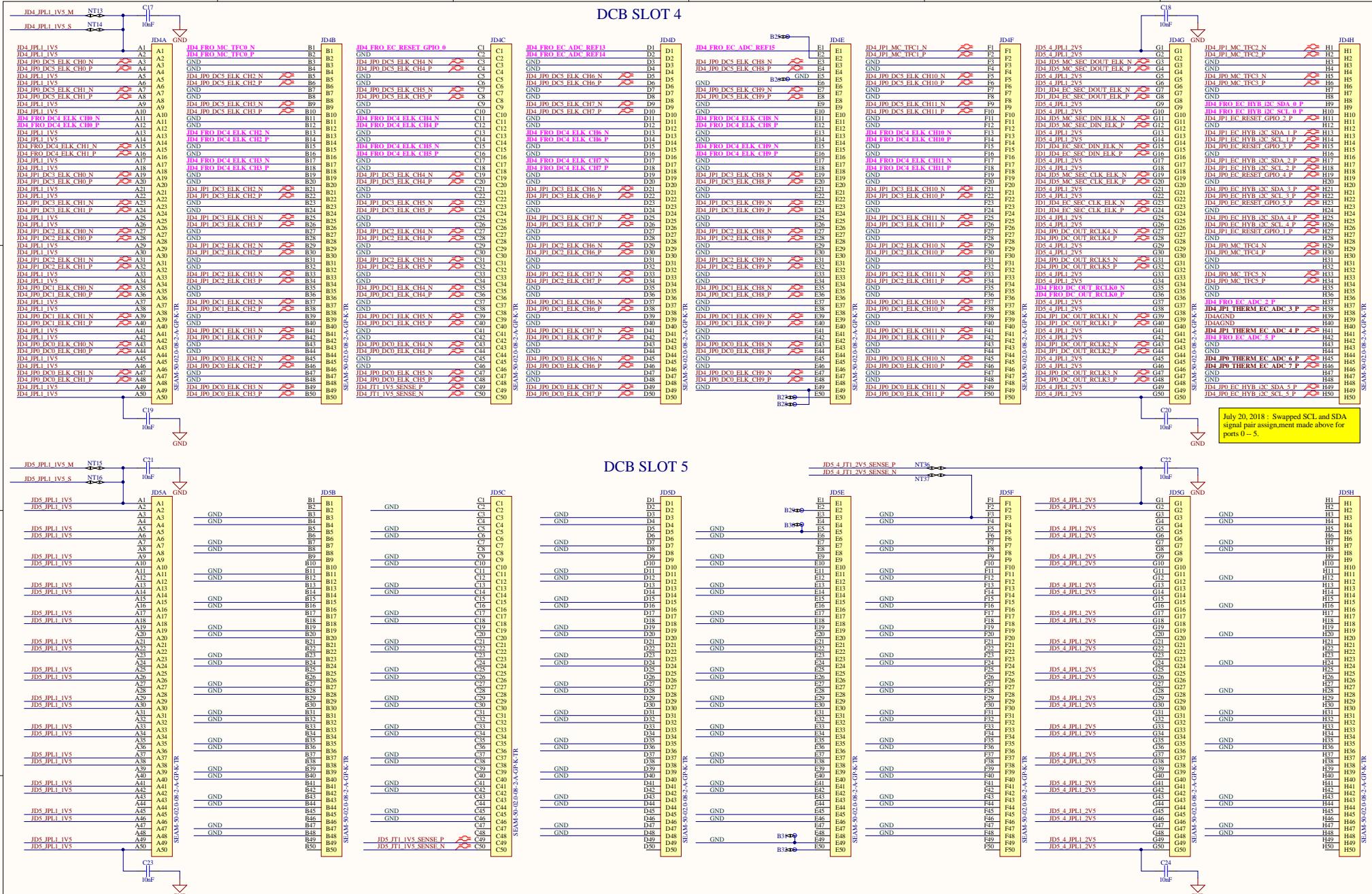


July 20, 2018 : Swapped SCL and SDA signal pair assignment made above for ports 0 - 5.

DCB SLOT 3

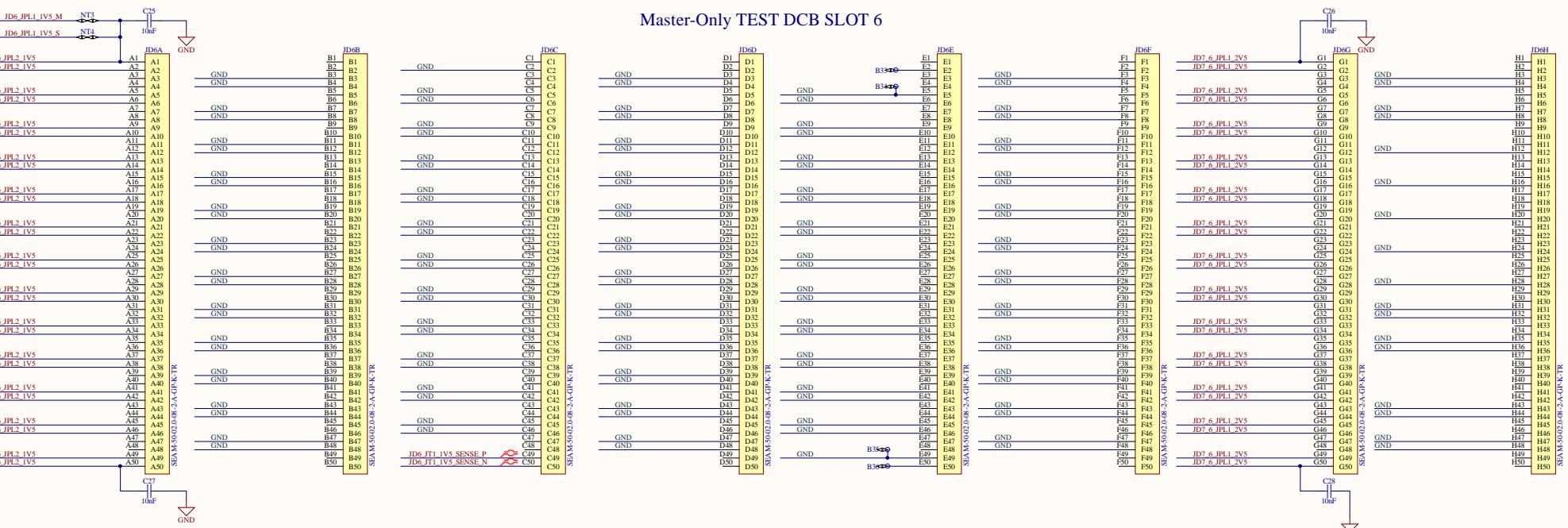
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Pathfinder Backplane

Size	Number	Revision
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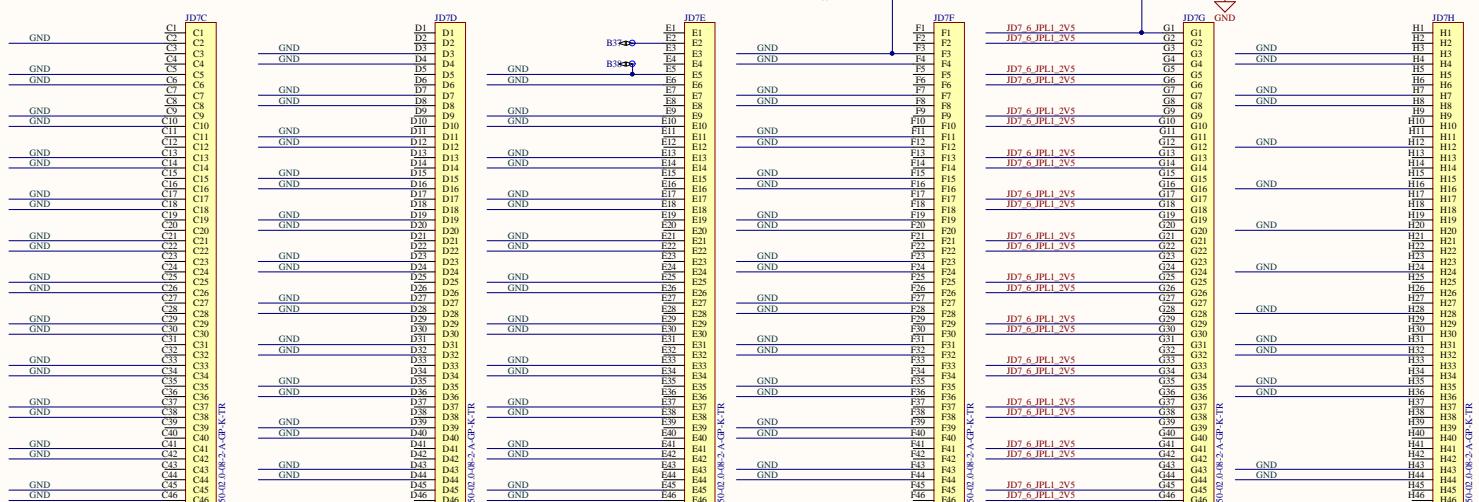


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Size: c	Number: DBC Slot Connector	Revision: A
Date: 7/23/2018	Sheet of 1	Drawn By:
File: C:\Users\JDC\Comms\4.SchDoc		

Master-Only TEST DCB SLOT 6



DCB SLOT 7

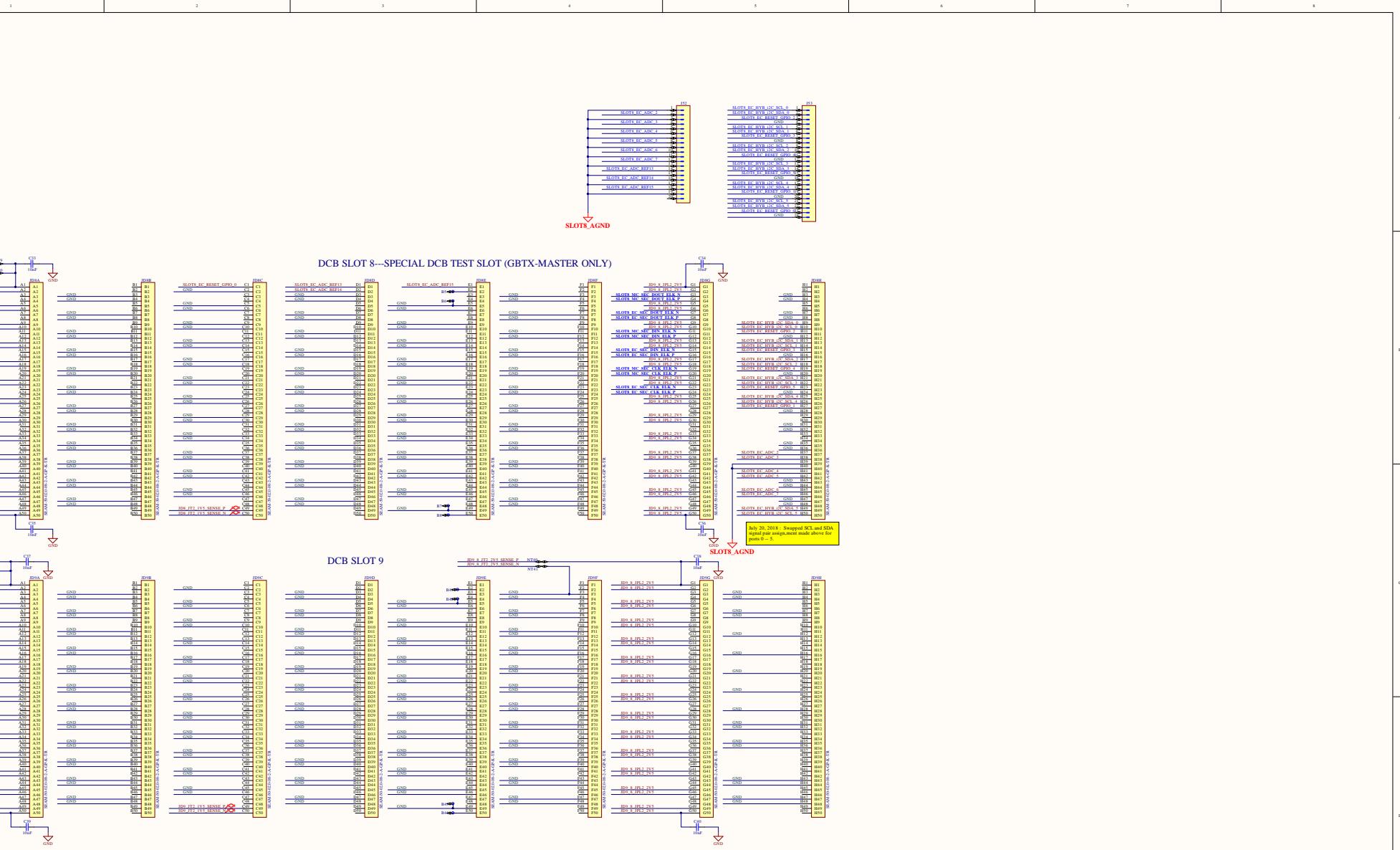


Title
Pathfinder Backplane

Size	Number	Revision
c	DCB Slot Connector	A

Date: 7/23/2018 Sheet of 1 Drawn By:

File: C:\Users\DCB_Conns\6.SchDoc



Rev	Date	Sheet Number	Revision
F0	7/20/2018	0000	A

NOTES:

FP² are placeholders for floating copper. These could be pressed against a carbon-impregnated foam to bleed charge, if needed.

Bright Blue = AC signal reference ground return

Dark Green = Floating DC Hybrid reference ground return

Light Green = Thermistors

Fuscia = Telemetry Thermistors for connections External to PEPI

These italics signals are not used in the middle and outer backplane locations

GENERAL GROUND RETURN RULES APPLIED

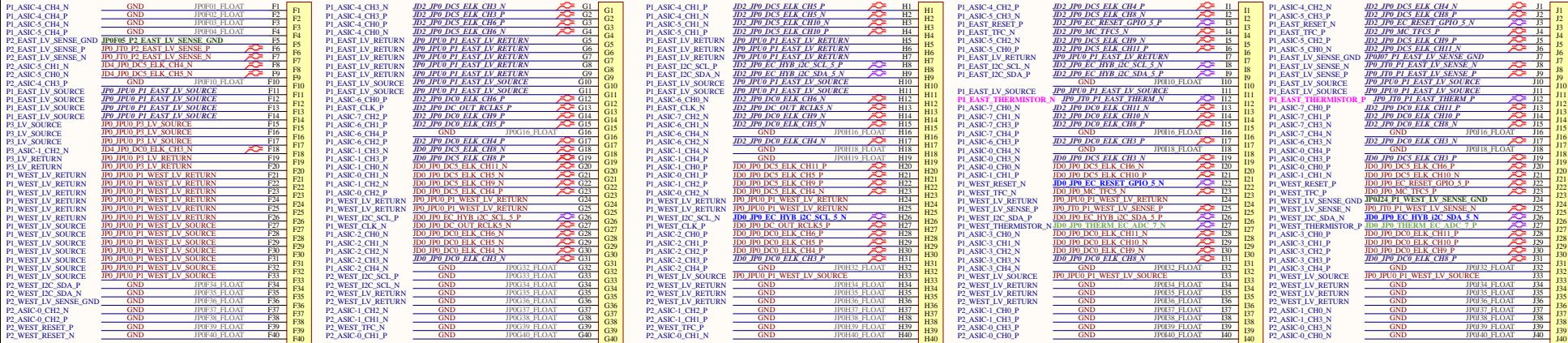
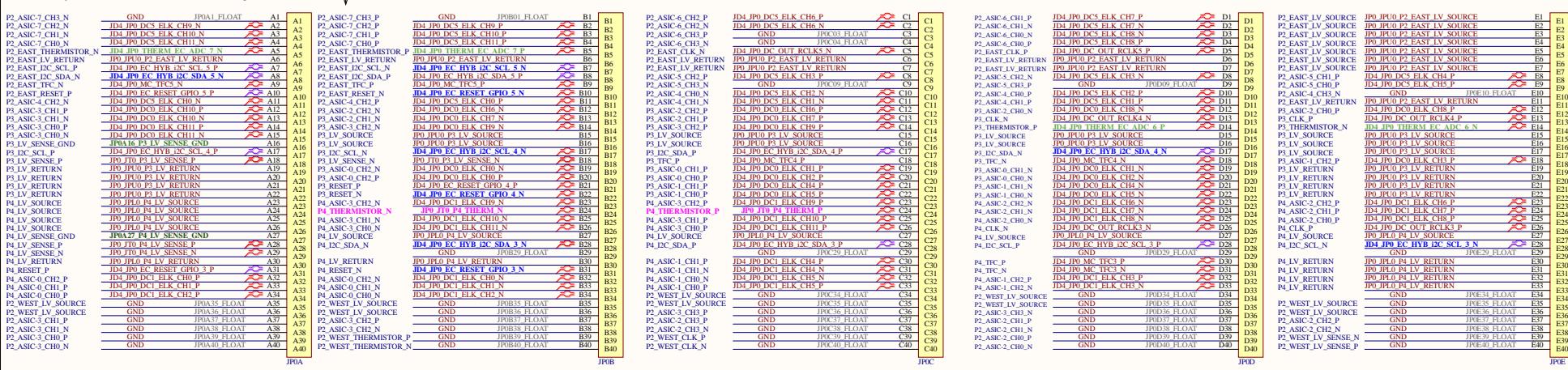
- 1) Each floating hybrid ground board is connected directly to the corresponding source regulator return path.

a.) But DC levels relative to the main backplane ground are maintained via ground sense resistor connected to the main backplane ground. This also has a small parallel EMI cap to shunt high frequency noise.

- 2) Every single-ended signal from each hybrid has a dedicated ground reference return that is connected to the main backplane ground via a small EMI cap to allow for a high frequency return path only.

- 3) Analog ground for the PT100 sensors is intentionally separate from the main backplane ground.

For REF: PigtailV3_Straight_Long

**Pigtail 0****GENERAL COMMENTS:**

EC_ADC_REF<15..13> ADC channels can be used to sample the hybrid ground sense.

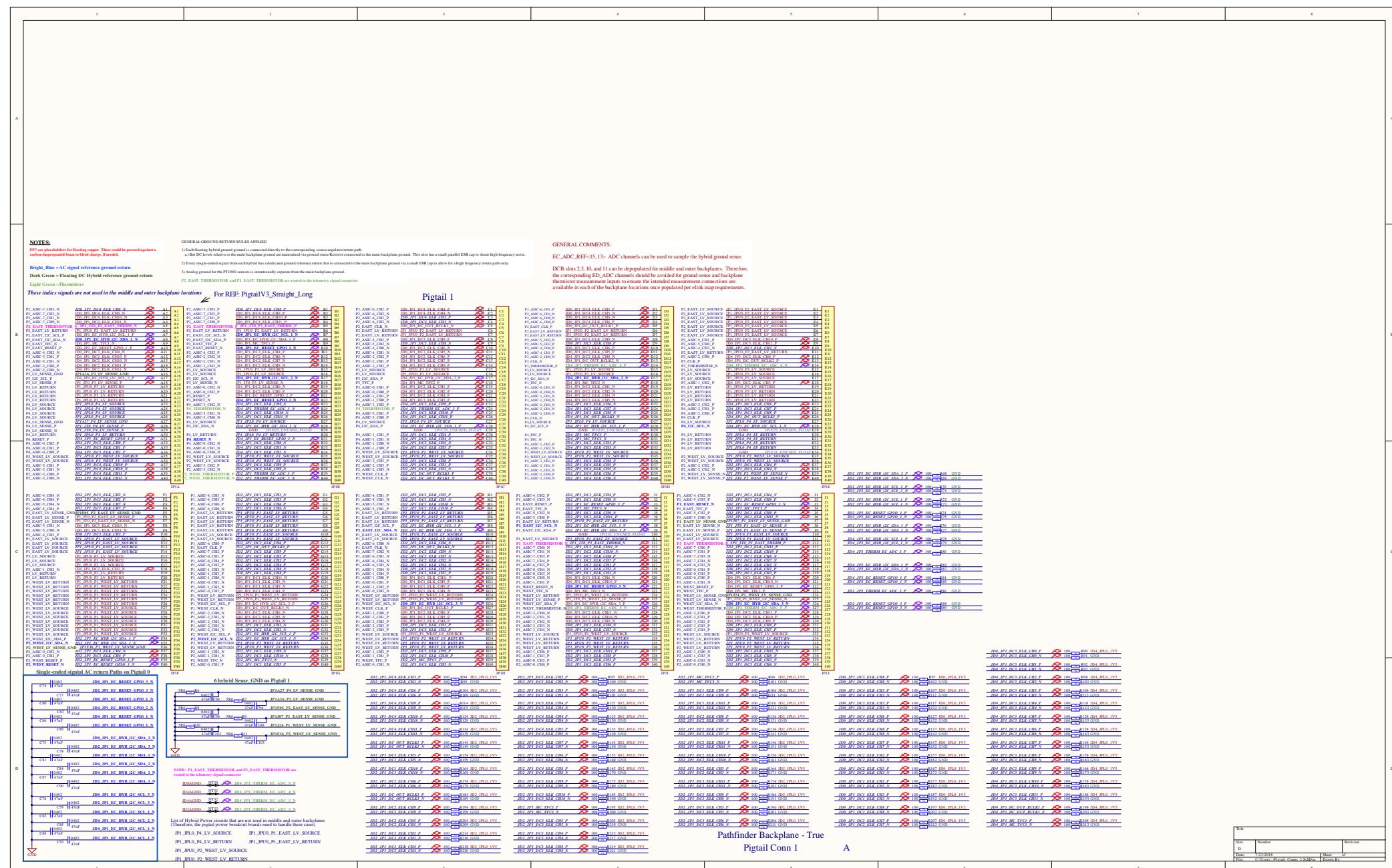
DCB slots 2,3,10, and 11 can be depopulated for middle and outer backplanes. Therefore, the corresponding ED_ADC channels should be avoided for ground sense and backplane thermistor measurement inputs to ensure the intended measurement connections are available in each of the backplane locations once populated per elink map requirements.

Pathfinder Backplane - True

Title	Part Number	Revision
Pigtail Conn 0		A

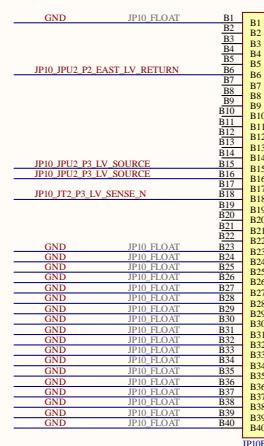
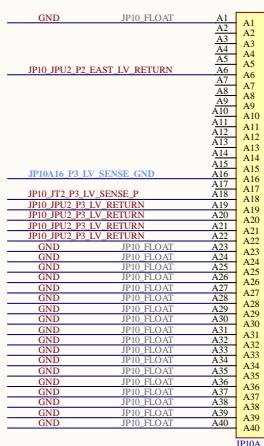
Date: 7/23/2018 Sheet of 1

File: C:\Users\jpepi\Comms\SchDoc Drawn By:

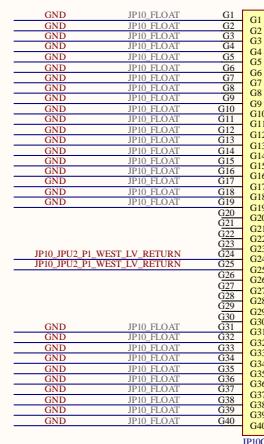
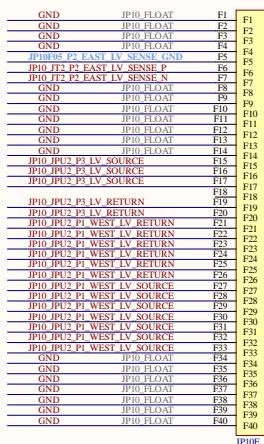


Pigtail 10

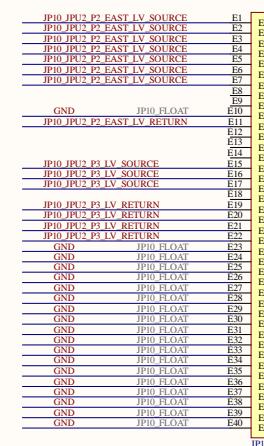
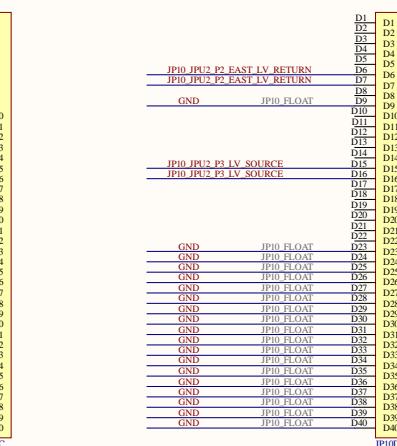
A



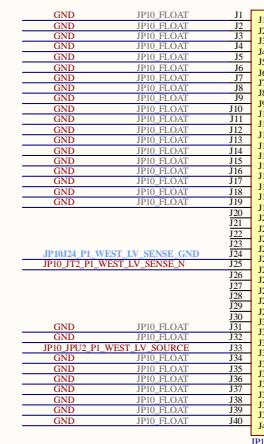
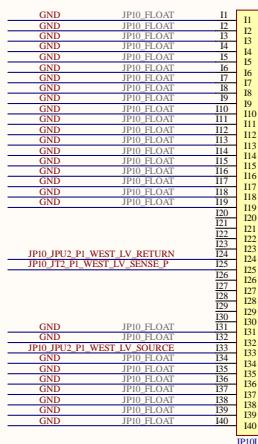
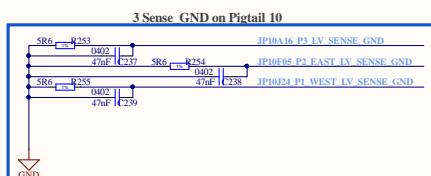
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C



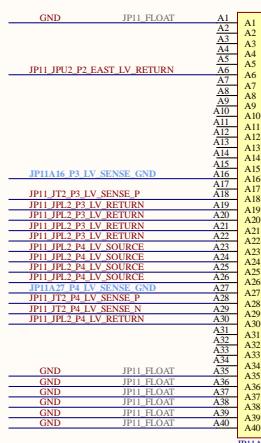
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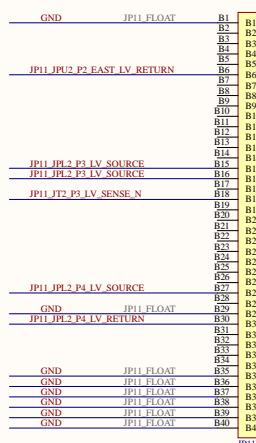
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Date: 7/23/2018	Sheet of	
File: C:\Users\...\Pigtail Conn 10.SchDoc	Drawn By:	

Pigtail 11

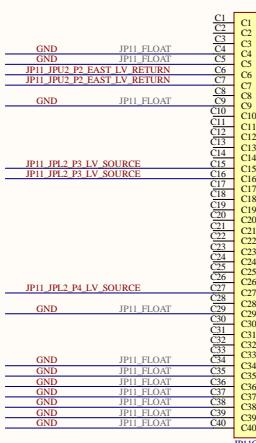
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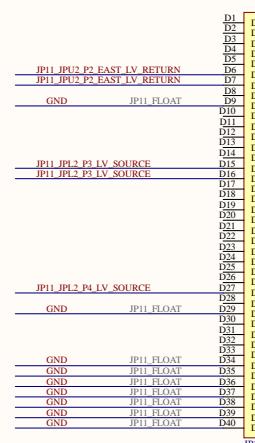
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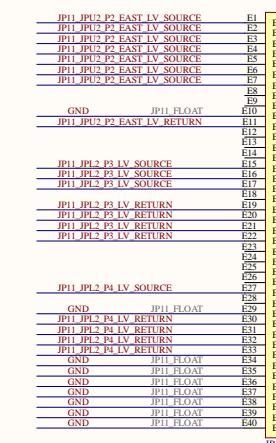
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JP11C

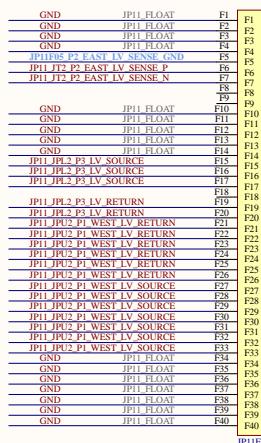


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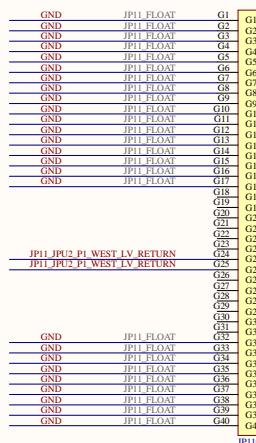


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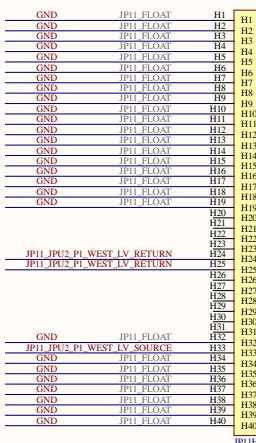
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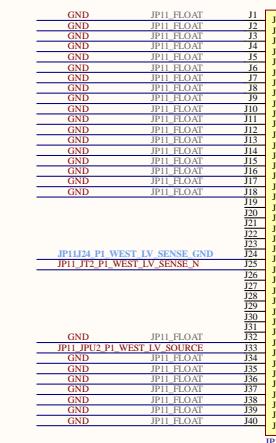
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JP11G

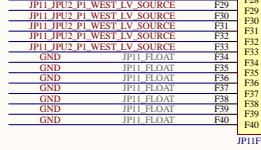


JP11H



JP11I

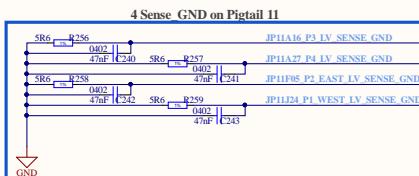
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JP11J

C

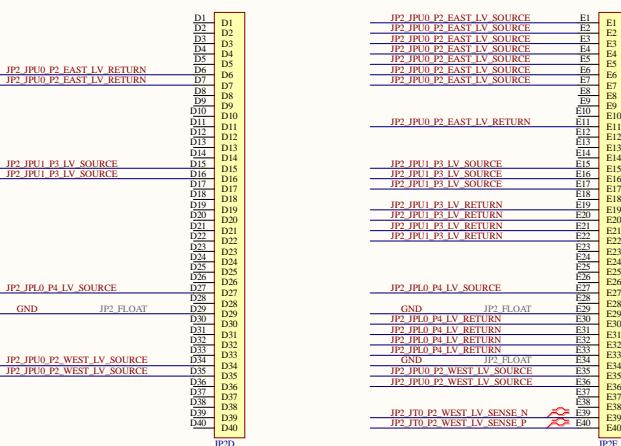
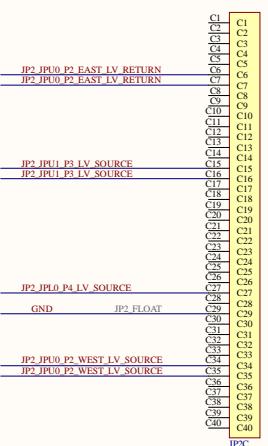
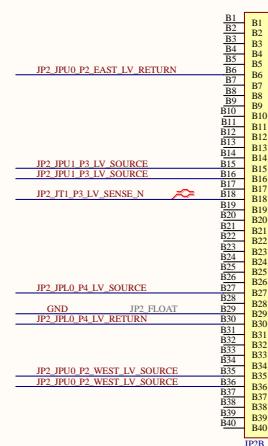
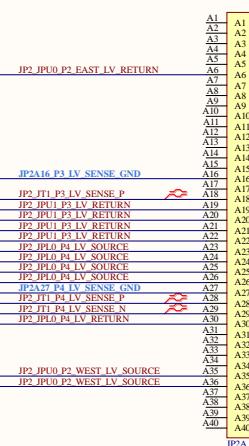
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Size	Number	Revision
c	Pigtail Conn 11	A
Date:	7/23/2018	Sheet of
File:	C:\Users\...\Pigtail Conn 11.SchDoc	Drawn By:

Pigtail 2

A



JP2A

JP2B

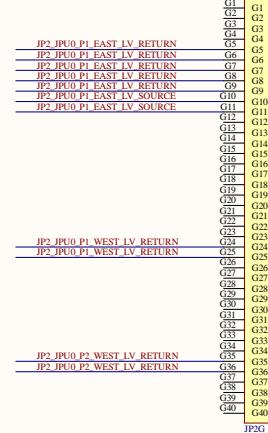
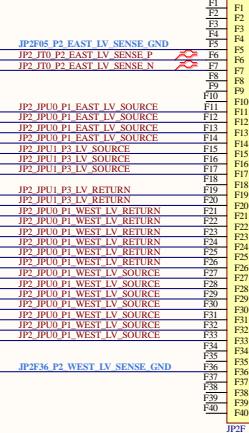
JP2C

JP2D

JP2E

A

B



JP2F

JP2G

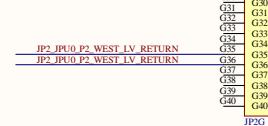
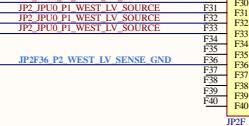
JP2H

JP2I

JP2J

B

C



JP2F

JP2G

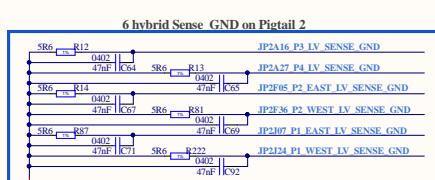
JP2H

JP2I

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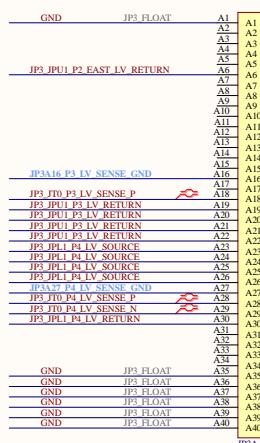
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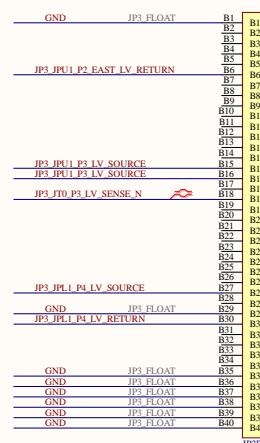
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Pigtail 3

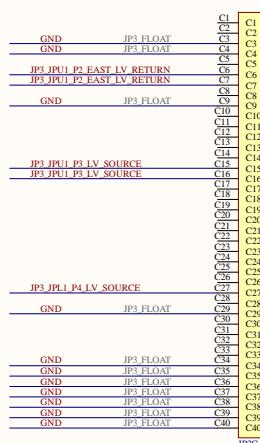
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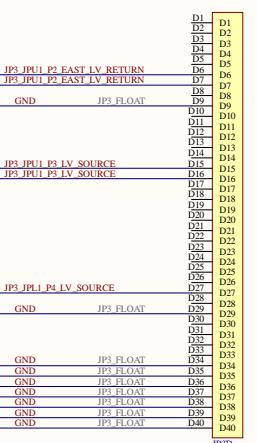
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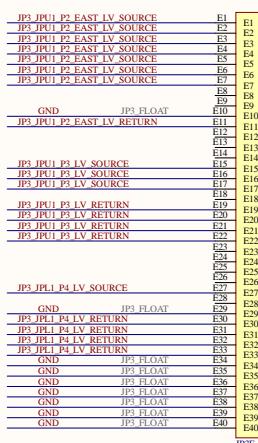
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JP3C

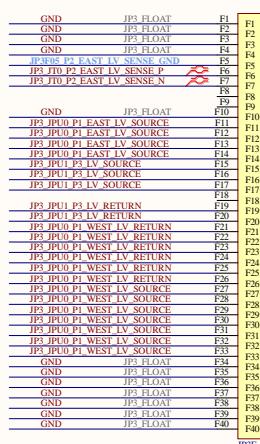


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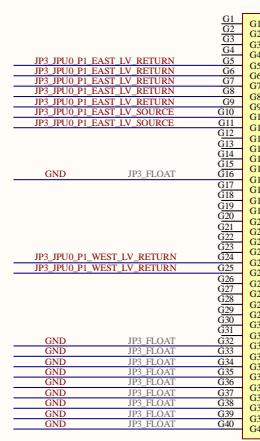


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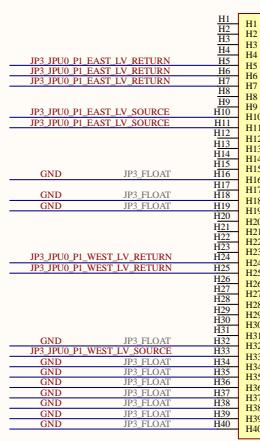
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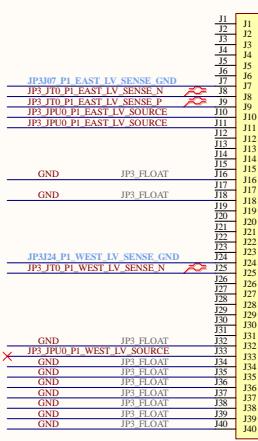
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JP3G

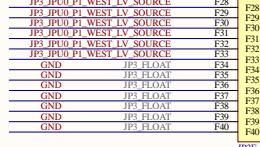


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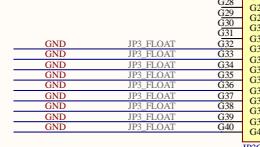


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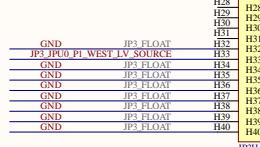
C



JP3J

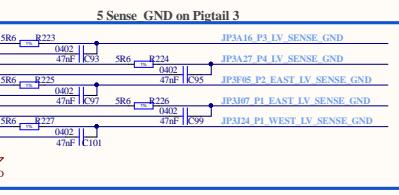


JP3K



JP3L

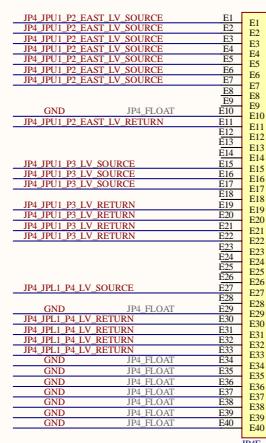
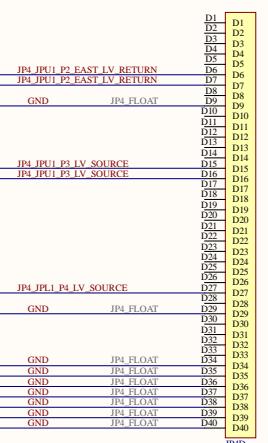
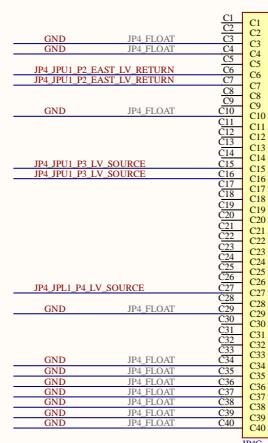
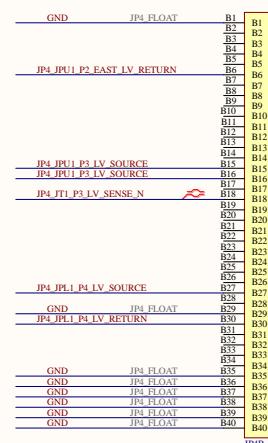
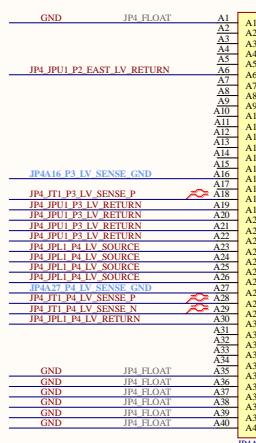
D



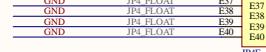
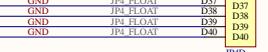
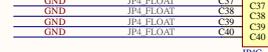
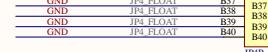
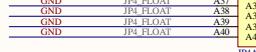
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Pigtail 4

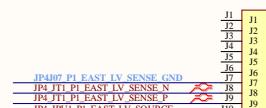
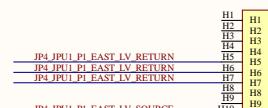
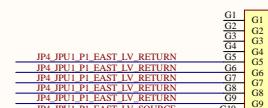
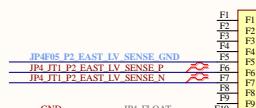
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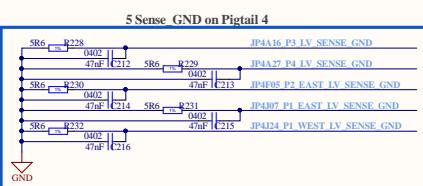
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C

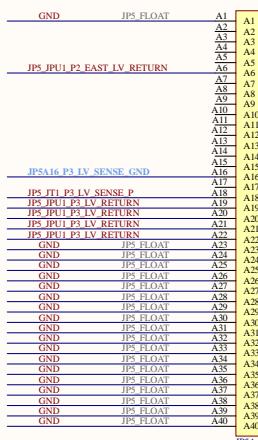


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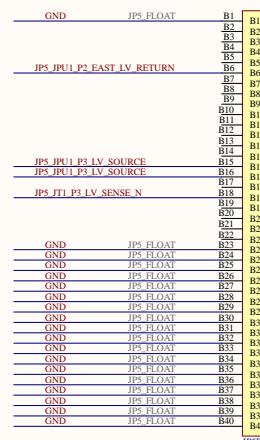


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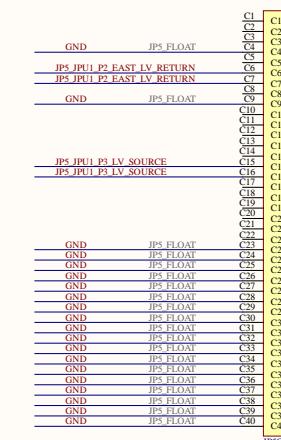
Pigtail 5



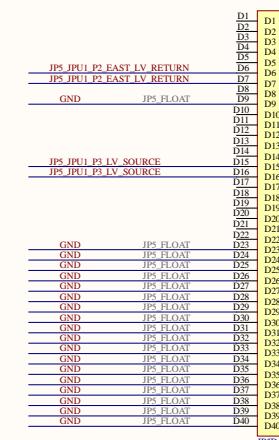
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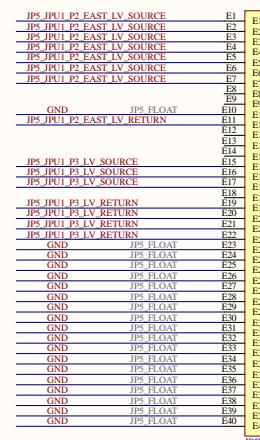
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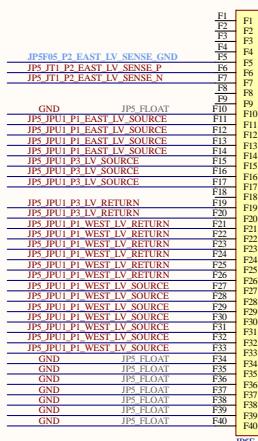
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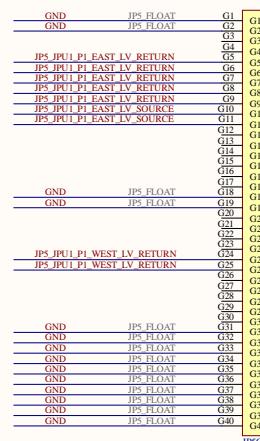
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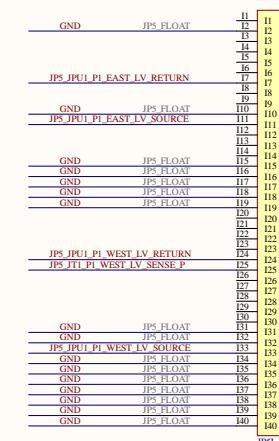
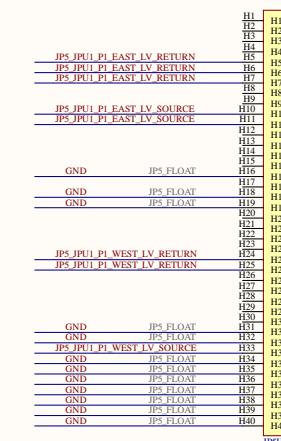
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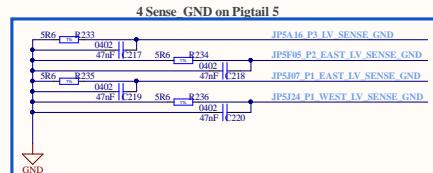
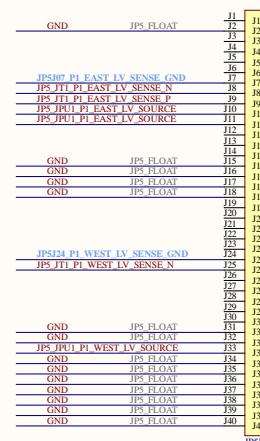
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G4



1

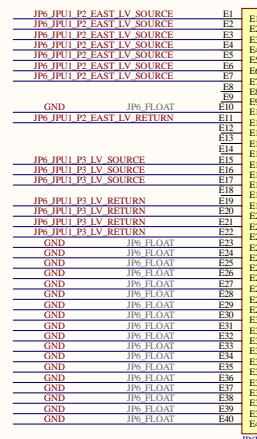
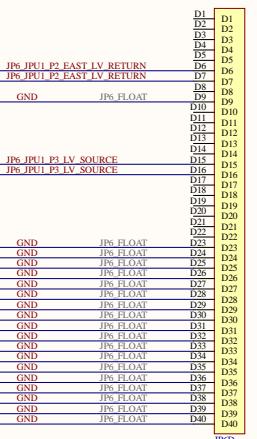
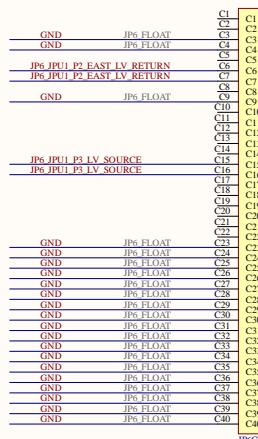
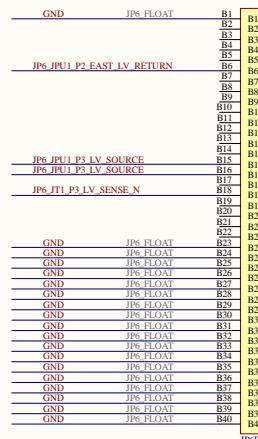
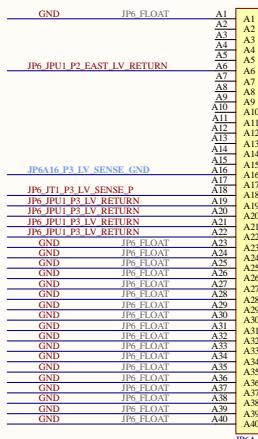


4 Sense_GND on Pigtail 5

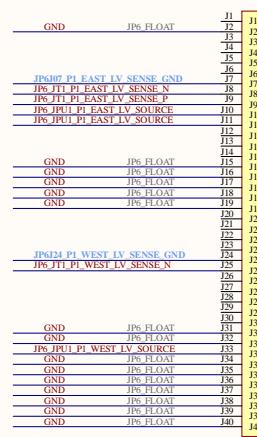
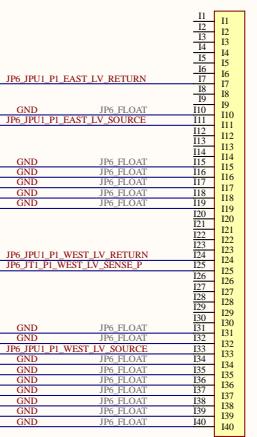
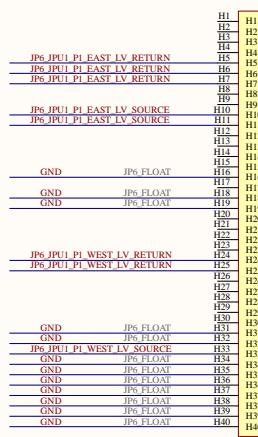
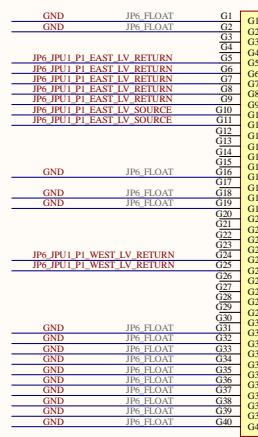
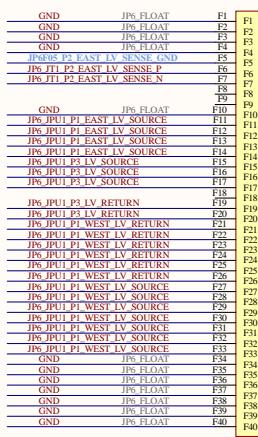
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Pigtail 6

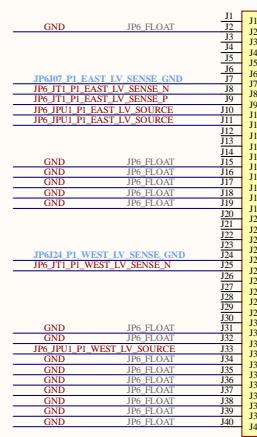
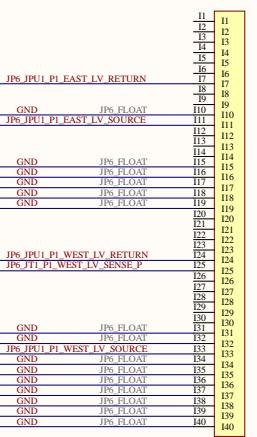
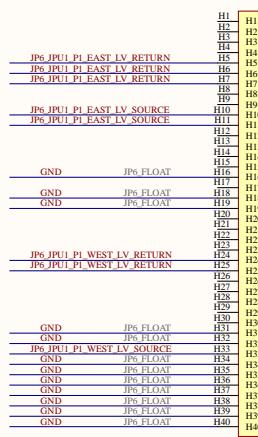
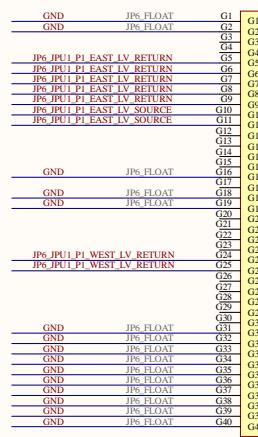
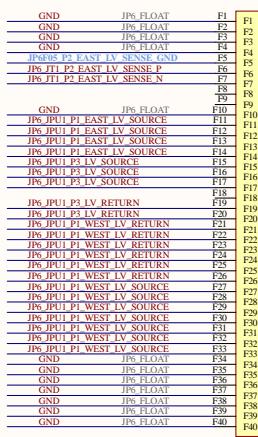
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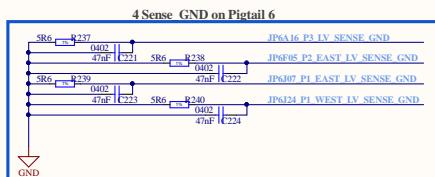
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C

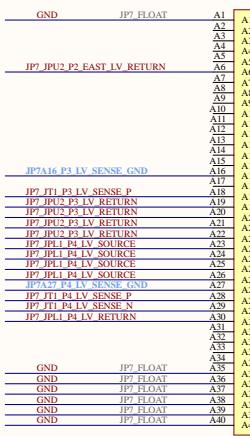


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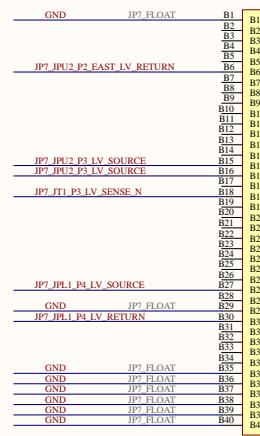


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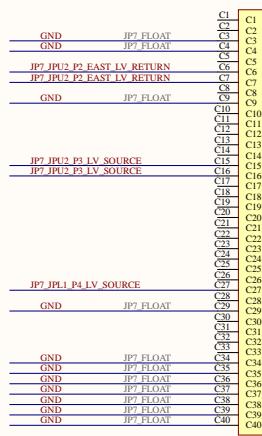
Pigtail 7



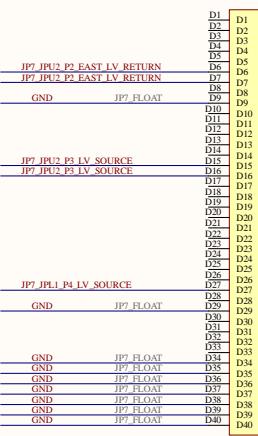
JP7A



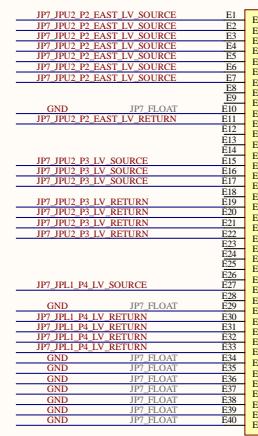
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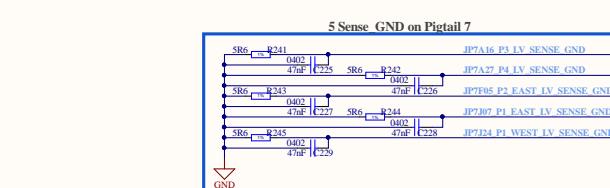
JP7C



JP7D



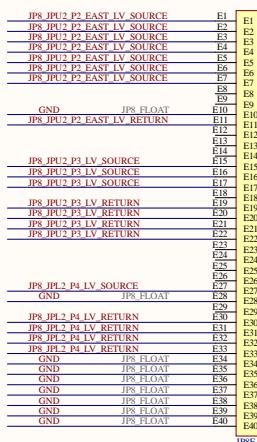
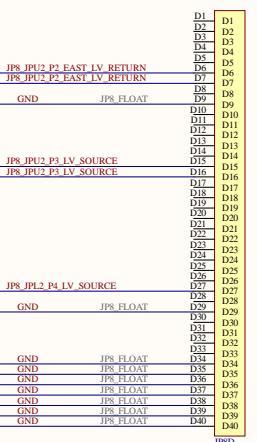
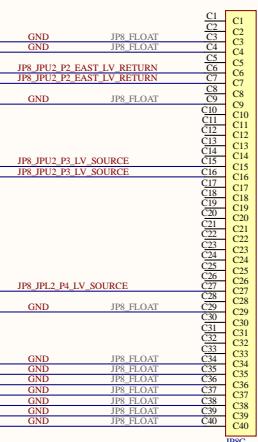
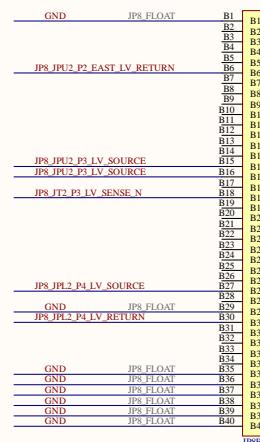
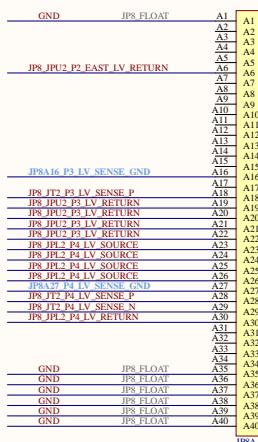
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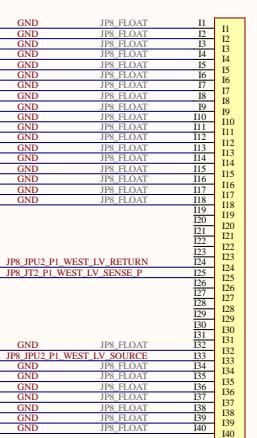
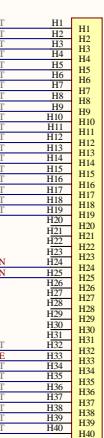
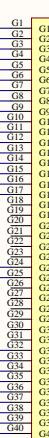
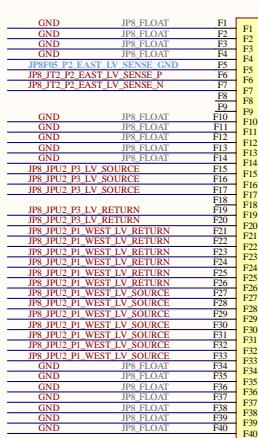
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Pigtail 8

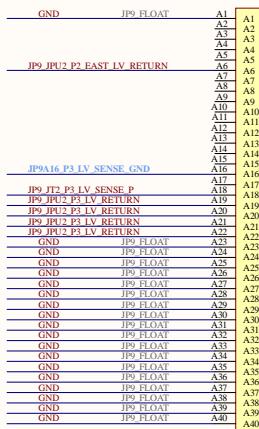
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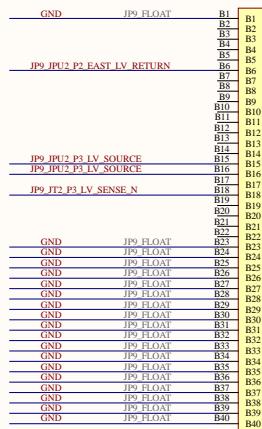
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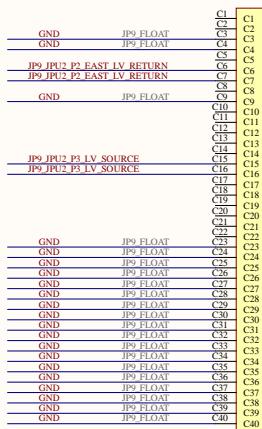
Pigtail 9



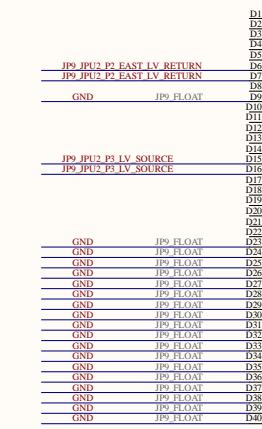
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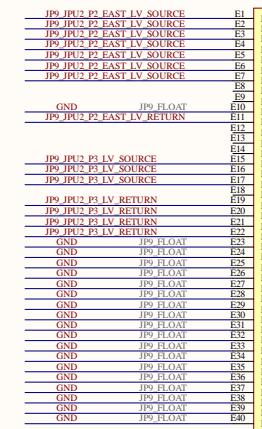
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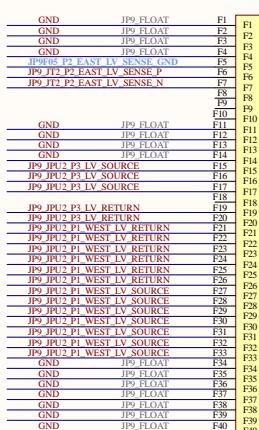
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JP9D

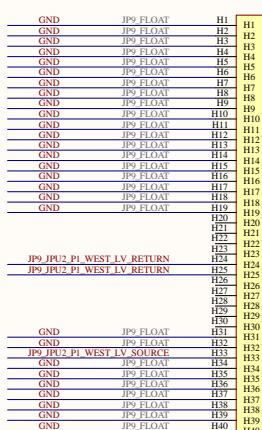


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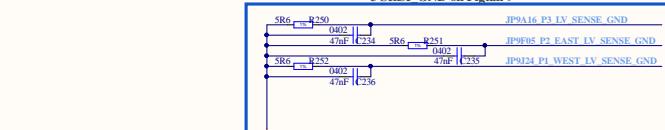


JP9F

JP9G



JP9H



GND

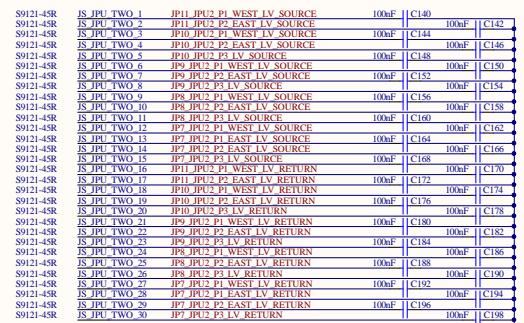


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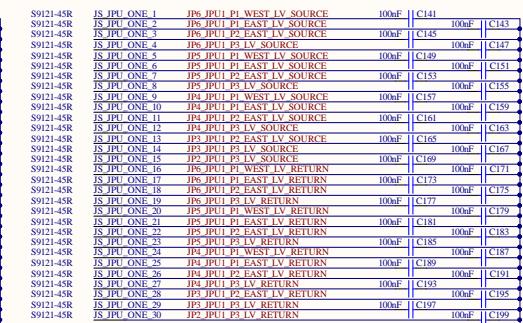
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Date:	7/23/2018	Sheet of
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UPPER Power Conns--(All dedicated to pigtail power routes)
JPUx connectors located directly on the Pigtail Power Breakout Board

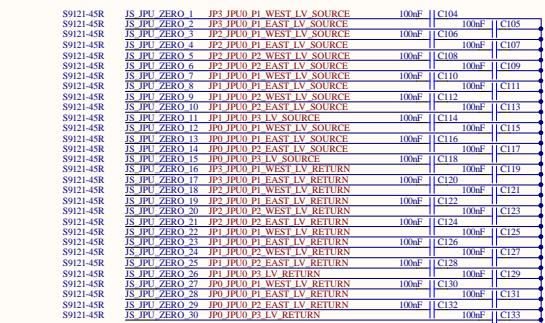
Fed by JPU2 on the Pigtail Power Breakout Brd



Fed by JPU1 on the Pigtail Power Breakout Brd



Fed by JPU0 on the Pigtail Power Breakout Brd

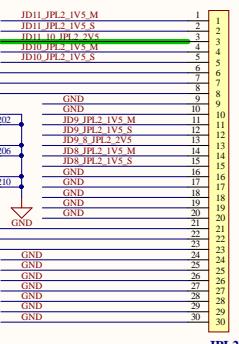


NOTE: ALL 3 of these contact / pigtail assignment grouping needed to be identical so one PCB design can be used in 3 places on the rear of the backplane

LOWER Power Conns--(All DCB slot power routes and a few pigtail power routes)

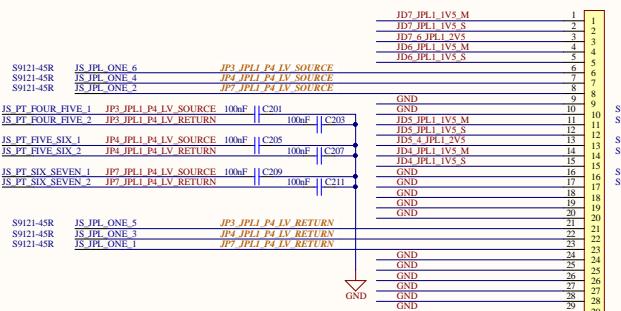
The JS_JPL_TWO_? contacts are located by the JPL2 connector.

The JS_PT_EIGHT_NINE_? contacts are located between pigtail conn P7A & P7B.
 The JS_PT_NINE_TEN_? contacts are located between pigtail conn P7C & P7D.
 The JS_PT_TEN_ELEVEN_? contacts are located between pigtail conn P7E & P7F.



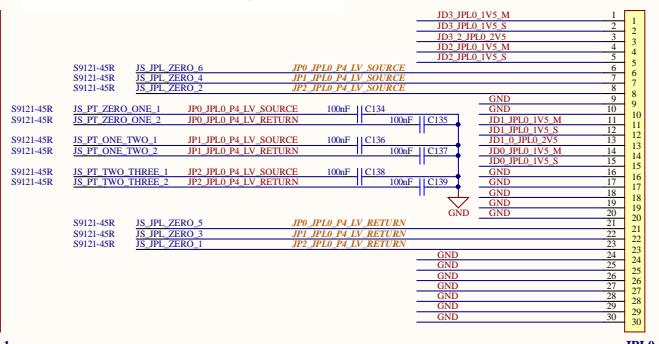
The JS_JPL_ONE_? contacts are located by the JPL1 connector.

The JS_PT_FOUR_FIVE_? contacts are located between pigtail conn P7A & P7B.
 The JS_PT_FIVE_SIX_? contacts are located between pigtail conn P7C & P7D.
 The JS_PT_SEVEN_EIGHT_? contacts are located between pigtail conn P7E & P7F.



The JS_JPL_ZERO_? contacts are located by the JPL0 connector.

The JS_PT_ZERO_ONE_? contacts are located between pigtail conn P7D & P7I.
 The JS_PT_ONE_TWO_? contacts are located between pigtail conn P7E & P7F.
 The JS_PT_TWO_THREE_? contacts are located between pigtail conn P7G & P7H.



NOTE: The pigtail power lines on JPL2, JPL1, and JPL0 get routed via the individual JS contacts to the PIGTAIL_POWER_Breakout_PCB

A

A

B

B

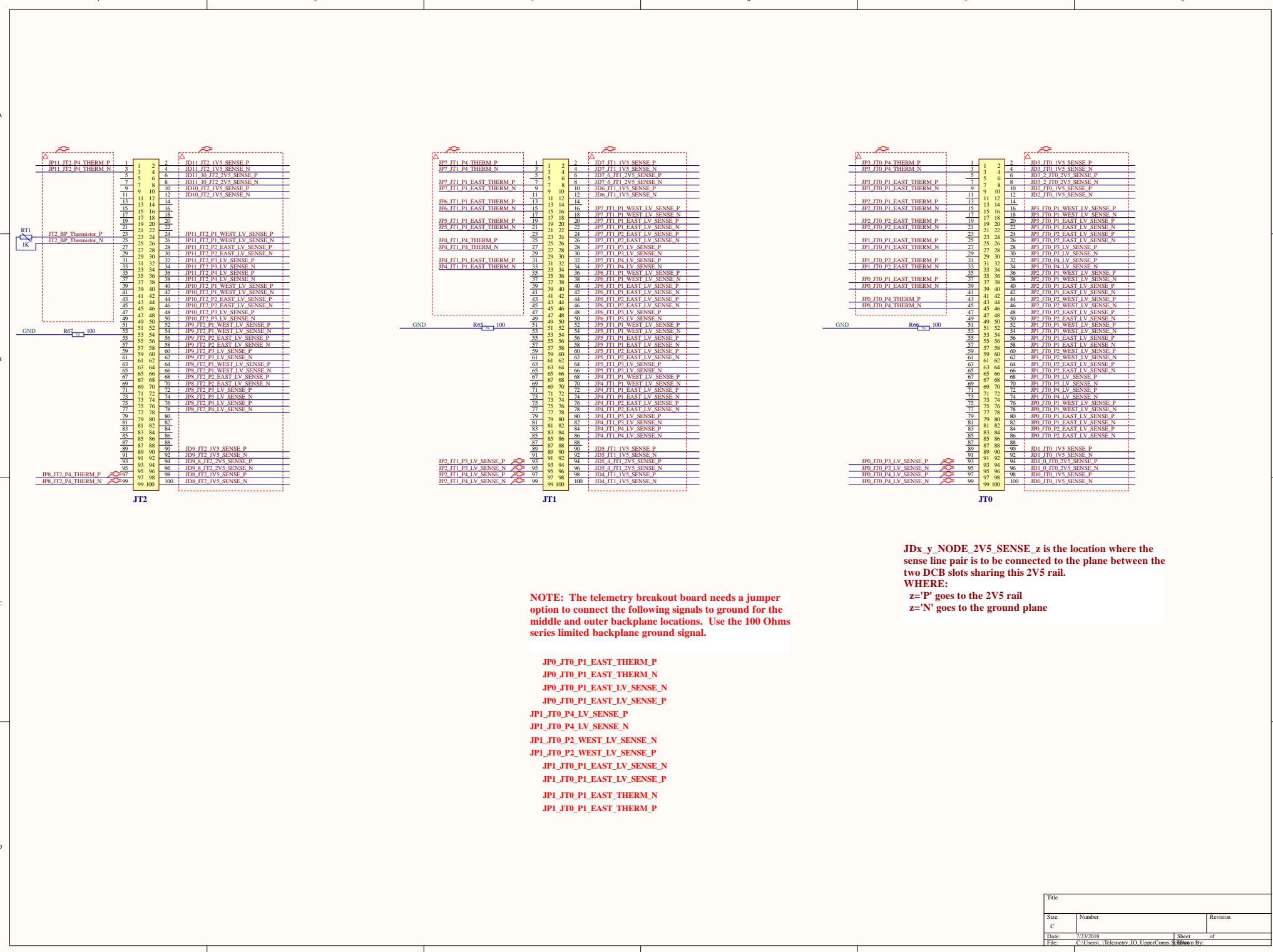
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C

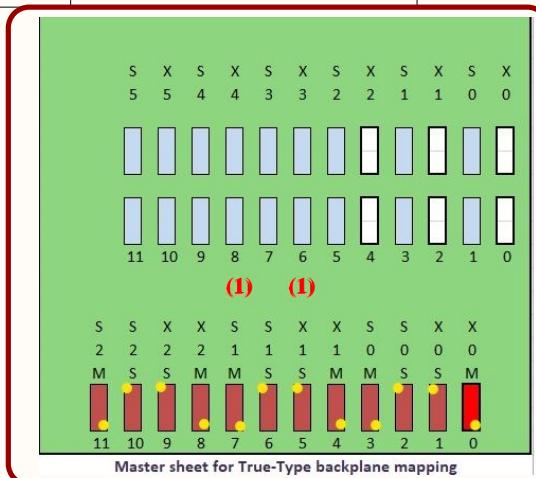
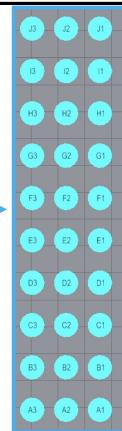
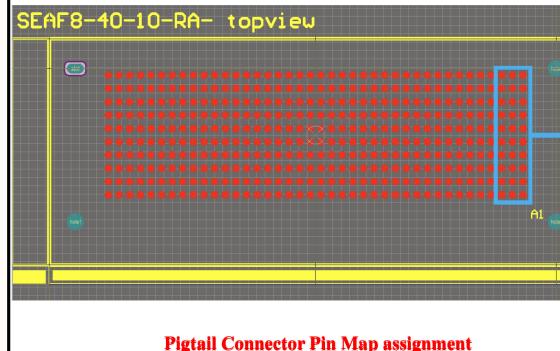
D

D

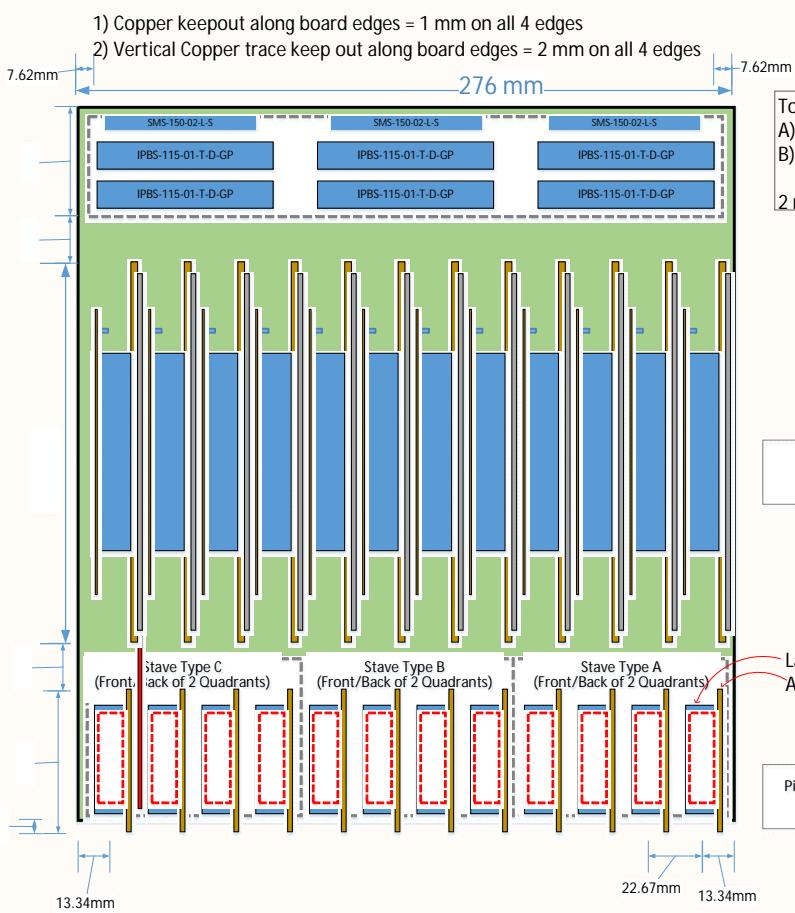
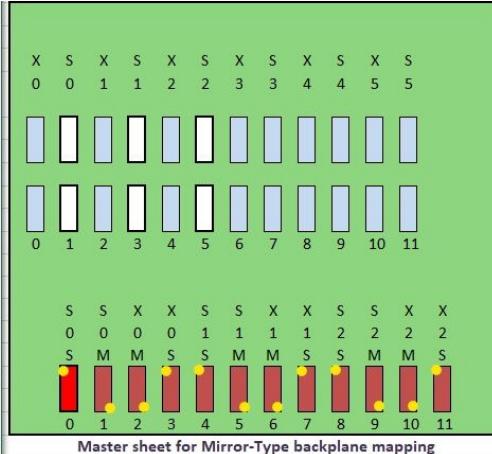
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Date:	7/23/2018	Sheet of
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	25	25
	26	26
	27	27
	28	28
	29	29
	30	30



SEAF8 footprint (to be matched by SEAM8)



(1) DCB Full Test via COMETs = Slots 6 and 8



Connector Types and Locations

- 1) Can via break out be added to the PCB lib footprint???
- 2) The final backplane has to route some of the thermistors for CO2 system.
- 3) upper conn in left diagram needs to be 2x50 each!!!!
- 4) MAKE the DIFF PAIR Track width UNIQUE to facilitate find and replace
- 5) NEED PLACE TO ATTACH GROUND BRAIDS to the breakout boards (grounds to be via breakout board conn)
- 6) Place a platinum thermistor on each backplane
- 7) Can a carbon impregnated foam be used to address floating traces by providing a charge bleed path between floating traces tied to vias and ground?
- 8) The plug-in power connns may need to short the power hybrid groups together since there are different configurations for each backplane location! ALT solution is to have the bus-bars allow for this customer config.
- 9) ALL Pigtails are electrically identical!

PATHFinder Backplane: TRUE type

Title		
Size	Number	Revision
C		
Date: 7/23/2018 File: C:\Users\...\Top_Notes_Sheet1.SchDoc	Sheet of	Drawn By: