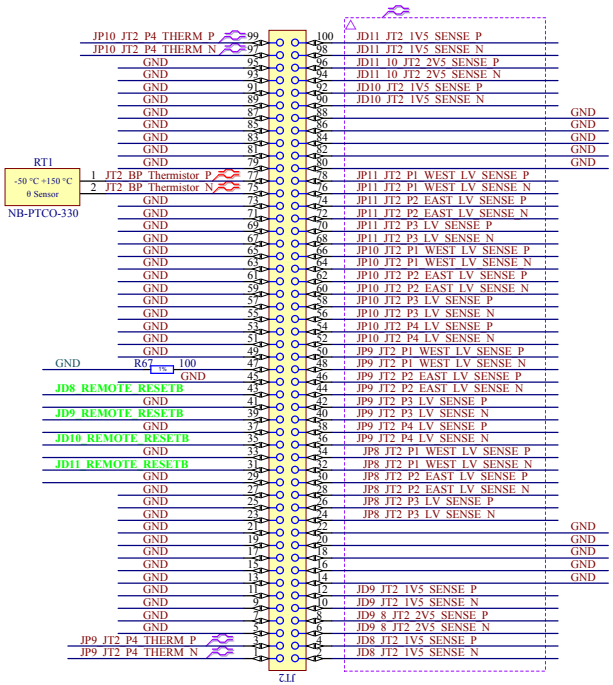
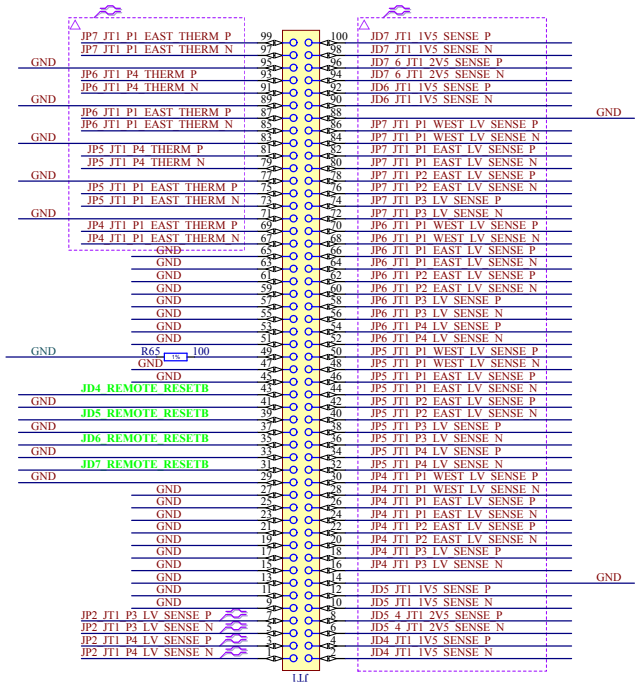
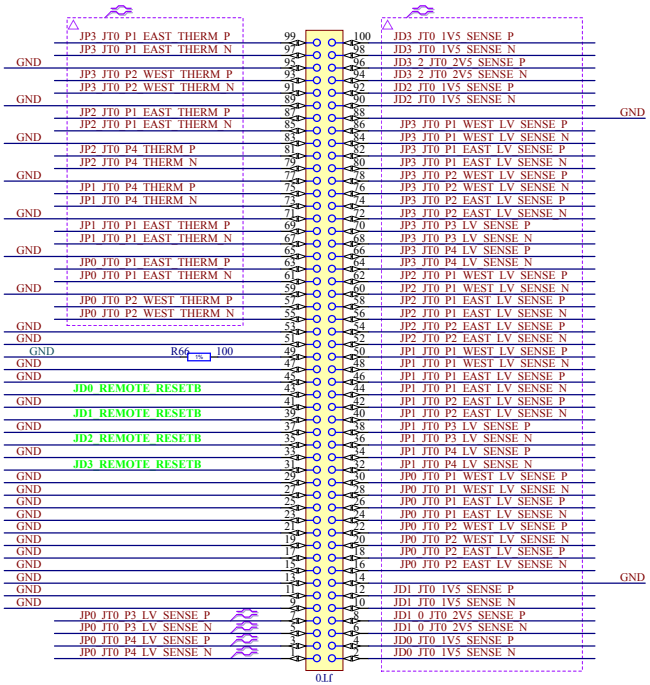






NOTE: The GND connected via the seies 100 Ohm can be used as a remote ground signal reference where needed.

JDx_y_NODE_2V5_SENSE_z is the location where the sense line pair is to be connected to the plane between the two DCB slots sharing this 2V5 rail.
WHERE:
z='P' goes to the 2V5 rail
z='N' goes to the ground plane

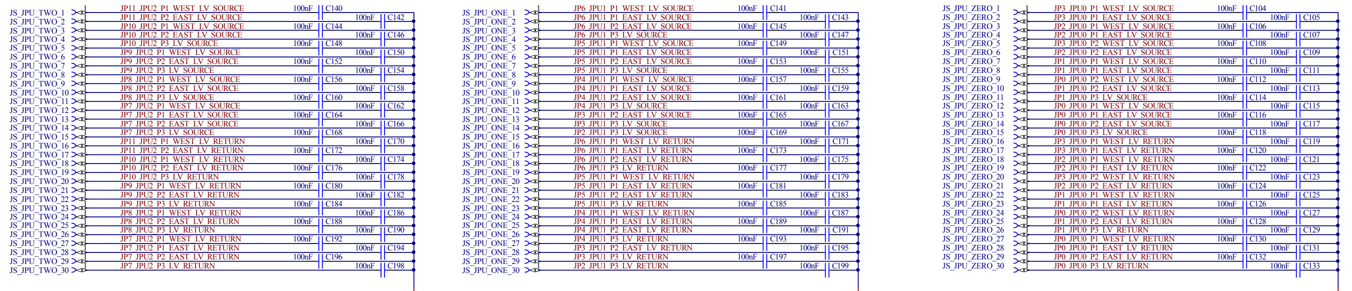
IMPORTANT NOTE: The "GND" pins MUST NOT EVER be connected to any remote ground nodes.

Project/Equipment -			
Document	Title Title2	Designer Designer Drawn by DrawnBy Check by - Last Mod. -	XX/XX/XXXX - 6/4/2019
TE/MPE		File Telemetry_IO_UpperConns.SchDoc	
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		Print Date 6/20/2019 7:52:36 AM	Sheet 2 of 21
	EDA-XXXXX-VX-X	Size A3	Rev -

UPPER Power Conns--(All dedicated to pigtail power routes)
JPUx connectors located directly on the Pigtail Power Breakout Board

NOTE: ALL 3 of these contact / pigtail assignment grouping needed to be identical so one PCB design can be used in 3 places on the rear of the backplane

Fed by JPU2 on the Pigtail Power Breakout Brd | Fed by JPU1 on the Pigtail Power Breakout Brd | Fed by JPU0 on the Pigtail Power Breakout Brd

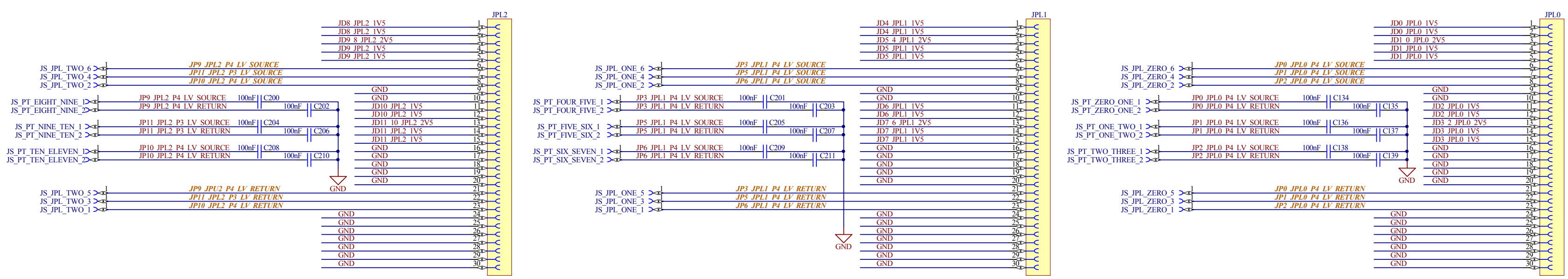


NOTE: These 100 Ohm bleed resistors are only installed in cases where the copper tracks are NOT being used (ie floating)

EACH Power Group receives SOURCE power from a single Maraton Channel.

The Maraton Channel is indirectly connected to system power ground via the ground sense resistor connections (ie one per 4-ASICs)

LOWER Power Conns--(All DCB slot power routes and a few pigtal power routes)



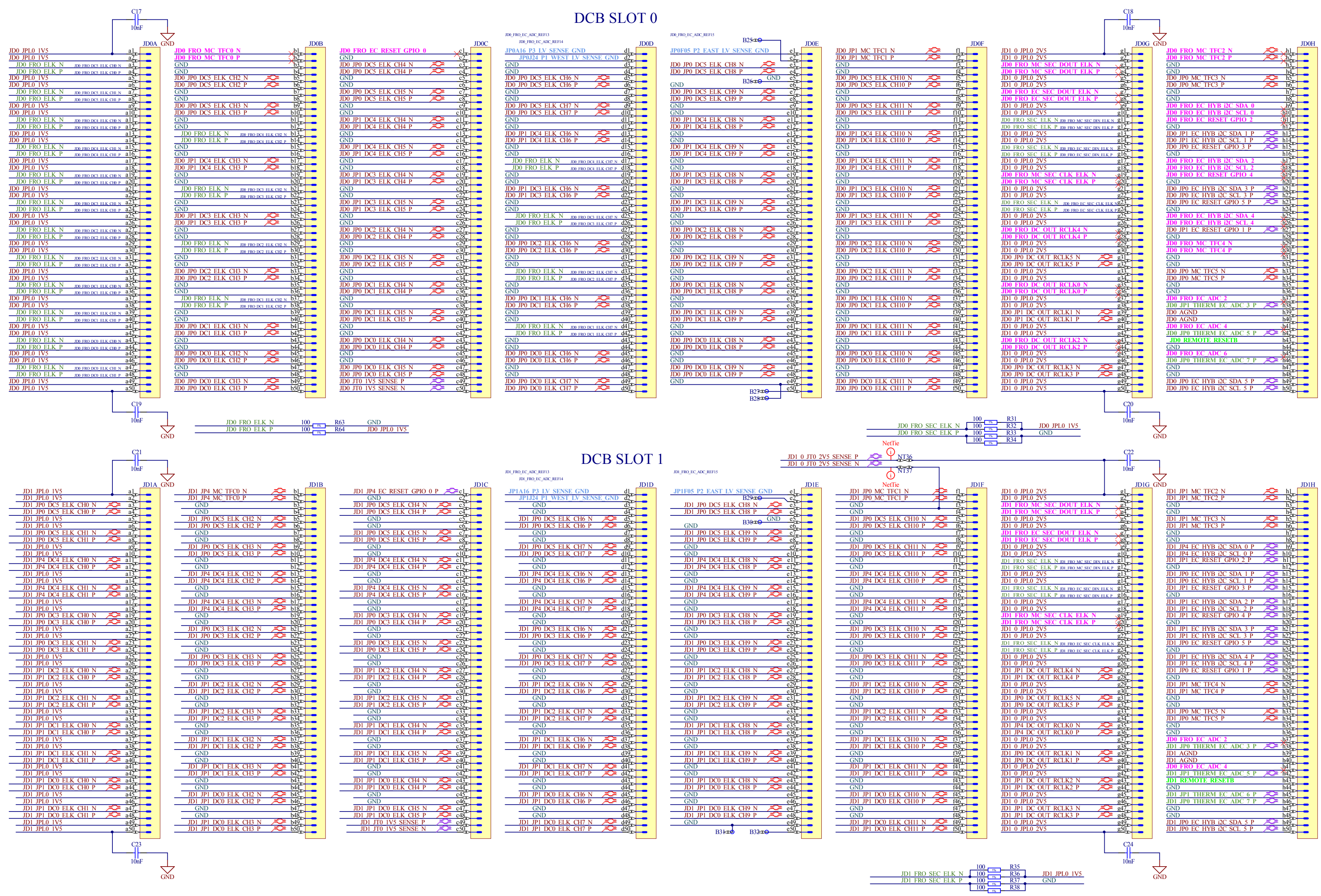
NOTE: (1) The pigtail power lines on JPL2, JPL1, and JPL0 get routed via the individual JS contacts to the PIGTAIL_POWER_Breakout_PCB.

(2) Each DCB slot uses 1 master + 1 slave channel. Both connector pins are labeled '_1V5. Therefore, one is for the Master cable and the second is for the slave cable.

(3) The power group 'returns' being joined together also prevents any unused pigtial and Stave flex cable tracks from being left floating.

(4) The power group 'Source' lines in depopulated 'beta' and 'gamma' BP positions are connected via resistors with designtors R_B? and R_G?, respectively, to the associated power group returns to avoid being left floating.

Project/Equipment	-	
Document	*Title* *- Power Bank Conns. -*	Designer: Designer; Drawn by: Drawnby XX/XX/XXXX; Check by: -; Last Mod.: - 6/4/2019; File: Power_Bank_Conns.SchDoc; Print Date: 6/20/2019 7:52:37 AM; Sheet 3 of 21
TE/MPE — European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	A2 -



Project/Equipment PEPI

Document

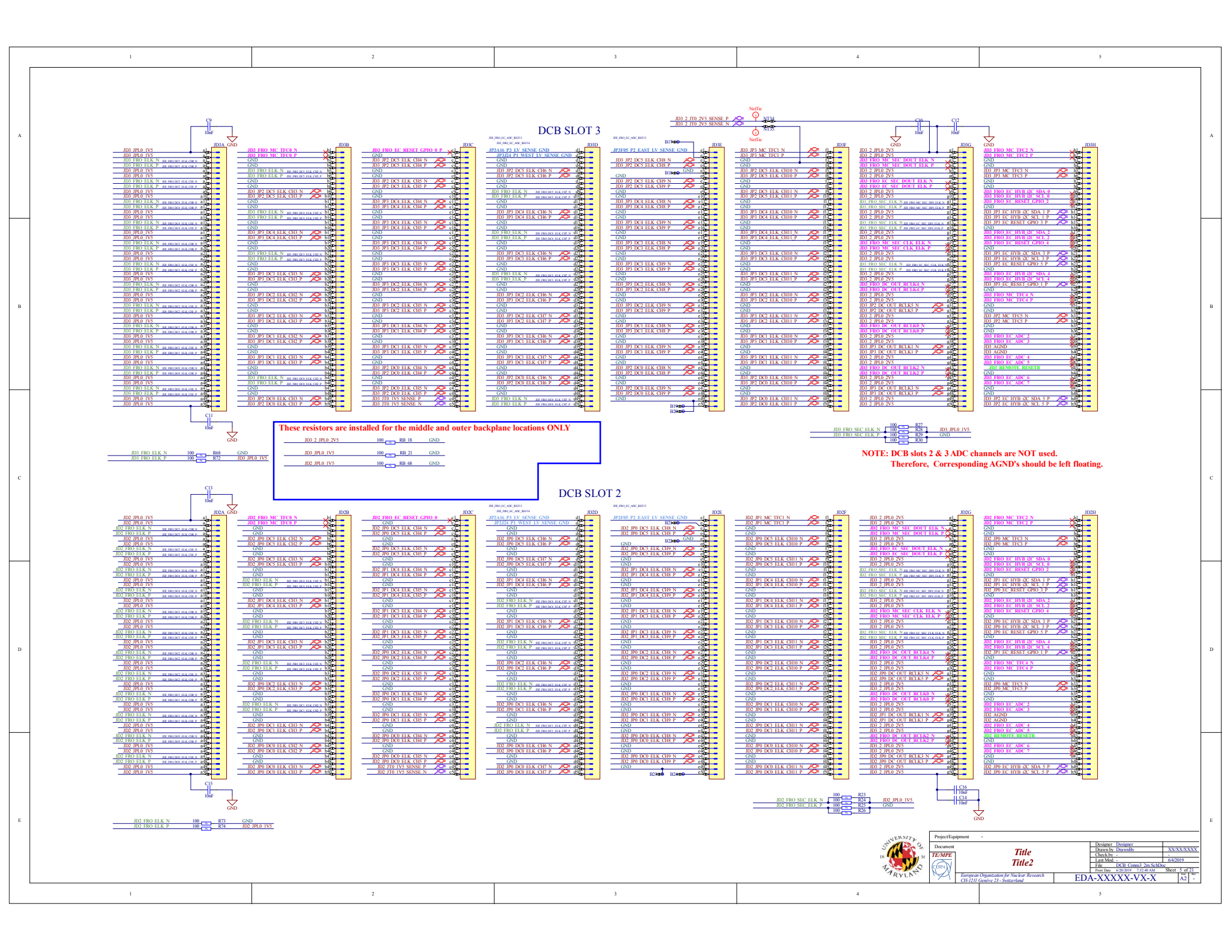
TE/MPE

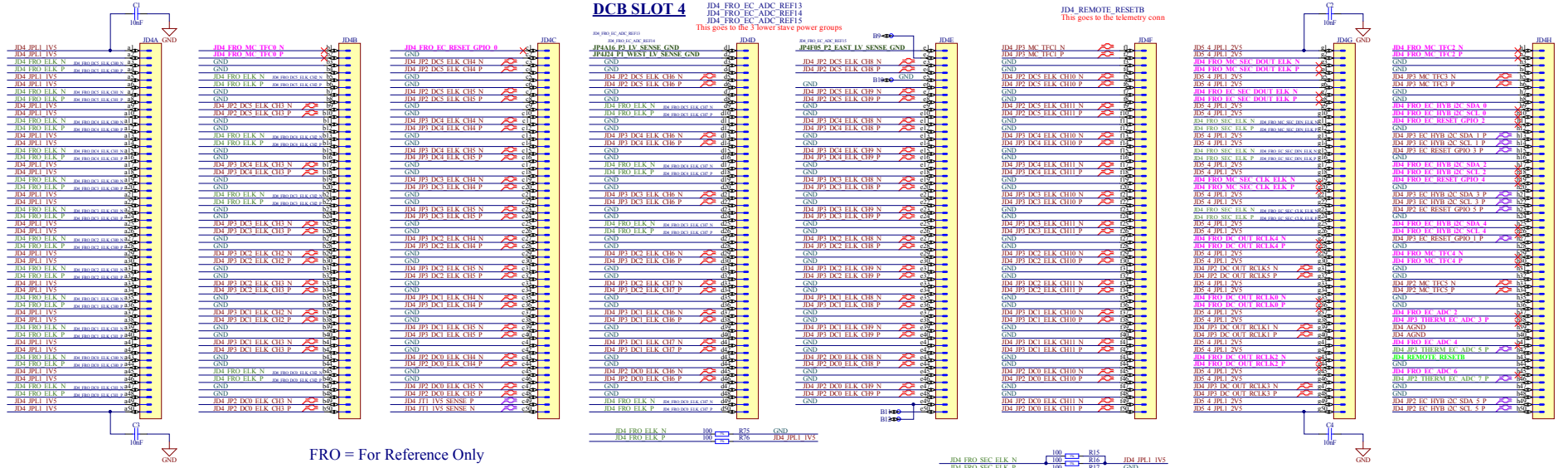
PEPI Backplane Mirror
DCB Slot Connector 0 & 1

European Organization for Nuclear Research
CH-1211 Genève 23 - Switzerland

Designer	M. Franco Sevilla	
Drawn by	M. Franco Sevilla	01/05/2019
Check.by	B. Civel	04/06/2019
Last Mod.	B. Civel	6/4/2019
File	DCB Conns1 0m.SchDoc	
Print Date	6/20/2019 7:52:38 AM	Sheet 4 of 21

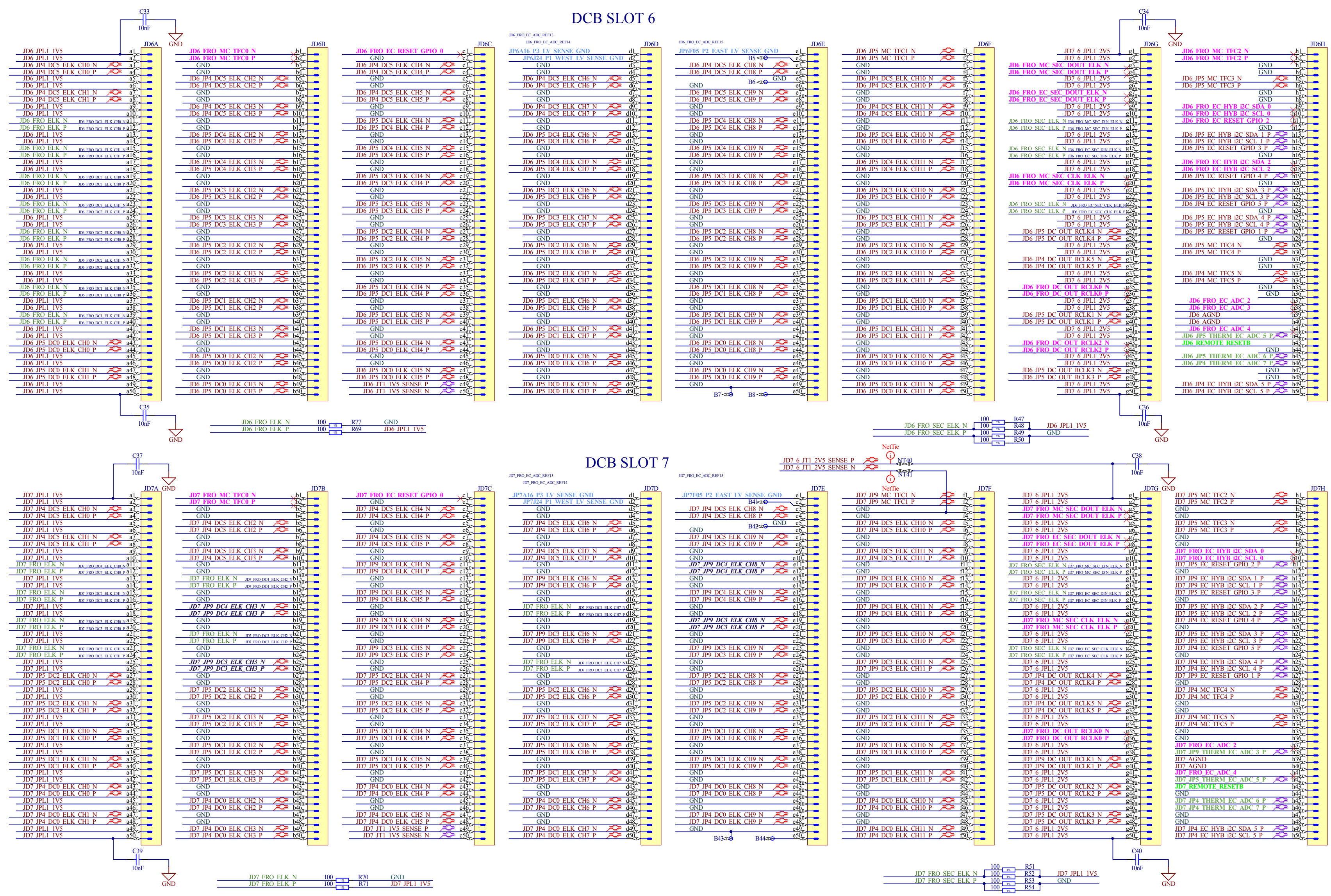
EDA-04066-V1-0 Size A2 Rev -


DCB SLOT 3
DCB SLOT 2
These resistors are installed for the middle and outer backplane locations ONLY
NOTE: DCB slots 2 & 3 ADC channels are NOT used.
Therefore, Corresponding AGND's should be left floating.
JD3A
JD3B
JD3C
JD3D
JD3E
JD3F
JD3G
JD3H
JD2A
JD2B
JD2C
JD2D
JD2E
JD2F
JD2G
JD2H
Project/Equipment -
Document
Title
Title2
TE/MPE
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland
Designer Designer
Drawn by Drawnby
Check by -
Last Mod. -
File DCB_Conn3_2m.SchDoc
Print Date 6/20/2019 7:52:40 AM
Sheet 5 of 21
EDA-XXXXX-VX-X
A2
XX/XX/XXXX
6/4/2019



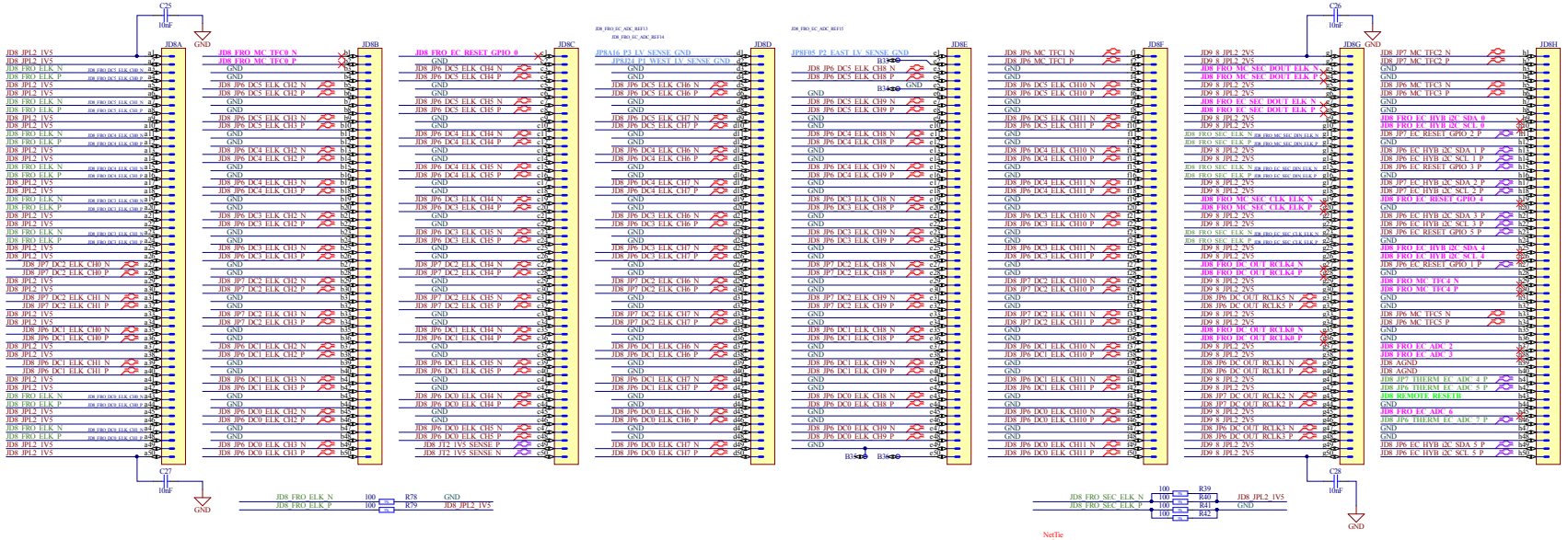
University of Maryland

Project/Equipment PEPI
Document
TE/MPE
CERN
PEPI Backplane Mirror
DCB Slot Connector 4 & 5
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland
Designer M. Franco Sevilla
Drawn by M. Franco Sevilla 01/05/2019
Check by B. Civel 04/06/2019
Last Mod. B. Civel 6/4/2019
File: DCB_Conns5_4m.SchDoc
Print Date 6/20/2019 7:52:43 AM Sheet 6 of 21
EDA-04066-V1-0
Size A2 Rev -

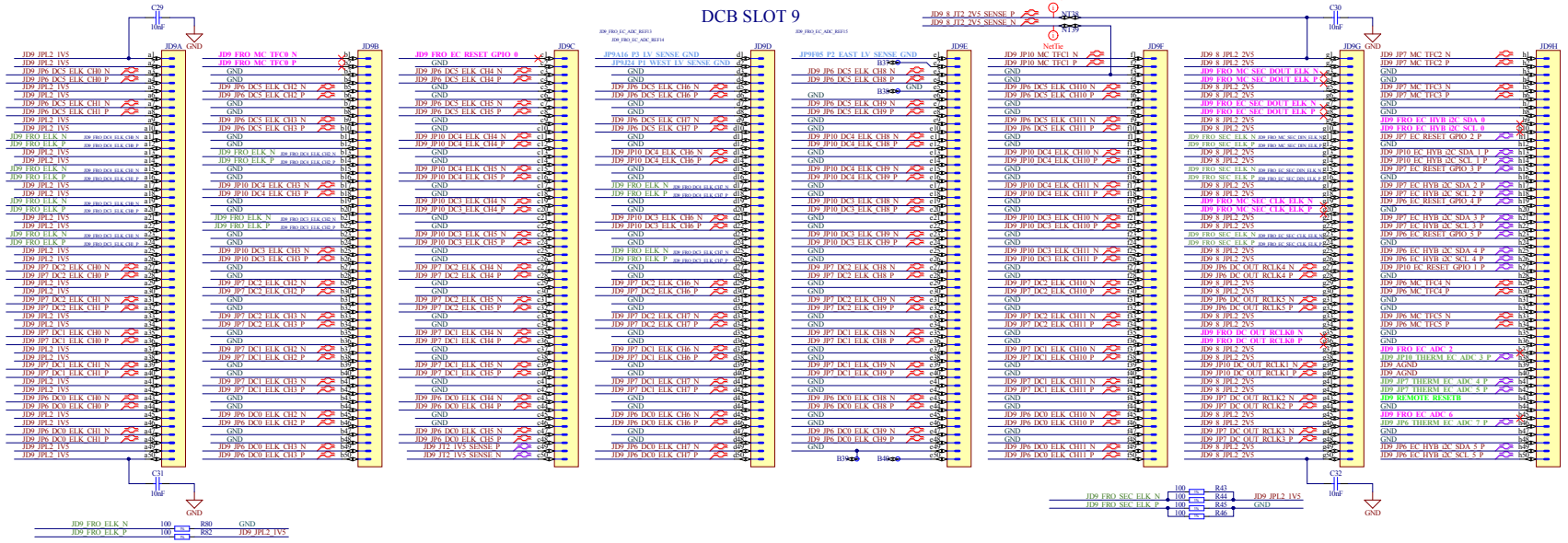


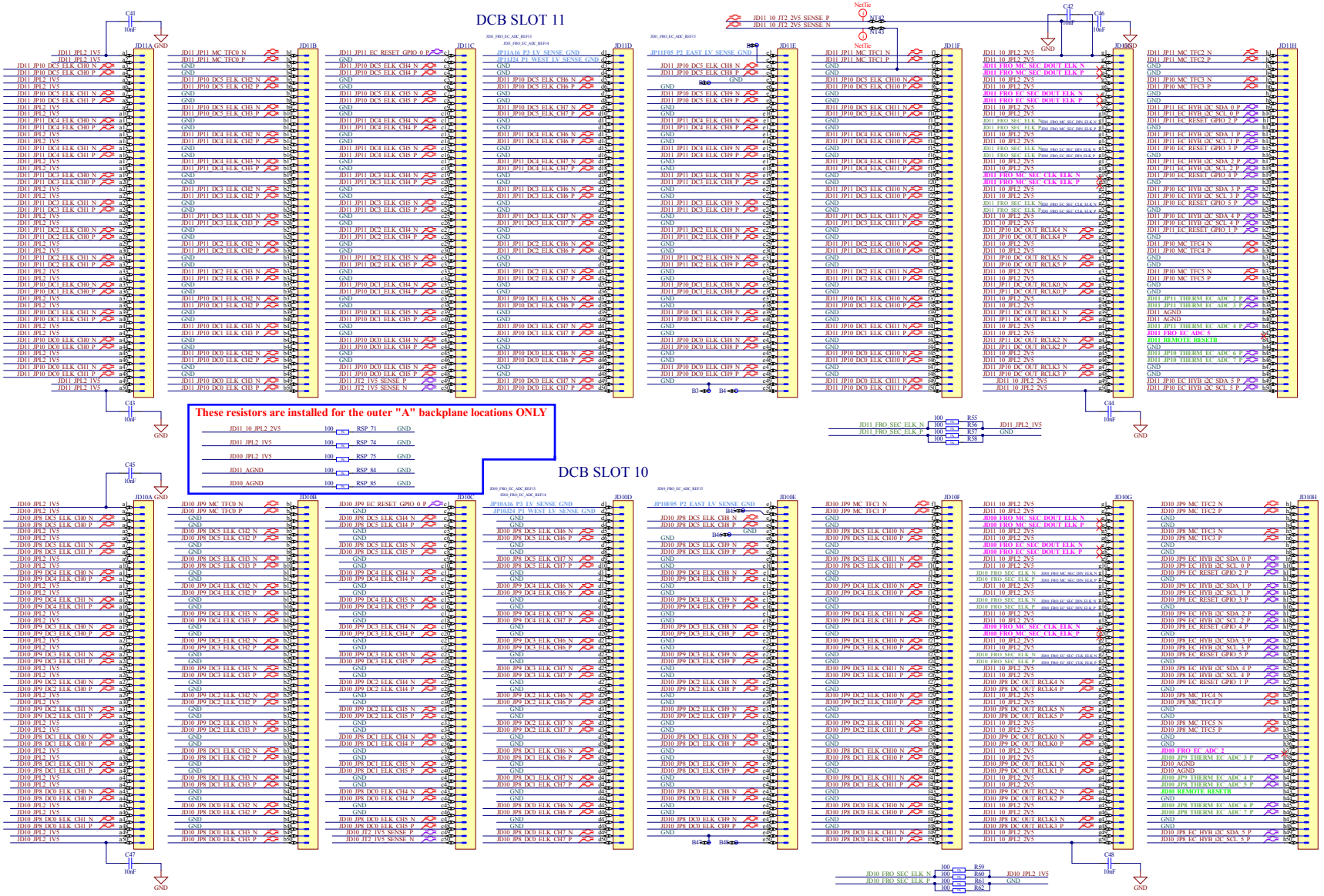
Project/Equipment	-		
Document	Title Title2	Designer	Designer
TE/MPE		Drawn by	DrawnBy XX/XX/XXXX
		Check.by	- -
		Last Mod.	- 6/4/2019
		File	DCB_Conns7_6_m.SchDoc
		Print Date	6/20/2019 7:52:45 AM Sheet 7 of 21
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland	EDA-XXXXX-VX-X	Size A2	Rev -

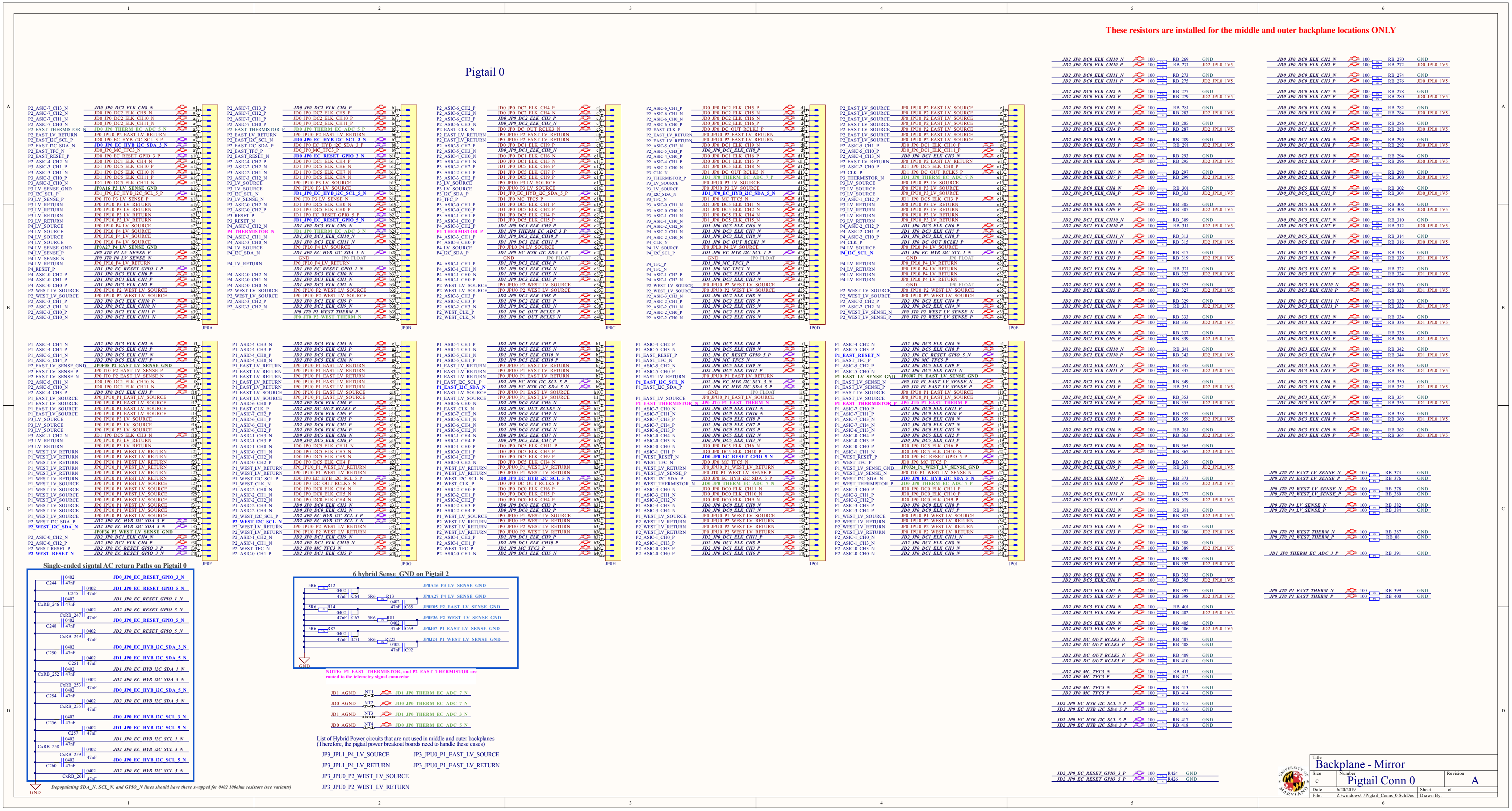
DCB SLOT 8



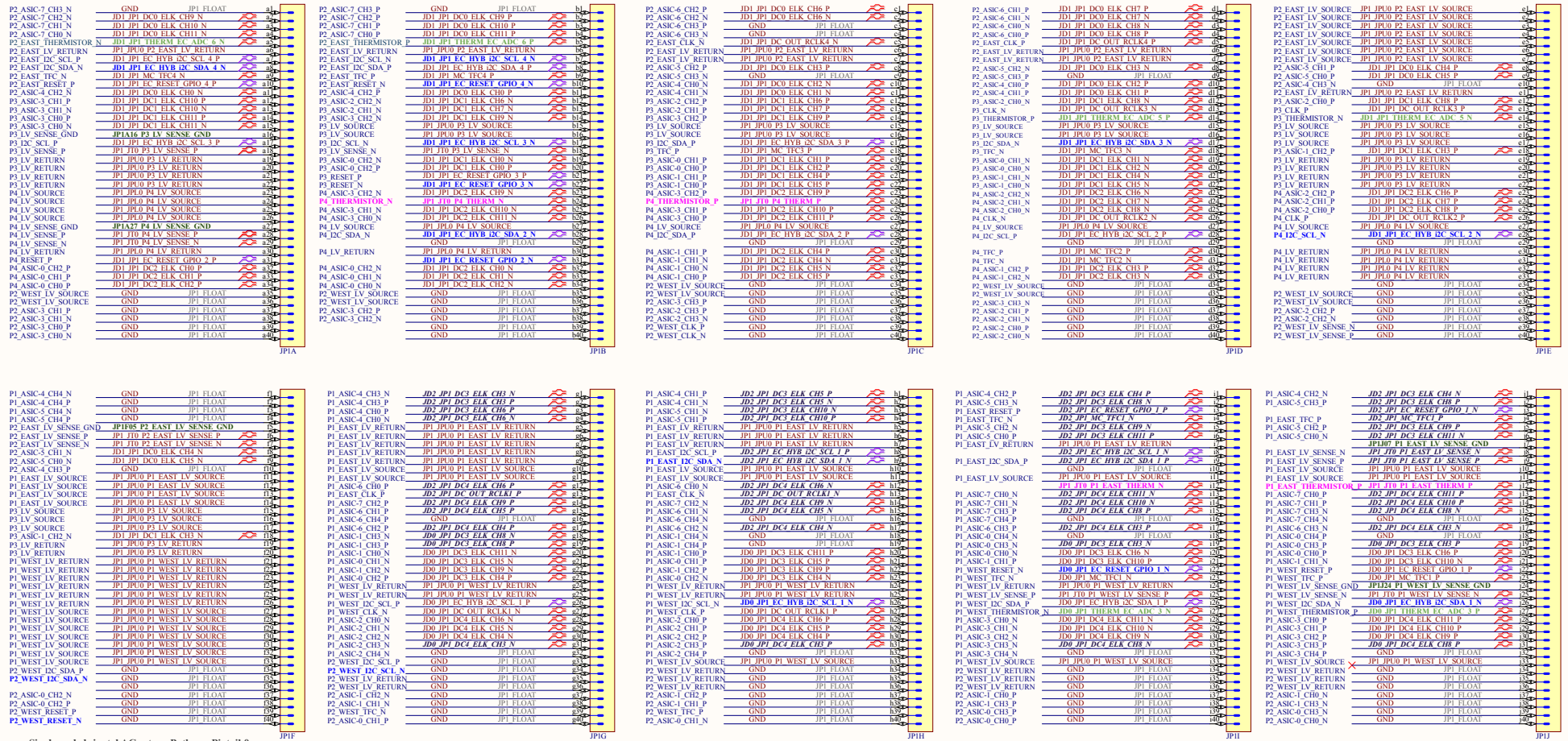
DCB SLOT 9



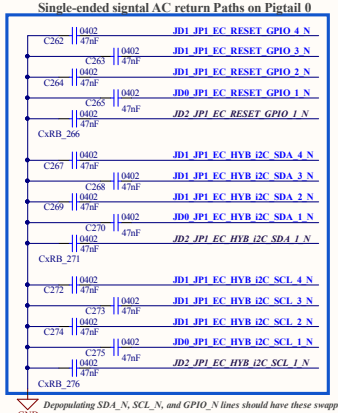

DCB SLOT 11
DCB SLOT 10
These resistors are installed for the outer "A" backplane locations ONLY
JD11_10_JPL2_2V5 100 RSP_71 GND
JD11_JPL2_1V5 100 RSP_74 GND
JD10_JPL2_1V5 100 RSP_75 GND
JD11_AGND 100 RSP_84 GND
JD10_AGND 100 RSP_85 GND
JD11A
JD11B
JD11C
JD11D
JD11E
JD11F
JD11G
JD11H
JD10A
JD10B
JD10C
JD10D
JD10E
JD10F
JD10G
JD10H
C41
C42
C43
C44
C45
C46
C47
C48
10nF
GND
NetTie
R55
R56
R57
R58
R59
R60
R61
R62
100
JD11_FRO_SEC_ELK_N
JD11_FRO_SEC_ELK_P
JD11_JPL2_1V5
JD10_FRO_SEC_ELK_N
JD10_FRO_SEC_ELK_P
JD10_JPL2_1V5
Project/Equipment -
Document
TE/MPE
Title
Title2
European Organization for Nuclear Research
CH-1211 Geneva 23 - Switzerland
Designer Designer
Drawn by Drawnby
Check by -
Last Mod. -
File DCB_Conn11_10m.SchDoc
Print Date 6/20/2019 7:52:49 AM
6/4/2019
XX/XX/XXXX
Sheet 9 of 21
EDA-XXXXX-VX-X
A2


These resistors are installed for the middle and outer backplane locations ONLY
Pigtail 0
Single-ended signal AC return Paths on Pigtail 0
6 hybrid Sense_GND on Pigtail 2
NOTE: P1_EAST_THERMISTOR, and P2_EAST_THERMISTOR are routed to the telemetry signal connector
List of Hybrid Power circuits that are not used in middle and outer backplanes
(Therefore, the pigtail power breakout boards need to handle these cases)
JP3_JPL1_P4_LV_SOURCE
JP3_JPL1_P4_LV_RETURN
JP3_JPU0_P2_WEST_LV_SOURCE
JP3_JPU0_P2_WEST_LV_RETURN
JP3_JPU0_P1_EAST_LV_SOURCE
JP3_JPU0_P1_EAST_LV_RETURN
Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)
Backplane - Mirror
Pigtail Conn 0
Revision A
Date: 6/20/2019

Pigtail 1

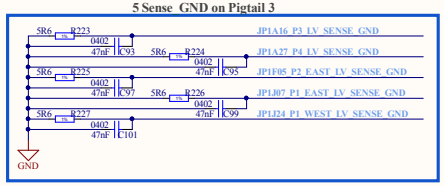


Single-ended signtal AC return Paths on Pigtail 0



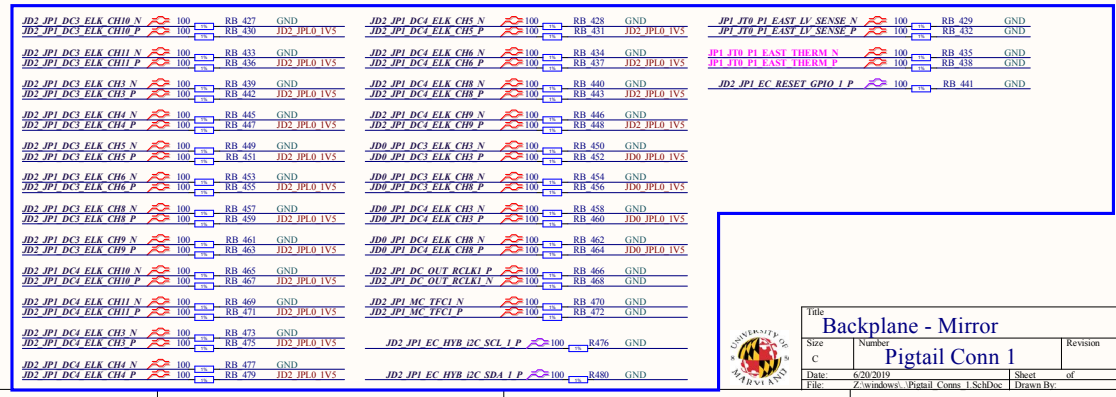
Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

5 Sense GND on Pigtail 3



NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

These resistors are installed for the middle and outer backplane locations ONLY



Title			
Backplane - Mirror			
Size	Number		Revision
C	Pigtail Conn 1		A
Date:	6/20/2019	Sheet	of
File:	Z:\windows\..\Pigtail_Conns_1.SchDoc	Drawn By:	

NOTES:

FP? are placeholders for floating copper. These could be pressed against a carbon-impregnated foam to bleed charge, if needed.

Bright_Blue = AC signal reference ground return

Dark Green = Floating DC Hybrid reference ground return

Light Green =Thermistors

Fuscia = Telemetry Thermistors for connections External to PEPI

These italics signals are not used in the middle and outer backplane locations

GENERAL GROUND RETURN RULES APPLIED

1) Each floating hybrid ground ground is connected directly to the corresponding source regulator return path.
a.) But DC levels relative to the main backplane ground are maintained via ground sense Resistor connected to the main backplane ground. This also has a small parallel EMI cap to shunt high frequency noise.

2) Every single-ended signal from each hybrid has a dedicated ground reference return that is connected to the main backplane ground via a small EMI cap to allow for a high frequency return path only.

3) Analog ground for the PT1000 sensors is intentionally separate from the main backplane ground.

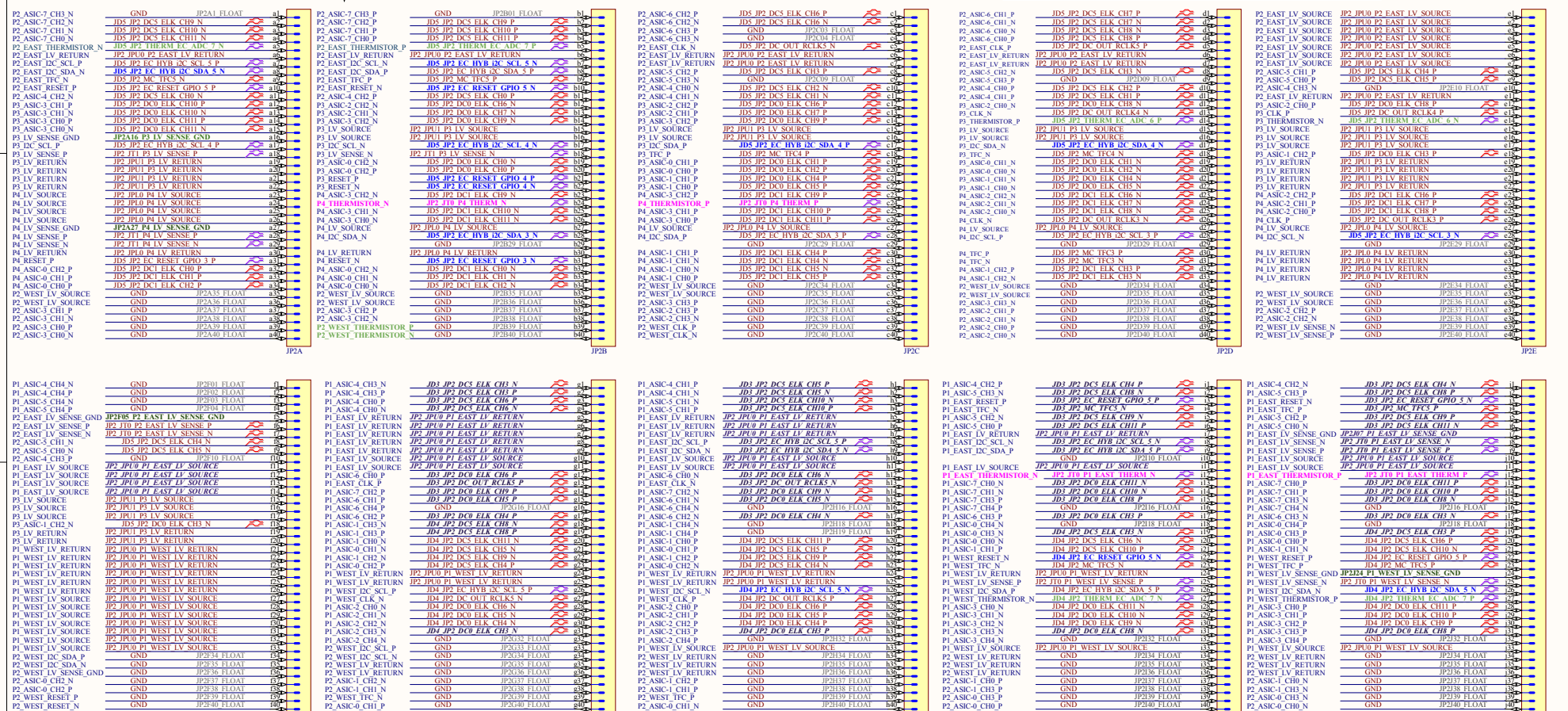
GENERAL COMMENTS:

EC_ADC_REF<15..13> ADC channels can be used to sample the hybrid ground sense.

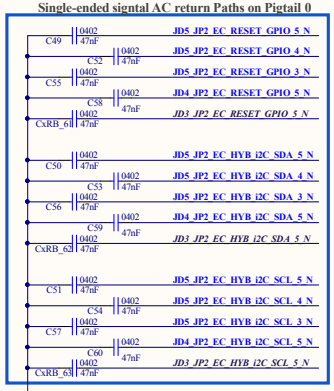
DCB slots 2,3, 10, and 11 can be depopulated for middle and outer backplanes. Therefore, the corresponding ED_ADC channels should be avoided for ground sense and backplane thermistor measurement inputs to ensure the intended measurement connections are available in each of the backplane locations once populated per elink map requirements.

For REF: PigtailV3_Straight_Long

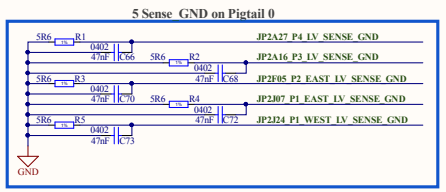
Pigtail 2



Single-ended signtal AC return Paths on Pigtail 0



5 Sense GND on Pigtail 0



NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

JD5_AGND NT27 JD5_JP2_THERM_EC_ADC_7_N

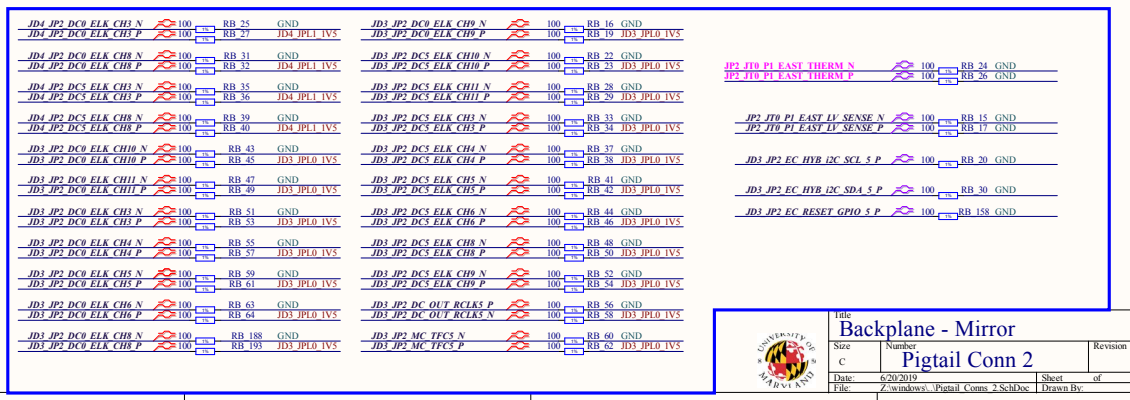
JD5_AGND NT28 JD5_JP2_THERM_EC_ADC_6_N

JD4_AGND NT29 JD4_JP2_THERM_EC_ADC_7_N

List of Hybrid Power circuits that are not used in middle and outer backplanes
(Therefore, the pigtail power breakout boards need to handle these cases)

JP2_JPU0_P1_EAST_LV_SOURCE
JP2_JPU0_P1_EAST_LV_RETURN

These resistors are installed for the middle and outer backplane locations ONLY



Title			
Backplane - Mirror			
Size	Number		Revision
C	Pigtail Conn 2		A
Date:	6/20/2019	Sheet	of
File:	Z:\windows\..\Pigtail_Conns_2.SchDoc	Drawn By:	

NOTES:

FP? are placeholders for floating copper. These could be pressed against a carbon-impregnated foam to bleed charge, if needed.

Bright_Blue =AC signal reference ground return

Dark Green = Floating DC Hybrid reference ground return

Light Green =Thermistors

These italics signals are not used in the middle and outer backplane locations

GENERAL GROUND RETURN RULES APPLIED

1) Each floating hybrid ground ground is connected directly to the corresponding source regulator return path:
a.) But DC levels relative to the main backplane ground are maintained via ground sense Resistor connected to the main backplane ground. This also has a small parallel EMI cap to shunt high frequency noise.

2) Every single-ended signal from each hybrid has a dedicated ground reference return that is connected to the main backplane ground via a small EMI cap to allow for a high frequency return path only.

3) Analog ground for the PT1000 sensors is intentionally separate from the main backplane ground.

P2_EAST_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

GENERAL COMMENTS:

EC_ADC_REF<15..13> ADC channels can be used to sample the hybrid ground sense.

DCB slots 2,3, 10, and 11 can be depopulated for middle and outer backplanes. Therefore, the corresponding ED_ADC channels should be avoided for ground sense and backplane thermistor measurement inputs to ensure the intended measurement connections are available in each of the backplane locations once populated per elink map requirements.

These resistors are installed for the middle and outer backplane locations ONLY

For REF: PigtailV3_Straight_Long

Pigtail 3

Single-ended signtal AC return Paths on Pigtail 0

6 hybrid Sense GND on Pigtail 1

NOTE: P1_EAST_THERMISTOR, and P2_EAST_THERMISTOR are routed to the telemetry signal connector

List of Hybrid Power circuits that are not used in middle and outer backplanes (Therefore, the pigtail power breakout boards need to handle these cases)

JP3_JP1_P4_LV_SOURCE JP3_JPU0_P1_EAST_LV_SOURCE

JP3_JP1_P4_LV_RETURN JP3_JPU0_P1_EAST_LV_RETURN

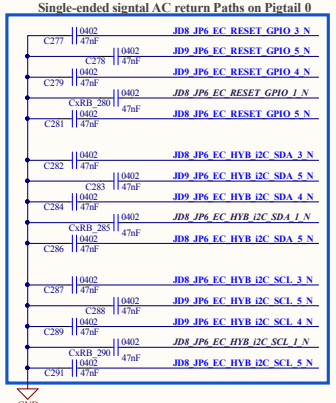
JP3_JPU0_P2_WEST_LV_SOURCE

JP3_JPU0_P2_WEST_LV_RETURN

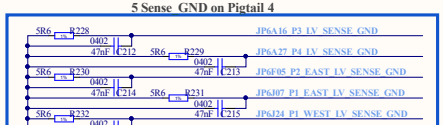
Depopulate SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 10kohm resistors (see variants)

Pigtail 6

Single-ended signtal AC return Paths on Pigtail 0



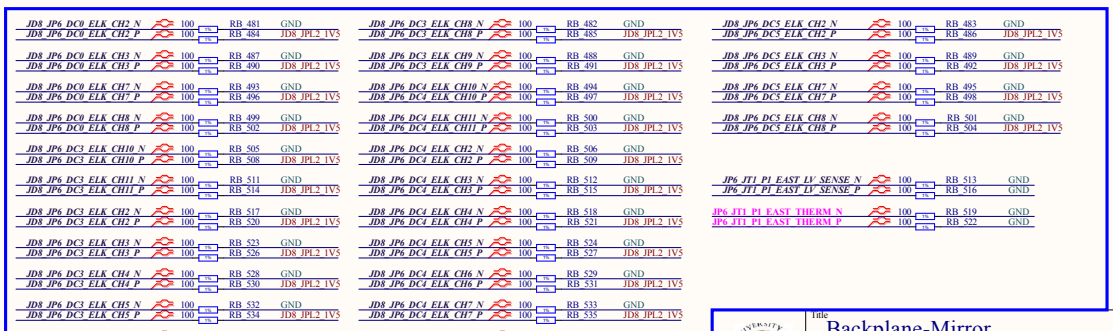
5 Sense GND on Pigtail 4



NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

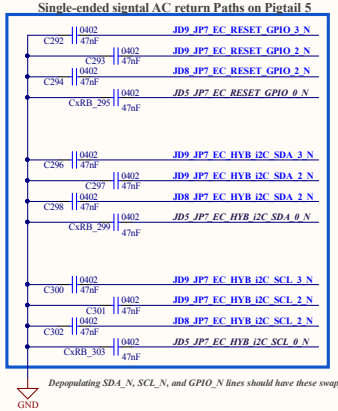
These resistors are installed for the middle and outer backplane locations ONLY



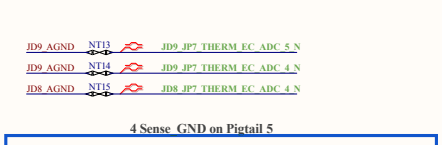
Title	Backplane-Mirror		
Size	Number		Revision
C	Pigtail Conn 6		A
Date:	6/20/2019	Sheet	of
File:	Z:\windows\..\Pigtail_Conns_6.SchDoc	Drawn By:	

Pigtail 7

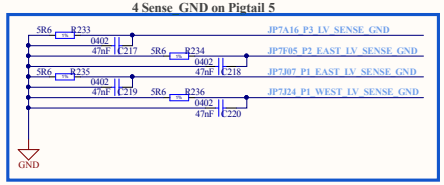
Single-ended signtal AC return Paths on Pigtail 5



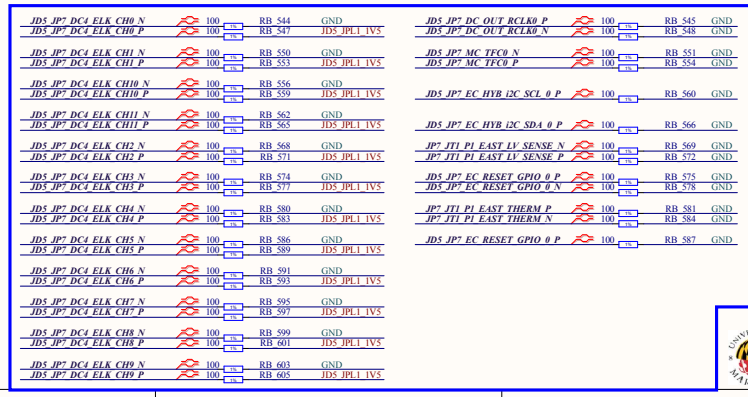
Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)



4 Sense_GND on Pigtail 5



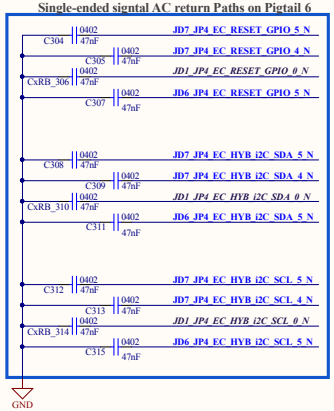
These resistors are installed for the middle and outer backplane locations ONLY



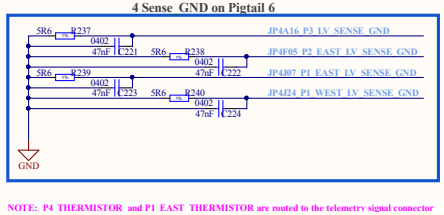
Title	Backplane - Mirror		
Size	Number		Revision
C	Pigtail Conn 7		A
Date:	6/20/2019	Sheet	of
File:	Z:\windows\..\Pigtail_Conns_7.SchDoc	Drawn By:	

Pigtail 4

Single-ended signtal AC return Paths on Pigtail 6



4 Sense GND on Pigtail 6



NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

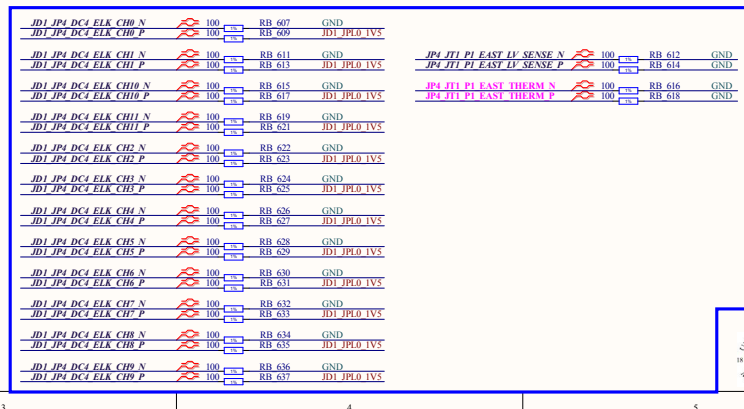
JD7_AGND — JD7_JP4_THERM_EC_ADC_7_N

JD7_AGND — JD7_JP4_THERM_EC_ADC_6_N

JD6_AGND — JD6_JP4_THERM_EC_ADC_7_N

Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

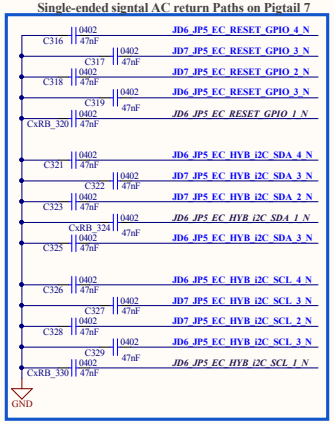
These resistors are installed for the middle and outer backplane locations ONLY



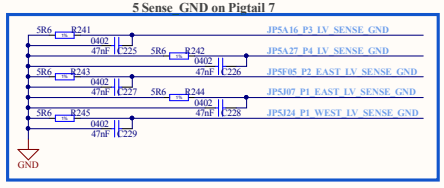
Title	Backplane - Mirror		
Size	Number	Pigtail Conn 4	Revision A
Date:	6/20/2019	Sheet	of
File:	Z:\windows\..\Pigtail_Conns_4.SchDoc	Drawn By:	

Pigtail 5

Single-ended signtal AC return Paths on Pigtail 7



5 Sense_GND on Pigtail 7

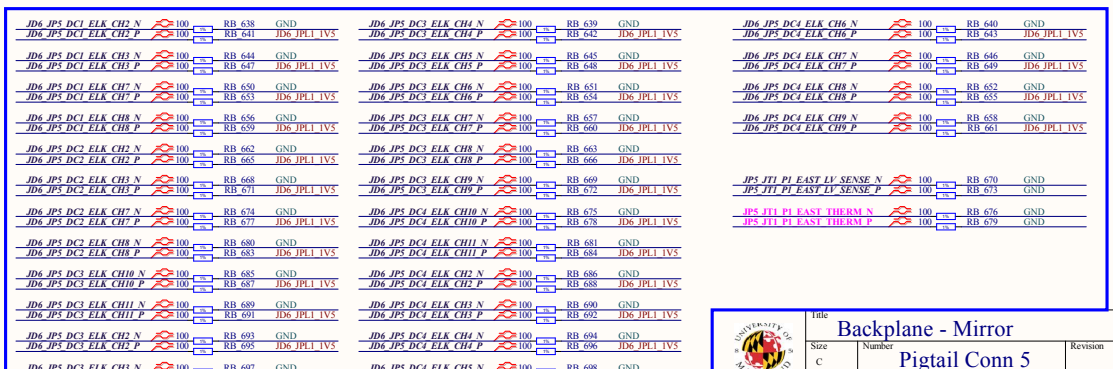


NOTE: P4_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector

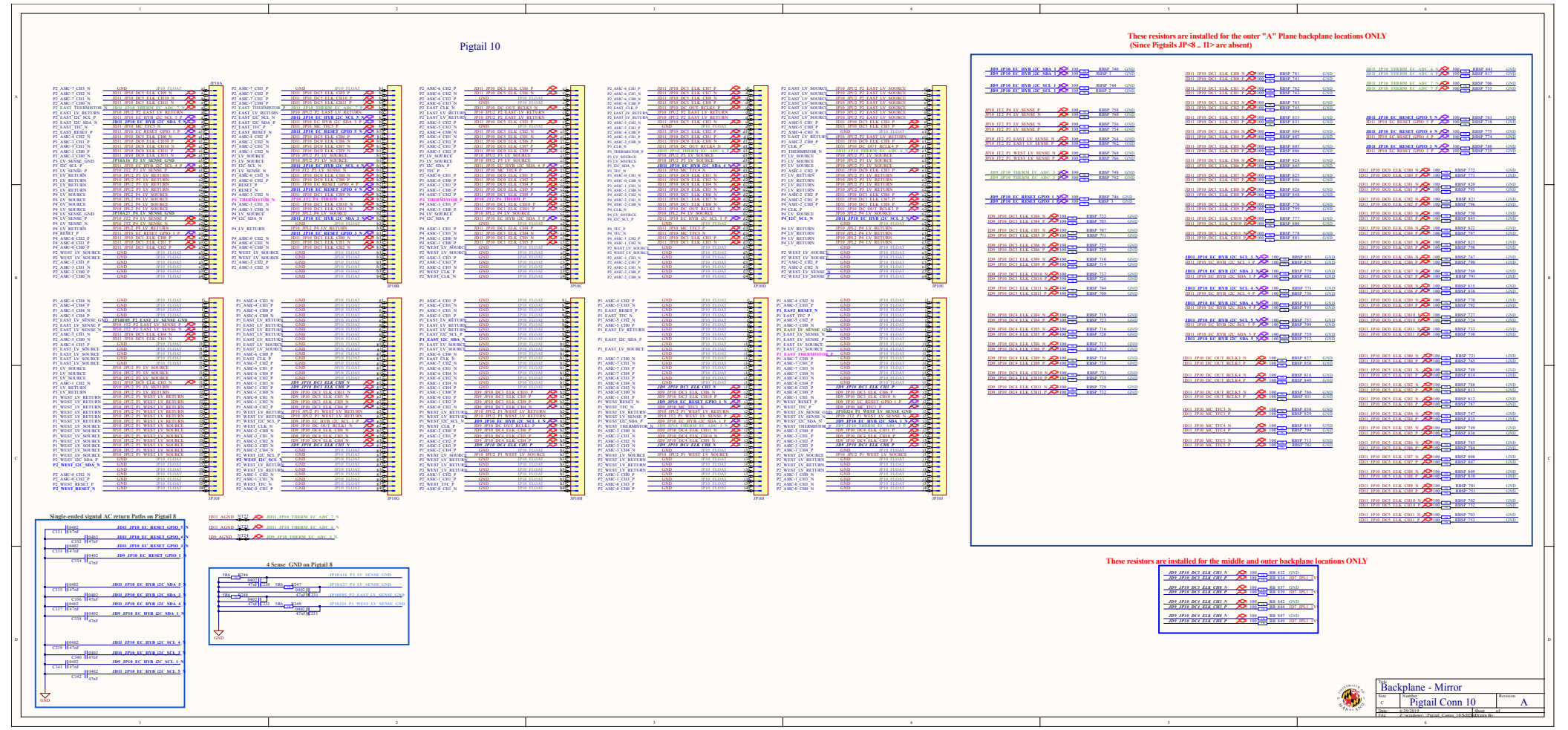
JD6 AGND NT19 JD6 JP5_THERM_EC_ADC_6_N
JD7 AGND NT20 JD7 JP5_THERM_EC_ADC_5_N
JD6 AGND NT31 JD6 JP5_THERM_EC_ADC_5_N

Depopulating SDA_N, SCL_N, and GPIO_N lines should have these swapped for 0402 100ohm resistors (see variants)

These resistors are installed for the middle and outer backplane locations ONLY

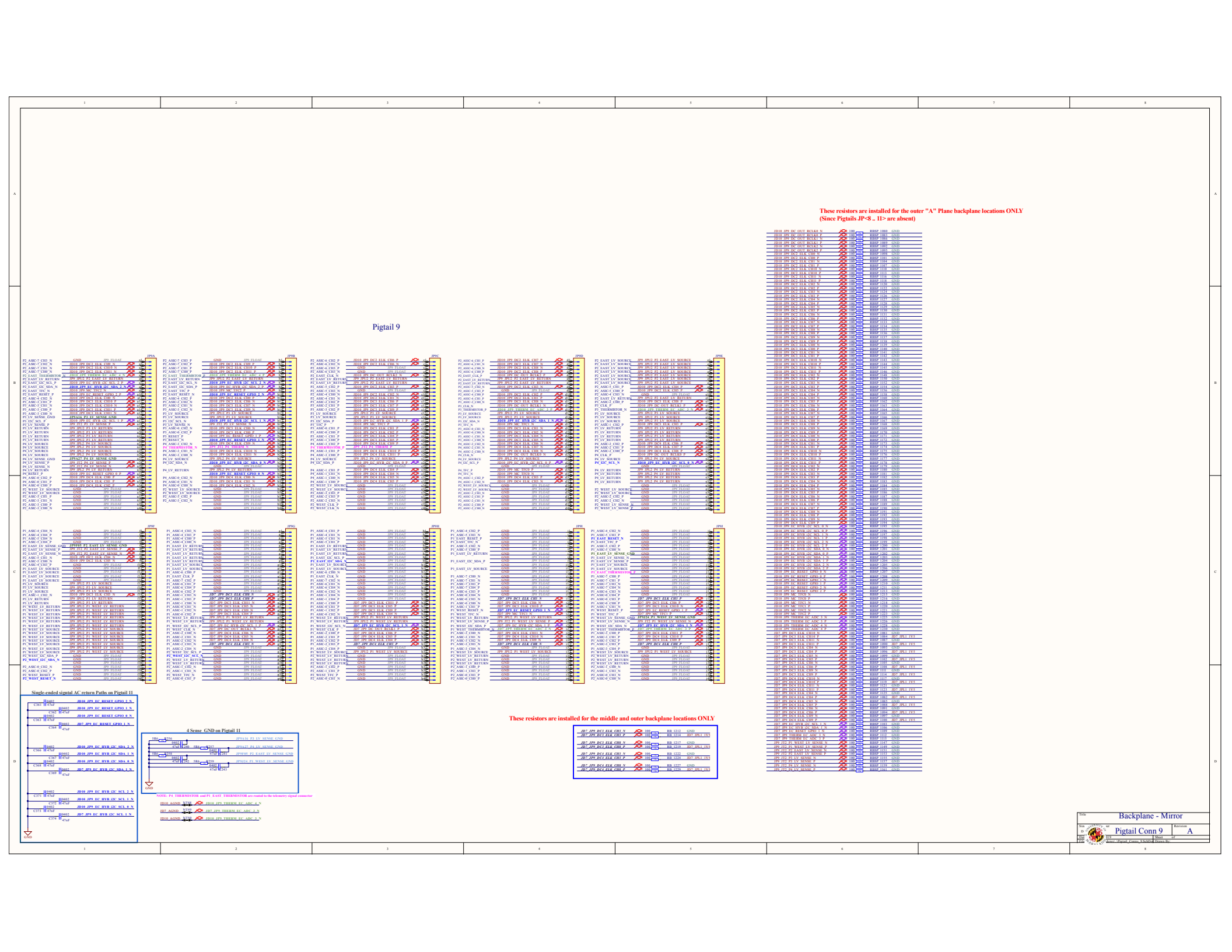


Title	Backplane - Mirror		
Size	Number		Revision
C	Pigtail Conn 5		A
Date:	6/20/2019	Sheet	of
File:	Z:\windows\..\Pigtail_Conns_5.SchDoc	Drawn By:	


Pigtail 10
These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)
These resistors are installed for the middle and outer backplane locations ONLY
Single-ended signtal AC return Paths on Pigtail 8
4 Sense GND on Pigtail 8
Backplane - Mirror
Pigtail Conn 10
A
4/20/2019


Pigtail 11
These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)
Single-ended signal AC return Paths on Pigtail 9
3 Sense GND on Pigtail 9
Backplane - Mirror
Pigtail Conn 11
A
Title
Backplane - Mirror
Size C
Number
Pigtail Conn 11
Revision
Date: 6/20/2019
Sheet of
File: Z:\windows\...\Pigtail_Conn_11.SchDoc
Drawn By:


Pigtail 8
These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)
Single-ended signtal AC return Paths on Pigtail 10
3 Sense GND on Pigtail 10
NOTE: P4 THERMISTOR and P1 EAST THERMISTOR are routed to the telemetry signal connector
Backplane - Mirror
Pigtail Conn 8
A
6/20/2019


Pigtail 9
These resistors are installed for the outer "A" Plane backplane locations ONLY
(Since Pigtails JP<8 .. 11> are absent)
These resistors are installed for the middle and outer backplane locations ONLY
Single-ended signtal AC return Paths on Pigtail 11
4 Sense GND on Pigtail 11
NOTE: P1_THERMISTOR and P1_EAST_THERMISTOR are routed to the telemetry signal connector
Backplane - Mirror
Pigtail Conn 9
A