

SLV\$outTestSel[1:0] = ckCt0[7:6] = Register 0[7:6]
dOut32 can be driven by the:

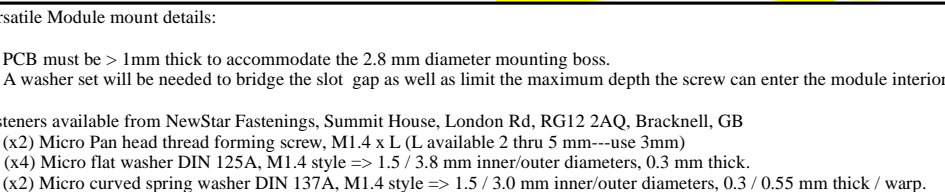
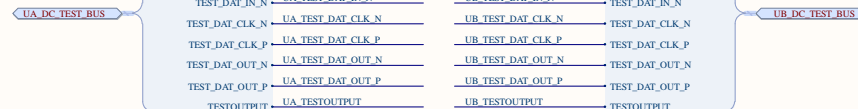
- a) normal data output,
- b) input dIn32
- c) a signal injected into the external CMOS pad SLV\$testInject.

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2.5V/100nF/L/47uF+0.1uF
L_c = 1uH to 4.7uH

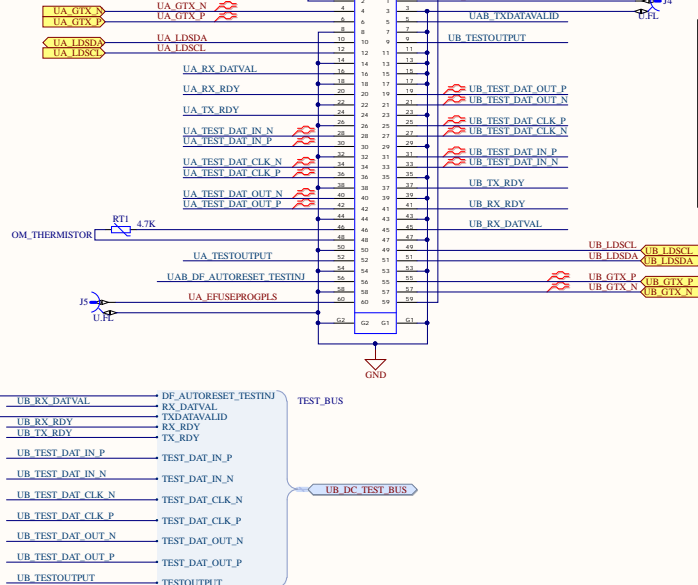


"TEST BUS" Label	MC VTTx Ah Signal Name
TESTOUTPUT	MC_RESETB
TEST_DAT_OUT_P	MC_I2C_SCL
TEST_DAT_OUT_N	MC_I2C_SDA
TEST_DAT_CLK_P	DC_RESETB
TEST_DAT_CLK_N	DC_I2C_SCL
TEST_DAT_IN_N	DC_I2C_SDA



Hermaphroditic Connector: HAS a swap of EVEN and ODD pin assignments relative to the mating board!!!

USE PEPI Library parts Optical_Module PCB and DCB. OPT_MOD_MATE Holes to align hole features between assemblies.



Samtec Conn P/N:
LSHM-130-06.0-L-DV-A-S-K-TR

Title DCB Optical Mezzanine Board		
Size C	Number	Revision A
Date: 7/23/2018	Sheet 1	of 1
File: C:\Users\... \DCB OPT DB Schematic.sch		Drawn By: Tom O'Bannon