

Willis Allstead

CPE 201L

Section: 1102

Deepak Tosh

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LAB 7

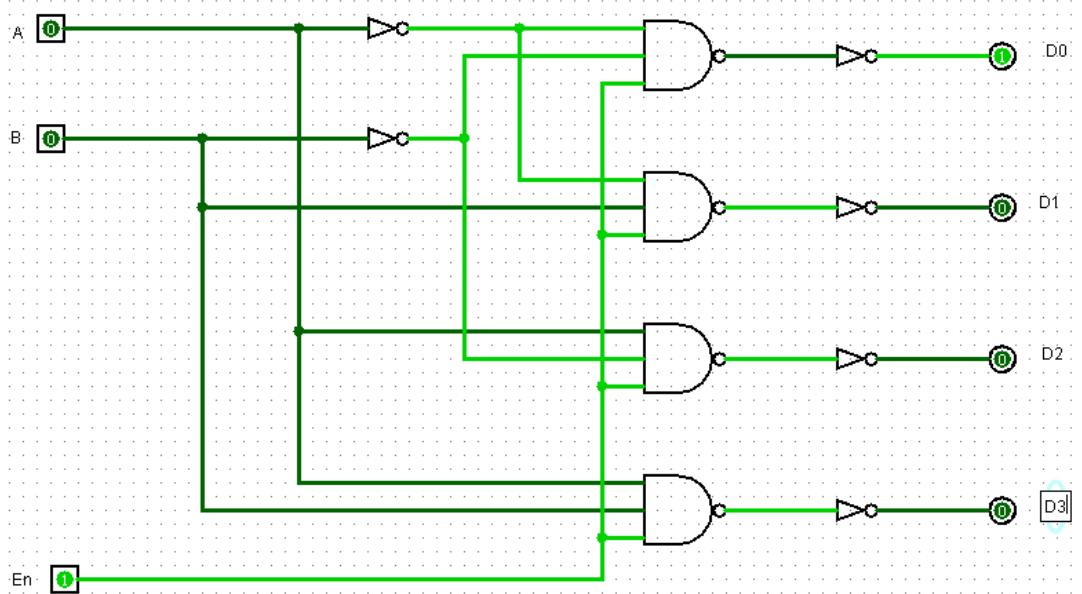
Work:

Lab 7 Decoders	
2 to 4 Active High Decoders	
EAB	D ₀ D ₁ D ₂ D ₃
000	0 0 0 0
001	0 0 0 0
010	0 0 0 0
011	0 0 0 0
100	0 0 0 0 → A'B' ✓
101	0 1 0 0 → A'B' ✓
110	0 0 1 0 → A'B' ✓
111	0 0 0 1 → AB ✓

A logic diagram showing a 2-to-4 active-high decoder. The inputs are E, A, and B. The outputs are D₀, D₁, D₂, and D₃. The circuit uses three AND gates and one OR gate.

2 to 4 Active Low Decoder	
EAB	D ₀ D ₁ D ₂ D ₃
000	0 1 1 1
001	1 0 1 1
010	1 1 0 1
011	1 1 1 0
100	1 1 1 1
101	1 1 1 1
110	1 1 1 1
111	1 1 1 1

2x4 Active High Decoder:



Combinational Analysis

a	b	c	x	y	z	u
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

Build Circuit

2x4 Active Low Decoder:

