	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	INC^1	INC^1	INC^1	INC^1	INC^1	INC^1	INC^1	INC^1	ADDC	ADDC	ADDC	ADDC	ADDC	ADDC	ADDC	ADDC
1x	MOV^1	MOV^1	MOV^1	MOV^1	MOV^1	MOV^1	MOV^1	MOV^1	OR	OR	OR	OR	OR	OR	OR	OR
2x	AND	AND	AND	AND	AND	AND	AND	AND	XOR	XOR	XOR	XOR	XOR	XOR	XOR	XOR
3x	RLC	RLC	RLC	RLC	RLC	RLC	RLC	RLC	RRC	RRC	RRC	RRC	RRC	RRC	RRC	RRC
4x	DEC	DEC	DEC	DEC	DEC	DEC	DEC	DEC	SUBB	SUBB	SUBB	SUBB	SUBB	SUBB	SUBB	SUBB
5x	ADD	ADD	ADD	ADD	ADD	ADD	ADD	ADD	SET	SET	SET	SET	SET	SET	SET	SET
6x	BIT	BIT	BIT	BIT	BIT	BIT	BIT	BIT	CLR	CLR	CLR	CLR	CLR	CLR	CLR	CLR
7x	MOV^2	MOV^2	MOV^2	MOV^2	MOV^2	MOV^2	MOV^2	MOV^2	CMP	CMP	CMP	CMP	CMP	CMP	CMP	CMP
8x	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	PUSH	POP	POP	POP	POP	POP	POP	POP	POP
9x	JNZ	JNC	JNN	JNB	JNF4	JNI	JNF6	JNF7	JZ	JC	JN	JB	JF4	JI	JF6	JF7
Ax	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?
Bx	?	?	?	?	?	?	?	?	DBG?	RET	IRET	?	JMP	?	?	CALL
Cx	INC^2	~~INC^2~~	INC^2	~~INC^2~~	INC^2	~~INC^2~~	INC^2	~~INC^2~~	MOV^3	MOV^3	MOV^3	MOV^3	MOV^3	MOV^3	MOV^3	MOV^3
Dx	MOV^4	~~MOV^4~~	MOV^4	~~MOV^4~~	MOV^4	~~MOV^4~~	MOV^4	~~MOV^4~~	MOV^5	~~MOV^5~~	MOV^5	~~MOV^5~~	MOV^5	~~MOV^5~~	MOV^5	~~MOV^5~~
Ex	MOV^6	MOV^6	MOV^6	MOV^6	MOV^6	MOV^6	MOV^6	MOV^6	MOV^7	MOV^7	MOV^7	MOV^7	MOV^7	MOV^7	MOV^7	MOV^7
Fx	MOV^8	~~MOV^8~~	MOV^8	~~MOV^8~~	MOV^8	~~MOV^8~~	MOV^8	~~MOV^8~~	MOV^9	~~MOV^9~~	MOV^9	~~MOV^9~~	MOV^9	~~MOV^9~~	MOV^9	~~MOV^9~~

Abbr.	Instruction
INC^1	INC Ra
INC^2	INC RbRa
MOV^1	MOV R0, Ra
MOV^2	MOV Ra, R0
MOV^3	MOV [#abs], Ra
MOV^4	MOV [RbRa], R0
MOV^5	MOV [RbRa+imm], R0
MOV^6	MOV Ra, #imm
MOV^7	MOV Ra, [#abs]
MOV^8	MOV R0, [RbRa]
MOV^9	MOV R0, [RbRa+imm]

Legend	
AND	Arithmetic, logical
MOV^1	Move, load, store
JZ	Control flow
PUSH	Stack
?	Unknown
╱	Broken