SNES / Super Famicom Joystick Data

This file was originally written by Jim Christy. It includes controller chip details and some info on it's inner workings. The file has been heavily modified, as usual, and any comments in yellow are by us. Enjoy!

Pin	Description	Wire Color
1	+5v	White
2	Data Clock	Yellow
3	Data Latch	Orange
4	Serial Data	Red
5	N/C	-
6	N/C	-
7	Ground	Brown

Additional notes by Jim Christy:

Pins 5 and 6 show a DC voltage of 5v on a DMM. I forgot to look at them on a scope so there may pulses too. However, they don't connect to anything at present.

Although rubber domes are used to provide the tactile response of the buttons, they are not capacitive technology as originally thought. Instead they use what appears to be carbon impregnated rubber on the underside which makes a resistive path (200 ohms) across 2 carbon coated PCB pads when depressed. ie, it's the same button system as in every other controller ever made!

Every 16.67ms (or about 60Hz), the SNES CPU sends out a 12us wide, positive going data latch pulse on pin 3. This instructs the ICs in the controller to latch the state of all buttons internally. Six microsenconds after the fall of the data latch pulse, the CPU sends out 16 data clock pulses on pin 2. These are 50% duty cycle with 12us per full cycle. The controllers serially shift the latched button states out pin 4 on every rising edge of the clock, and the CPU samples the data on every falling edge.

Each button on the controller is assigned a specific ID which corresponds to the clock cycle during which that button's state will be reported. The table in section 4.0 lists the ids for all

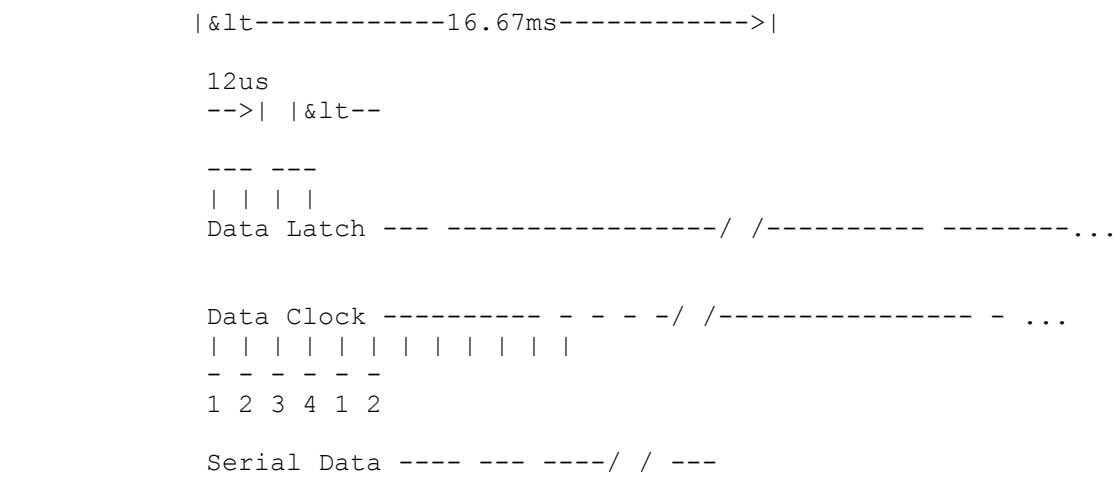
buttons. Note that multiple buttons may be depressed at any given moment. Also note that a logic "high" on the serial data line means the button is NOT depressed.

At the end of the 16 cycle sequence, the serial data line is driven low until the next data latch pulse. The only slight deviation from this protocol is apparent in the first clock cycle. Because the clock is normally high, the first transition it makes after latch signal is a high-to-low transition. Since data for the first button (B in this case) will be latched on this transition, it's data must actually be driven earlier. The SNES controllers drive data for the first button at the falling edge of latch. Data for all other buttons is driven at the rising edge of clock. Hopefully the following timing diagram will serve to illustrate this. Only 4 of the 16 clock cycles are shown for brevity.

SNES Controller Button-to-Clock Pulse Assignment

Clock Cycle	Button Reported
1	B
2	Y
3	Select
4	Start
5	Up on joypad
6	Down on joypad
7	Left on joypad
8	Right on joypad
9	A
10	X
11	L
12	R
13-16	none (always high)

Clock cycles 13-16 are essentially unused. It would be interesting to see how the SNES responds if we drive low button data during these cycles. Nintendo may use these for future controllers with more capabilities.



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(Buttons B --- --- --- ----------
& Select norm B SEL norm
pressed). low low
12us
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