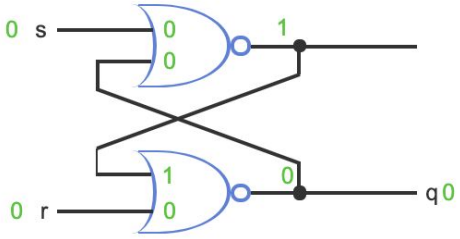
3.1 SR latches

- Storing a bit
  - A ***sequential circuit***'s output is dependent on the present and the past *sequence* of input values, which necessarily means the circuit stores at least one bit. In contrast, a ***combinational circuit***'s output is dependent only on the present *combination* of input values
- SR latch
  - Latch: simplest circuit for storing a bit
  - SR latch: stores one bit, with an input **s** to set the latch to 1, an input **r** to reset the latch to 0, and with the stored bit appearing on output **q**.
    - S and s are for "set"
    - R and r are for "reset"



Reminder

a	b	NOR
0	0	1
0	1	0
1	0	0
1	1	0

s	r	q
0	0	Previously-stored bit
0	1	0 ("Reset")
1	0	1 ("Set")
1	1	Unknown

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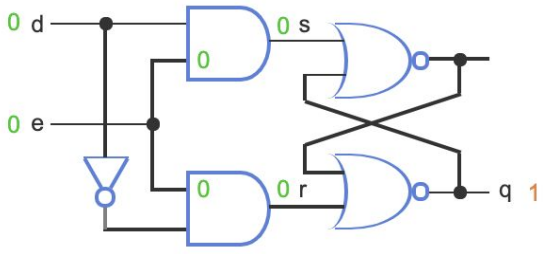
  - s = 1 and r = 1 causes a problem
  - Oscillate means to change from 0 to 1 to 0 to 1 repeatedly
    - q oscillates while s and r are both 1's
    - The problem appears when s and r both change back to 0's

3.2 Clocks, D flip-flops, and register

- D latch:
  - stores 1 bit with an input d having the bit to be stored
  - An input e that when 1 enables storing the bit
  - With the storing bit appearing on output q



e	d	q
0	0	Previously-stored bit (d is ignored)
0	1	Previously-stored bit (d is ignored)
1	0	0 (d is stored)
1	1	1 (d is stored)

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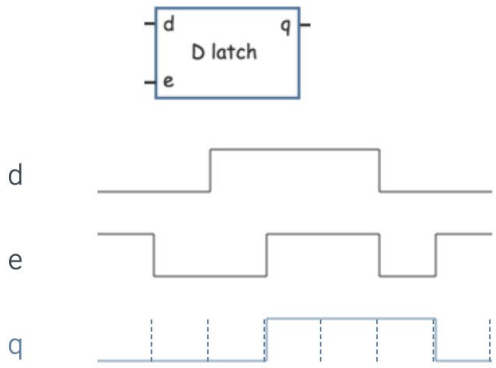
- Clock
  - Oscillating signal, to control when to store bits

- Rather than bits being stored while an enable signal is high, bits are stored only at a clock's **rising edge**: signal changes from 0 to 1
    - Clock style - time between two rising edges, AKA clock period
    - Clock frequency - cycles per second, in units of hertz(Hz)
        - 1 MHz clock has 1 million cycles per second
        - 1 microsecond (0.000001) period yields a frequency of 1 MHz
- On each rising clock edge, the bits move **simultaneously**
- On each rising clock edge, the bits move one place to the **right**
- A **triangle** indicates the clock input of a component

- D flip-flops
    - A latch stores a new bit while an enable input is 1
    - A latch is said to be **level sensitive**, storing when the enable's "level" is high
    - In contrast, a flip-flop stores a new bit only at the instant of clock input's rising
    - A flip-flop is said to be edge-triggered
    - Master servant VS Master slave
        - Implemented by cascading two D latches
        - 1st - enable inverted - master
        - 2nd - servant



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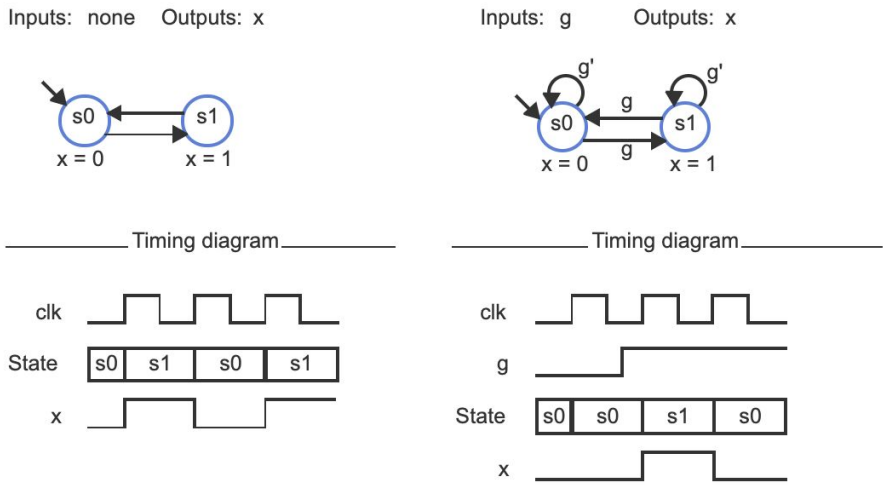
    - Note that **q stays the same when e = 0, when e = 1, d is stored in q**

- Basic Register
    - A circuit that stores a group of bits
    - eg: 3-bit register stores 3 bits
    - Storing bits in a register is known as **loading the register**
    - Note that **register only loads a rising clock edge**

3.3 FSMs

- Combinational
  - A circuit is combinational if the circuit's output values depend solely on the present combination of input values
- Sequential
  - If the output depends **not only** on the present input values **but also on the sequence of past values**
- FSM
  - Finite-state machine, computation model capable of describing sequential behavior
  - Execution
    - **State** - present situation of digital system
    - Every time an implicit clock input rises, the FSM changes to a next state pointed to by a transition whose condition evaluates to true (1)
    - A transition **without** a listed condition has an implicit condition of true.



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3.4 FSM Simulator

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