Instruction Set Architecture

	[17:15] (opcode)	[14:11]	[10:7]	[6]	[5:4]	[3:0]
ADD	000	DST	SRC1	0	00	SRC2
ADDI	000	DST	SRC	1	imm6	
AND	001	DST	SRC1	0	00	SRC2
ANDI	001	DST	SRC	1	imm6	
OR	010	DST	SRC1	0	00	SRC2
ORI	010	DST	SRC	1	imm6	
XOR	011	DST	SRC1	0	00	SRC2
XORI	011	DST	SRC	1	imm6	
LD	100	DST	Address11			
ST	101	SRC	Address11			
JUMP	110	Address15 - PC Relative				

ADD DST,SRC1,SRC2 ; DST = SRC1 + SRC2

ADDI DST,SRC,imm6 ; DST = SRC + Sign Extend[imm6](Sign extend 6 bits immediate to 16 bits)

AND DST,SRC1,SRC2 ; DST = SRC1 & SRC2

ANDI DST,SRC,imm6 ; DST = SRC & Sign Extend[imm6](Sign extend 6 bits immediate to 16 bits)

OR DST,SRC1,SRC2 ; DST = SRC1 | SRC2

ORI DST,SRC,imm6 ; DST = SRC | Sign Extend[imm6](Sign extend 6 bits immediate to 16 bits)

XOR DST,SRC1,SRC2 ; DST = SRC1 $\oplus$ SRC2

XORI DST,SRC,imm6 ; DST=SRC $\oplus$ Sign Extend[imm6](Sign extend 6 bits immediate to 16 bits)

LD DST,Address11 ; DST = DataMemory[ZeroExtend[Address11]]

ST SRC,Address11 ; DataMemory[ZeroExtend[Address11]] = SRC

JUMP Address15 ; PC = SignExtend[Address15](Sign extend 15 bits immediate to 16 bits)

	[17:15](opcode)	[14:12](nzp)	[11:8]	[7:4]	[3:0]
BEQ	111	010	OP1	OP2	Address4 - PC Rel
BGT	111	001	OP1	OP2	Address4 - PC Rel
BLT	111	100	OP1	OP2	Address4 - PC Rel
BGE	111	011	OP1	OP2	Address4 - PC Rel
BLE	111	110	OP1	OP2	Address4 - PC Rel

BEQ OP1,OP2,Address4 ;

If OP1 == OP2 then GO TO SignExtend[Address4](Sign extend 4 bits immediate to 16 bits)

BGT OP1,OP2,Address4 ;

If OP1 > OP2 then GO TO SignExtend[Address4](Sign extend 4 bits immediate to 16 bits)

BLT OP1,OP2,Address4 ;

If OP1 < OP2 then GO TO SignExtend[Address4](Sign extend 4 bits immediate to 16 bits)

BGE OP1,OP2,Address4 ;

If OP1 >= OP2 then GO TO SignExtend[Address4](Sign extend 4 bits immediate to 16 bits)

BLE OP1,OP2,Address4 ;

If OP1 <= OP2 then GO TO SignExtend[Address4](Sign extend 4 bits immediate to 16 bits)

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