# CSE 3015 DIGITAL LOGIC DESIGN TERM PROJECT

**Step 1:** At this step, we design the instruction set architecture with 3-bit opcodes. While designing ISA at first, we thought using unique opcodes for each operation, but it was not efficient. Then, we used the same opcode for 2 register arithmetic operations and one register-one immediate value operations, for example ADD and ADDI have same opcode. And all branches also have same opcode because they have unique 'nzp' value for identify themselves.

After designing ISA, we wrote a java code for converting Assembly instructions to Hexadecimal values according to ISA file. We did this because Logisim memory images can only have hex instructions.

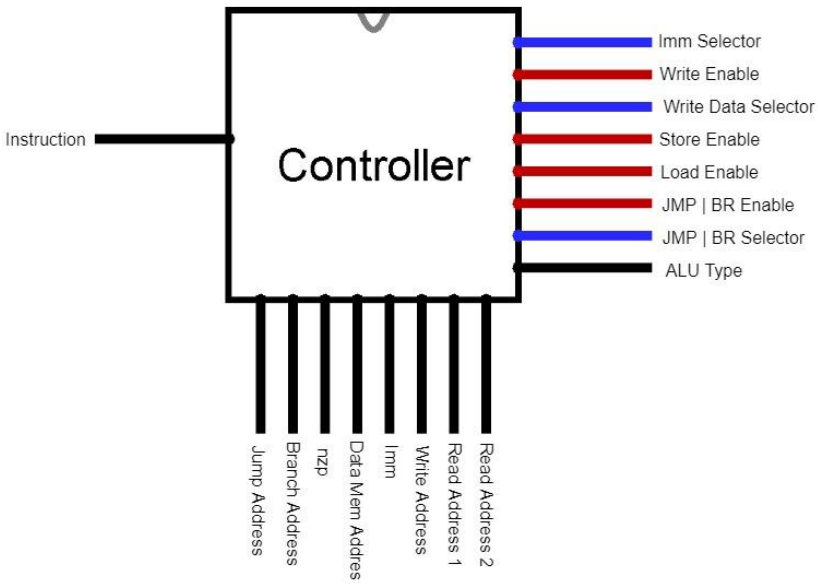
**Step 2:** At this step, we started to design out circuit. Firstly, we create and design arithmetic logic unit, instruction memory, data memory, jump instruction, branch instruction, and register file components. Only for this step we used Logisim's sign extender, adder, and comparator components. At the end of this step, our circuit was working but there were no controller and the whole mission was run on main circuit.

**Step 3:** At this step, we design adder, comparator, sign extenders, and controller. 18-bit adder has 1 half adder and 17 full adders. It is working with two's complement numbers.

18-bit comparator has 17 comparator stages. It is 17 because left-most bit of a number is the sign bit. We are checking these bits separately. For example, if OP1's left-most bit is 1 and OP2's left-most bit is 0 then OP1 is smaller than OP2 because OP1 is negative and OP2 is positive and vice-versa. If their left-most bits have same value, comparator normally controls the numbers.

Also, we have 3 sign extenders. 4 to 18 sign extenders used for branch instructions' addresses. 6 to 18 sign extenders used for ADDI, ANDI, ORI, XORI operations' immediate values. 15 to 18 sign extenders used for extending jump instructions' addresses.

Our controller takes instruction and returns some values to control the whole circuit.

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