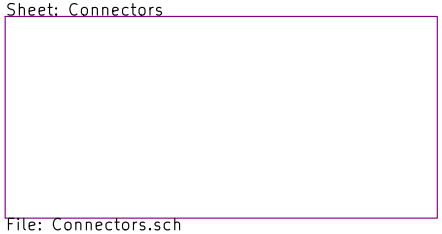
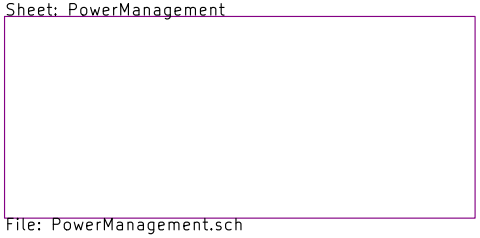
Sheet: Connectors



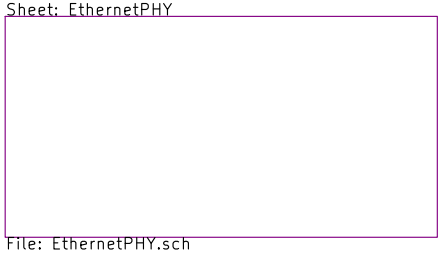
File: Connectors.sch

Sheet: PowerManagement



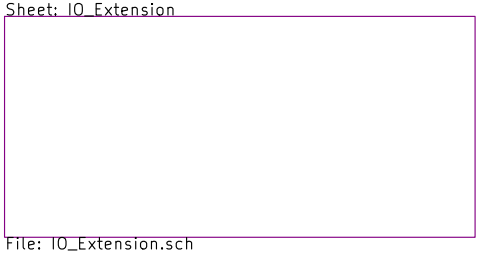
File: PowerManagement.sch

Sheet: EthernetPHY



File: EthernetPHY.sch

Sheet: IO_Extension

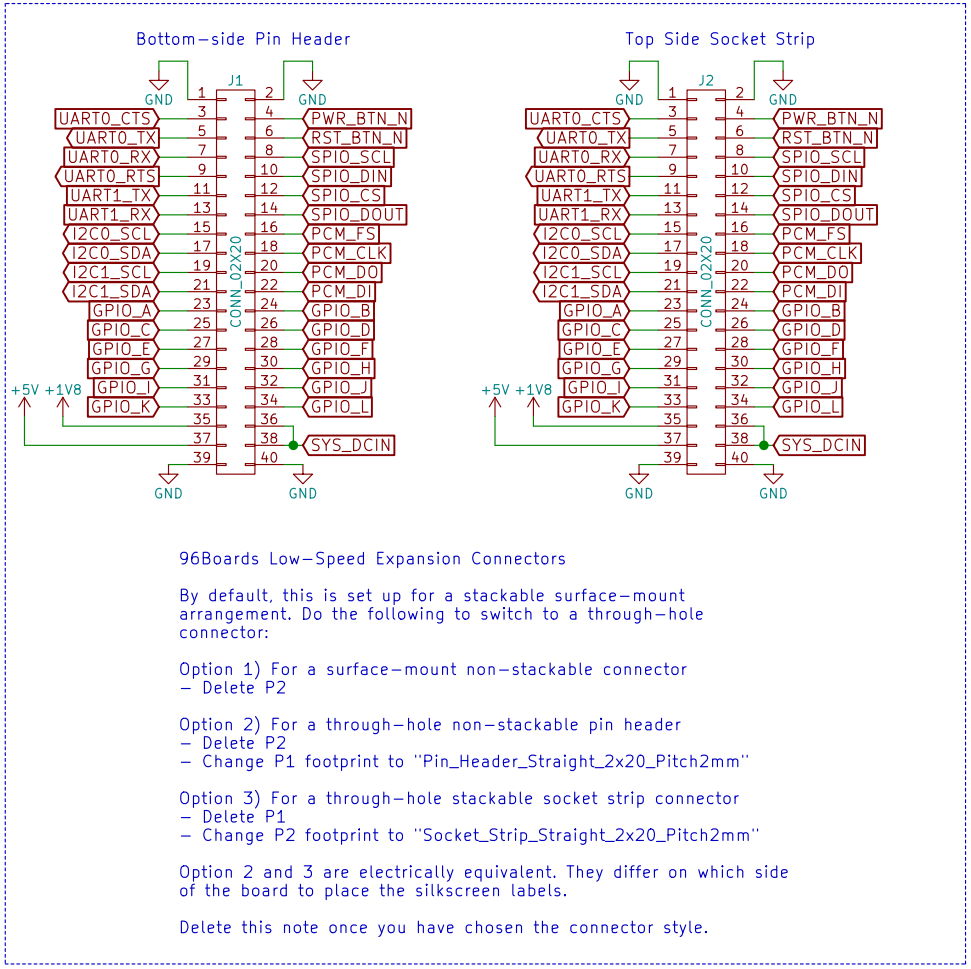


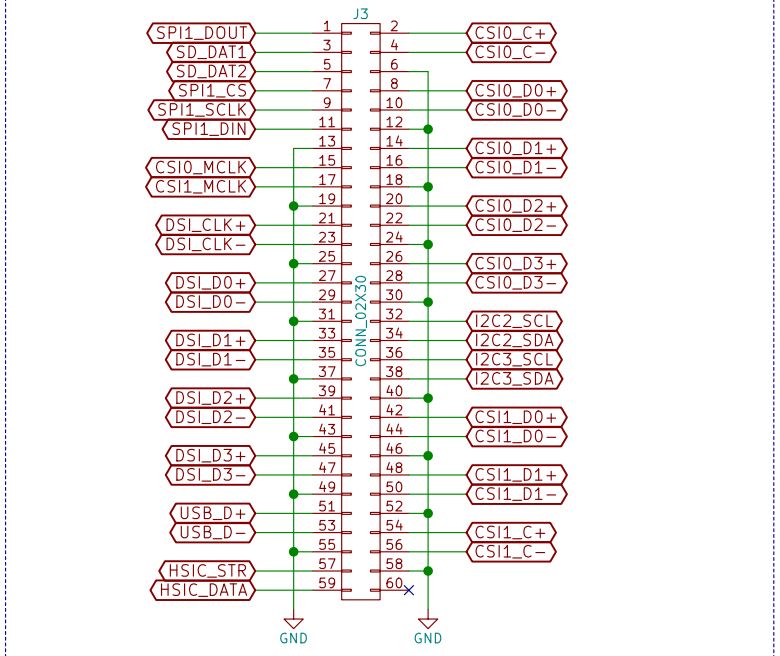
File: IO_Extension.sch

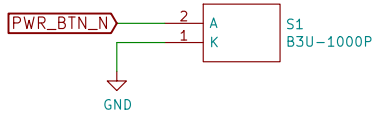
Sheet: /
File: EthernetBoard.sch

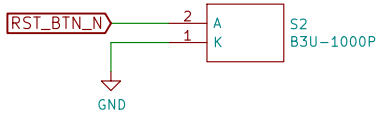
Title: 96Boards Mezzanine Project Template

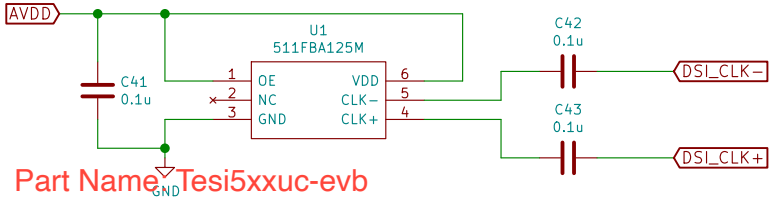
Size: A4	Date: 14 Aug 2015	**Rev: A**
KiCad E.D.A. kicad 5.1.5-52549c584ubuntu18.04.1		Id: 1/5











Part Name Tesi5xxuc-evb
(Universal Oscillator Evaluation Kitxt) used 1.1uF for C41.
Did not reflect on here this time.

Sheet: /Connectors/ File: Connectors.sch		
Title:		
Size: A4	Date:	**Rev:**
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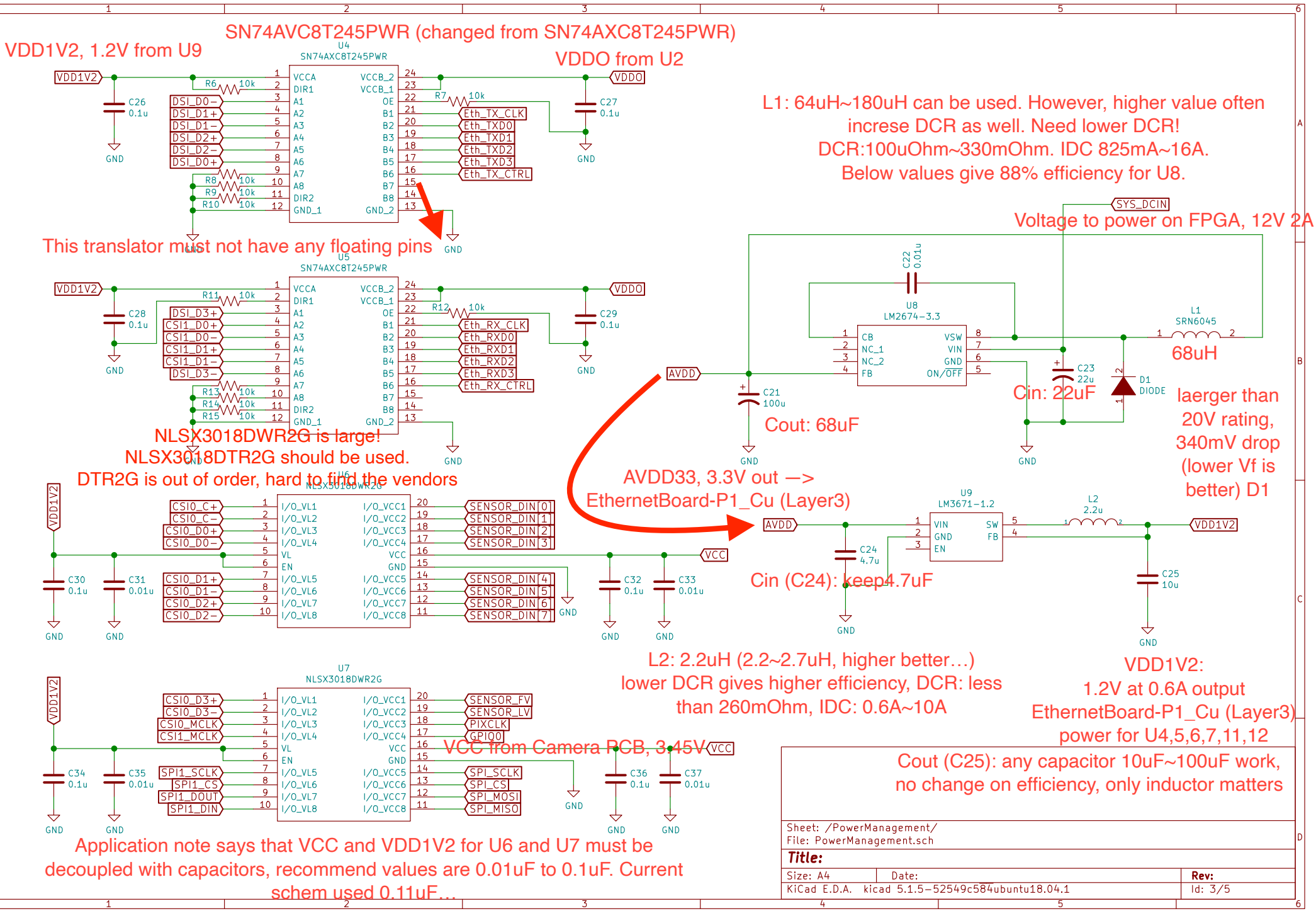
SN74AVC8T245PWR (changed from SN74AXC8T245PWR)
VDD1V2, 1.2V from U9
VDDO from U2
U4
SN74AXC8T245PWR
VDD1V2
VDDO
R6 10k
R7 10k
R8 10k
R9 10k
R10 10k
C26 0.1u
C27 0.1u
GND
DSI_D0−
DSI_D1+
DSI_D1−
DSI_D2+
DSI_D2−
DSI_D0+
Eth_TX_CLK
Eth_TXD0
Eth_TXD1
Eth_TXD2
Eth_TXD3
Eth_TX_CTRL
VCCA
DIR1
A1
A2
A3
A4
A5
A6
A7
A8
DIR2
GND_1
VCCB_2
VCCB_1
OE
B1
B2
B3
B4
B5
B6
B7
B8
GND_2
This translator must not have any floating pins
U5
SN74AXC8T245PWR
R11 10k
R12 10k
R13 10k
R14 10k
R15 10k
C28 0.1u
C29 0.1u
DSI_D3+
CSI1_D0+
CSI1_D0−
CSI1_D1+
CSI1_D1−
DSI_D3−
Eth_RX_CLK
Eth_RXD0
Eth_RXD1
Eth_RXD2
Eth_RXD3
Eth_RX_CTRL
NLSX3018DWR2G is large!
NLSX3018DTR2G should be used.
DTR2G is out of order, hard to find the vendors
U6
NLSX3018DWR2G
CSI0_C+
CSI0_C−
CSI0_D0+
CSI0_D0−
CSI0_D1+
CSI0_D1−
CSI0_D2+
CSI0_D2−
I/O_VL1
I/O_VL2
I/O_VL3
I/O_VL4
VL
EN
I/O_VL5
I/O_VL6
I/O_VL7
I/O_VL8
I/O_VCC1
I/O_VCC2
I/O_VCC3
I/O_VCC4
VCC
GND
I/O_VCC5
I/O_VCC6
I/O_VCC7
I/O_VCC8
SENSOR_DIN[0]
SENSOR_DIN[1]
SENSOR_DIN[2]
SENSOR_DIN[3]
SENSOR_DIN[4]
SENSOR_DIN[5]
SENSOR_DIN[6]
SENSOR_DIN[7]
C30 0.1u
C31 0.01u
C32 0.1u
C33 0.01u
U7
NLSX3018DWR2G
CSI0_D3+
CSI0_D3−
CSI0_MCLK
CSI1_MCLK
SPI1_SCLK
SPI1_CS
SPI1_DOUT
SPI1_DIN
SENSOR_FV
SENSOR_LV
PIXCLK
GPIO0
SPI_SCLK
SPI_CS
SPI_MOSI
SPI_MISO
C34 0.1u
C35 0.01u
C36 0.1u
C37 0.01u
VCC from Camera PCB, 3.45V
Application note says that VCC and VDD1V2 for U6 and U7 must be decoupled with capacitors, recommend values are 0.01uF to 0.1uF. Current schem used 0.11uF…
AVDD33, 3.3V out —> EthernetBoard-P1_Cu (Layer3)
L1: 64uH~180uH can be used. However, higher value often increse DCR as well. Need lower DCR!
DCR:100uOhm~330mOhm. IDC 825mA~16A.
Below values give 88% efficiency for U8.
SYS_DCIN
Voltage to power on FPGA, 12V 2A
U8
LM2674−3.3
C22 0.01u
C21 100u
C23 22u
D1
DIODE
L1
SRN6045
68uH
AVDD
Cout: 68uF
Cin: 22uF
laerger than 20V rating, 340mV drop (lower Vf is better) D1
U9
LM3671−1.2
L2
2.2u
C24 4.7u
C25 10u
Cin (C24): keep4.7uF
L2: 2.2uH (2.2~2.7uH, higher better…)
lower DCR gives higher efficiency, DCR: less than 260mOhm, IDC: 0.6A~10A
VDD1V2:
1.2V at 0.6A output
EthernetBoard-P1_Cu (Layer3)
power for U4,5,6,7,11,12
Cout (C25): any capacitor 10uF~100uF work, no change on efficiency, only inductor matters
Sheet: /PowerManagement/
File: PowerManagement.sch
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Size: A4
Date:
Rev:
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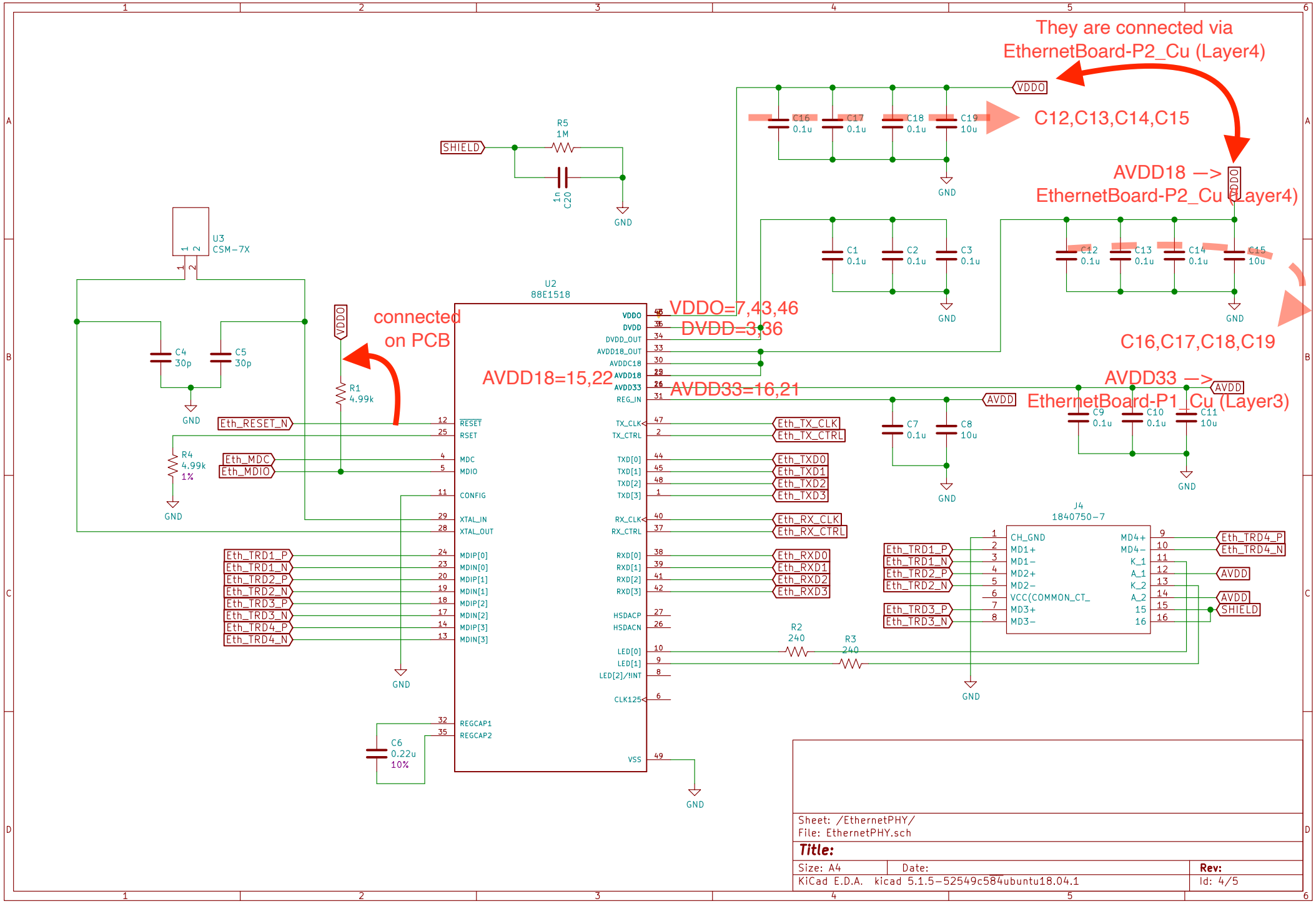
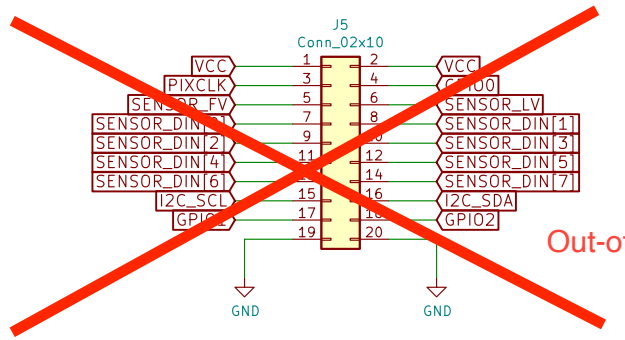
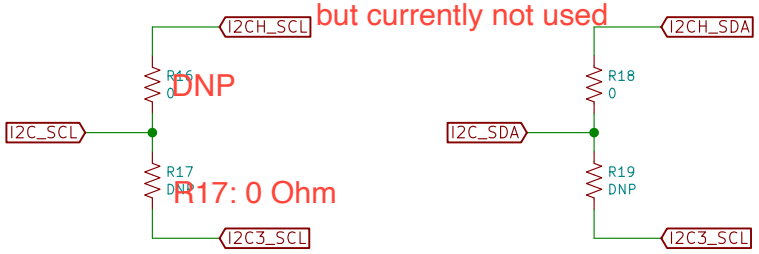
Id: 3/5


They are connected via
EthernetBoard-P2_Cu (Layer4)
C12,C13,C14,C15
AVDD18 —>
EthernetBoard-P2_Cu (Layer4)
C16,C17,C18,C19
AVDD33 —>
EthernetBoard-P1_Cu (Layer3)
connected
on PCB
VDDO=7,43,46
DVDD=3,36
AVDD18=15,22
AVDD33=16,21
U2
88E1518
U3
CSM-7X
R5
1M
1n
C20
SHIELD
R1
4.99k
R4
4.99k
1%
C4
30p
C5
30p
C6
0.22u
10%
R2
240
R3
240
J4
1840750-7
Eth_RESET_N
Eth_MDC
Eth_MDIO
Eth_TRD1_P
Eth_TRD1_N
Eth_TRD2_P
Eth_TRD2_N
Eth_TRD3_P
Eth_TRD3_N
Eth_TRD4_P
Eth_TRD4_N
Eth_TX_CLK
Eth_TX_CTRL
Eth_TXD0
Eth_TXD1
Eth_TXD2
Eth_TXD3
Eth_RX_CLK
Eth_RX_CTRL
Eth_RXD0
Eth_RXD1
Eth_RXD2
Eth_RXD3
VDDO
AVDD
SHIELD
GND
Sheet: /EthernetPHY/
File: EthernetPHY.sch
Title:
Size: A4
Date:
Rev:
KiCad E.D.A. kicad 5.1.5-52549c584ubuntu18.04.1
Id: 4/5



Out-of-Date

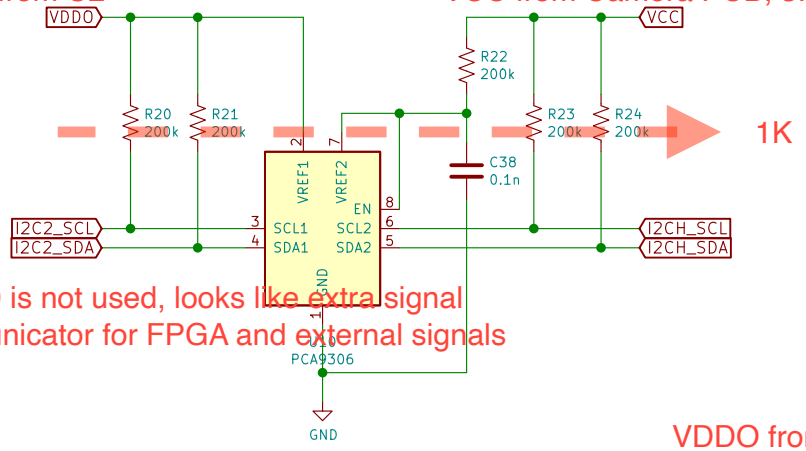
These circuits look like for extra signal communicator for FPGA and external signals, but currently not used



R17: 0 Ohm

VDDO from U2

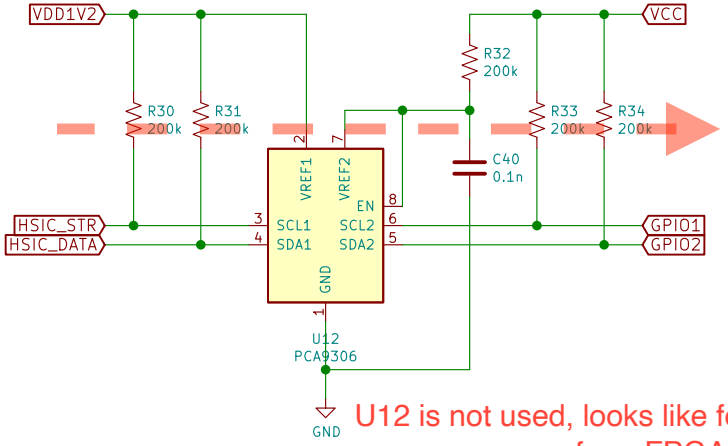
VCC from Camera PCB, 3.45V



1K

U10 is not used, looks like extra signal communicator for FPGA and external signals

VCC from Camera PCB, 3.45V

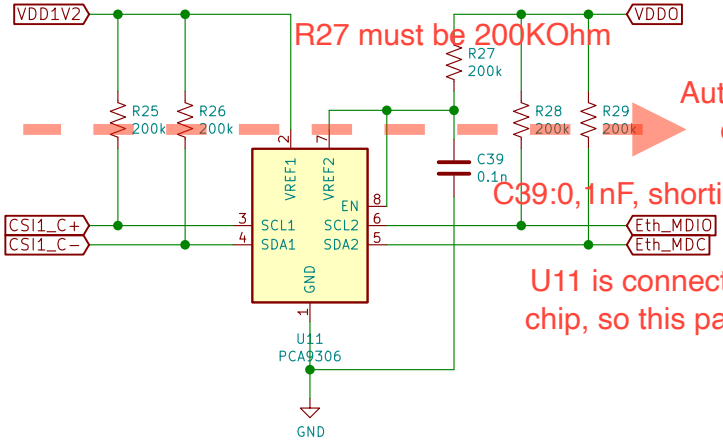


1K

U12 is not used, looks like for GPIO TTL out from FPGA

VDDO from U2

R27 must be 200KOhm



Author used 1K Ohm, however, these pull up resistor should be carefully calculated depending on each side voltage and current driver sink!

C39:0,1nF, shorting or any small values are fine.

U11 is connected to ethernet chip, so this part is important!

Sheet: /IO_Extension/ File: IO_Extension.sch		
Title:		
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.5-52549c584ubuntu18.04.1		Id: 5/5