

1 2 3

TMF8801 Daughter Card

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Sheet 1: Title Page

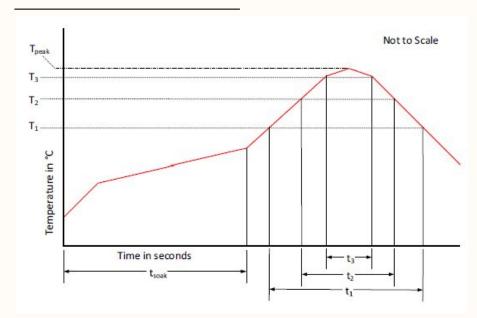
Sheet 2: Project Page (This page)

Sheet 3: Schematics

Revision History

Version: A J.Dolic Initial Release

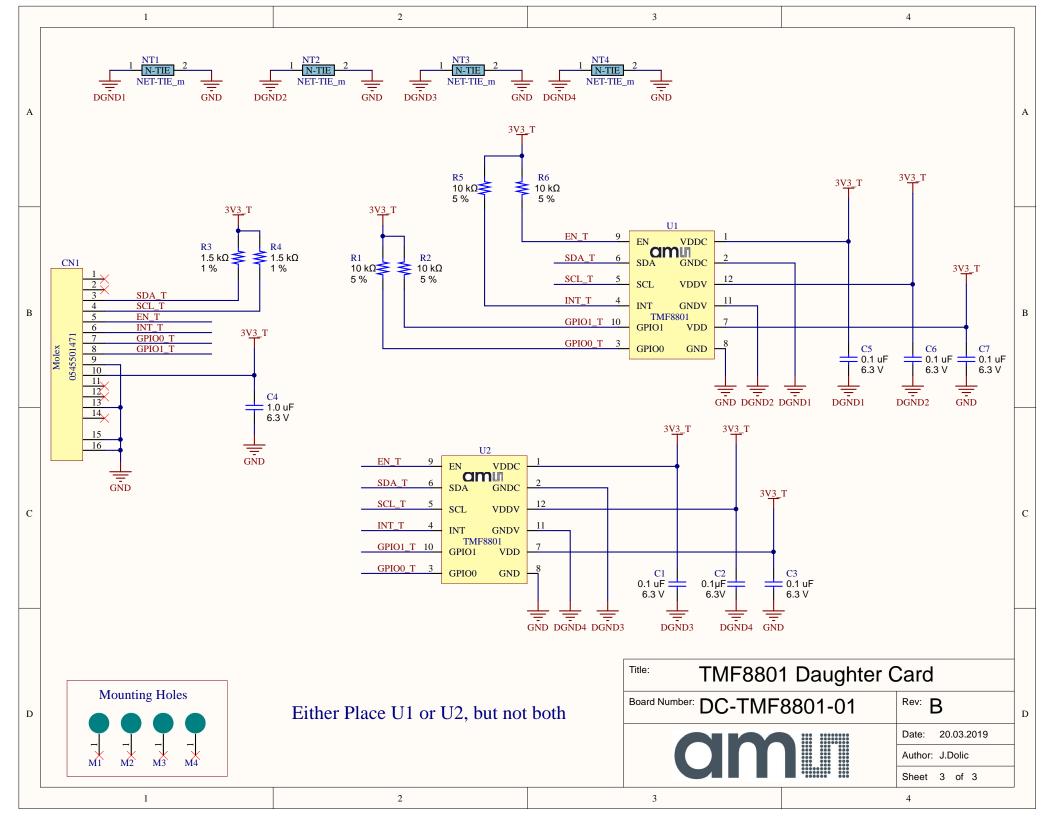
Suggested Board Reflow Profile

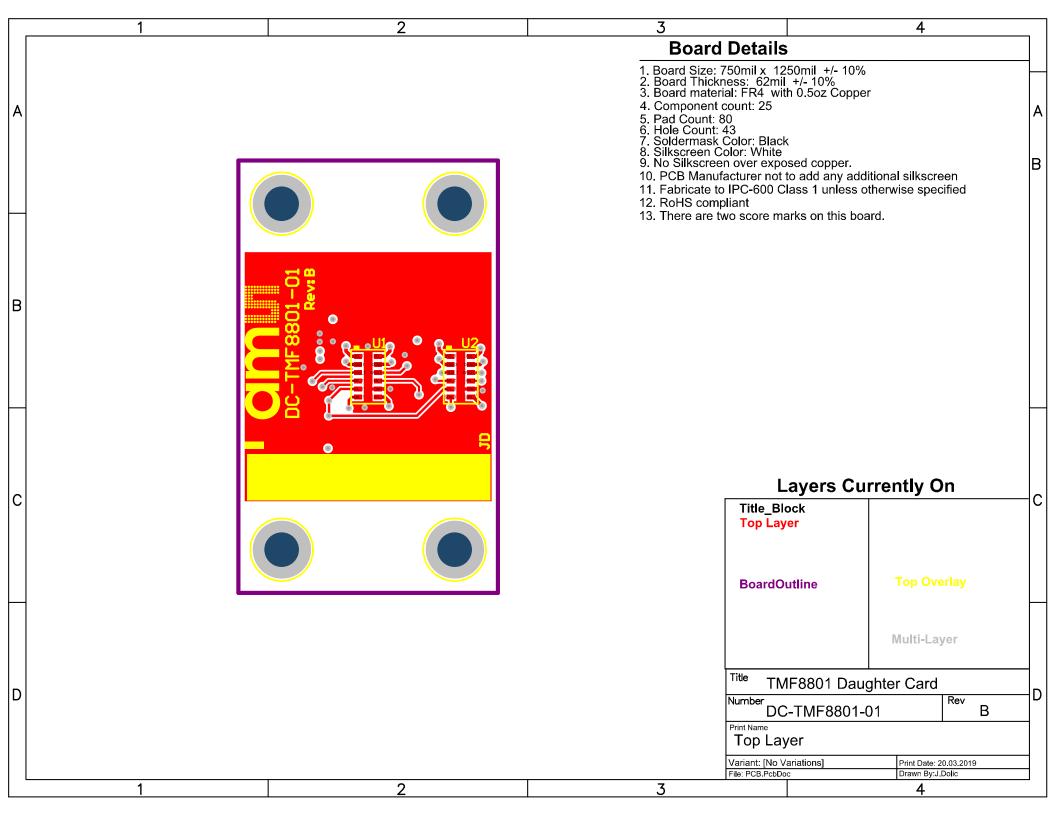


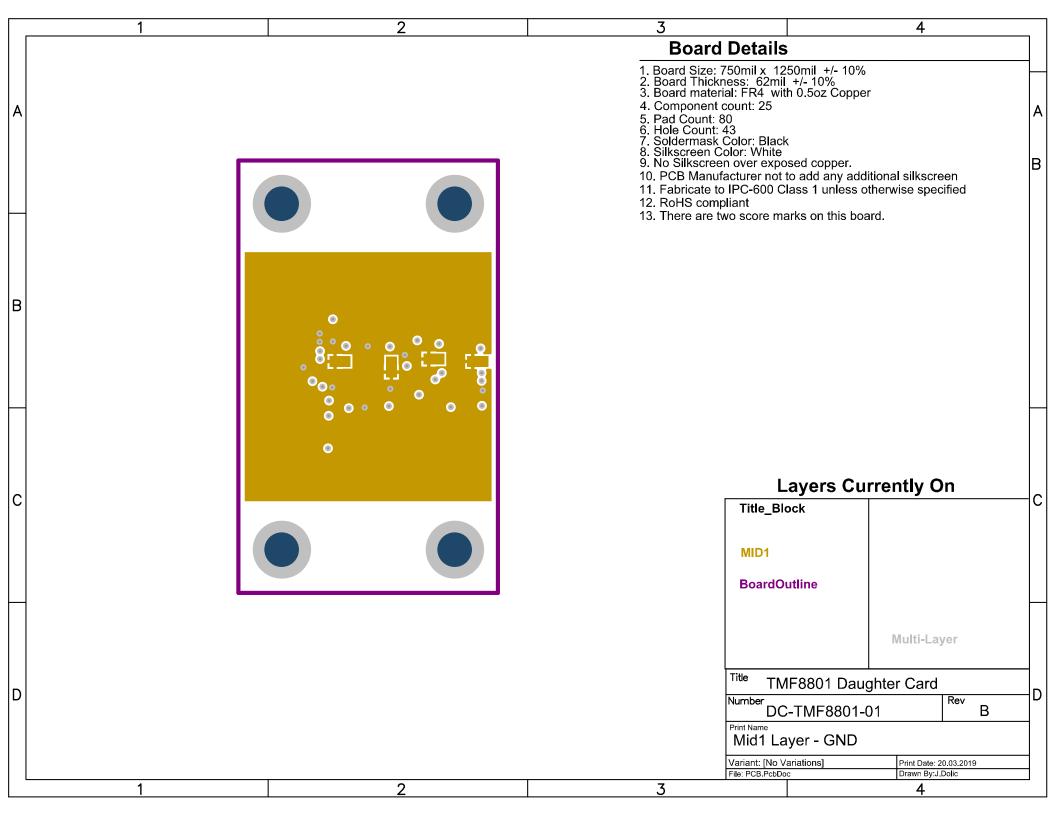
Parameter	Reference	Device
Average temperature gradient in preheating		2.5 °C/sec
Soak time	t _{soak}	2 to 3 minutes
Time above 217 °C (T1)	t ₁	Max 60 sec
Time above 230 °C (T2)	t ₂	Max 50 sec
Time above T _{peak} – 10 °C (T3)	t ₃	Max 10 sec
Peak temperature in reflow	T _{peak}	260 °C
Temperature gradient in cooling		Max -5 °C/sec

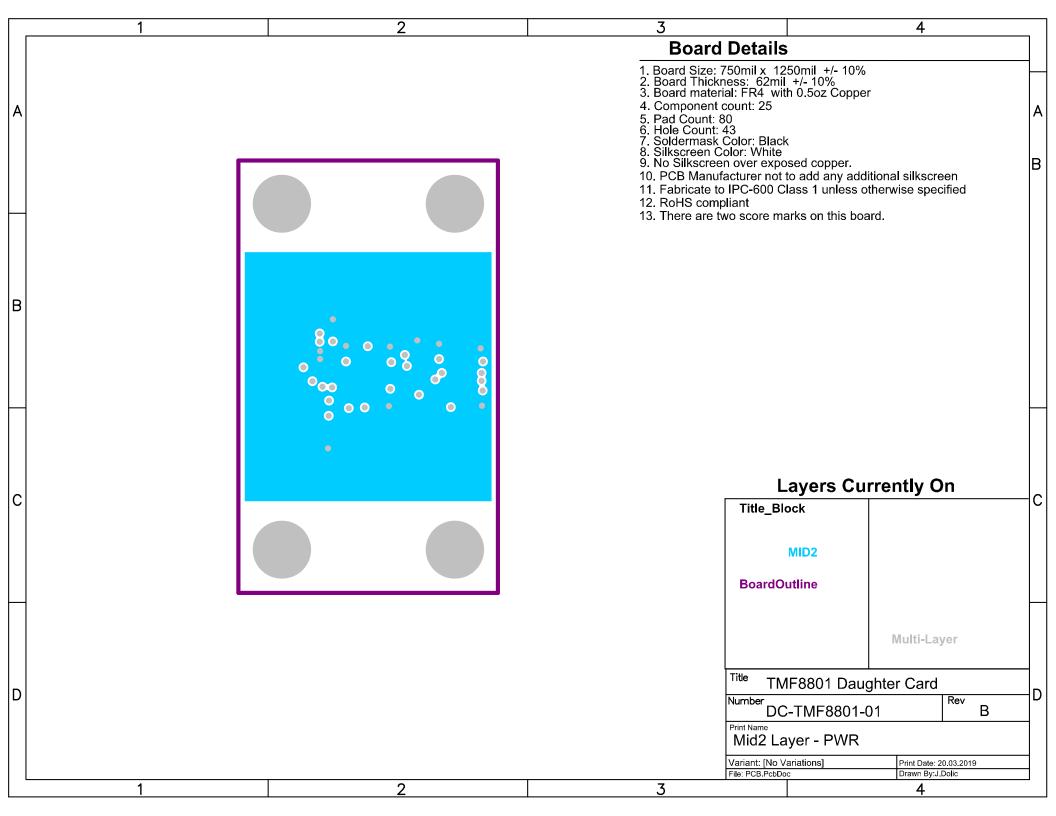
Number DC-TMF8801-01 Revision B	TMF8801 Daughter Card			
		Number DC-TMF880	01-01	Revision B
File: \\\Project Page.SchDoc Drawn By: J.Dolic	Date:	20.03.2019	Sheet 2	3 of
	File:	\\\Project Page.SchDoc	Drawn By:	J.Dolic

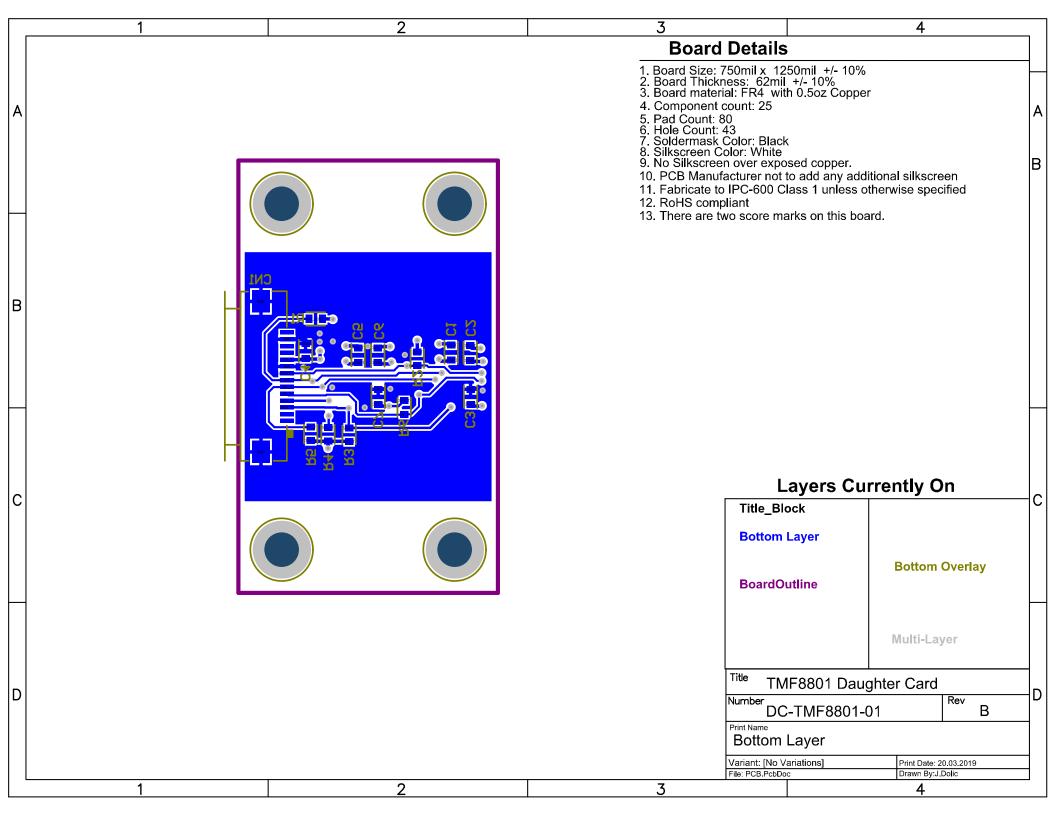
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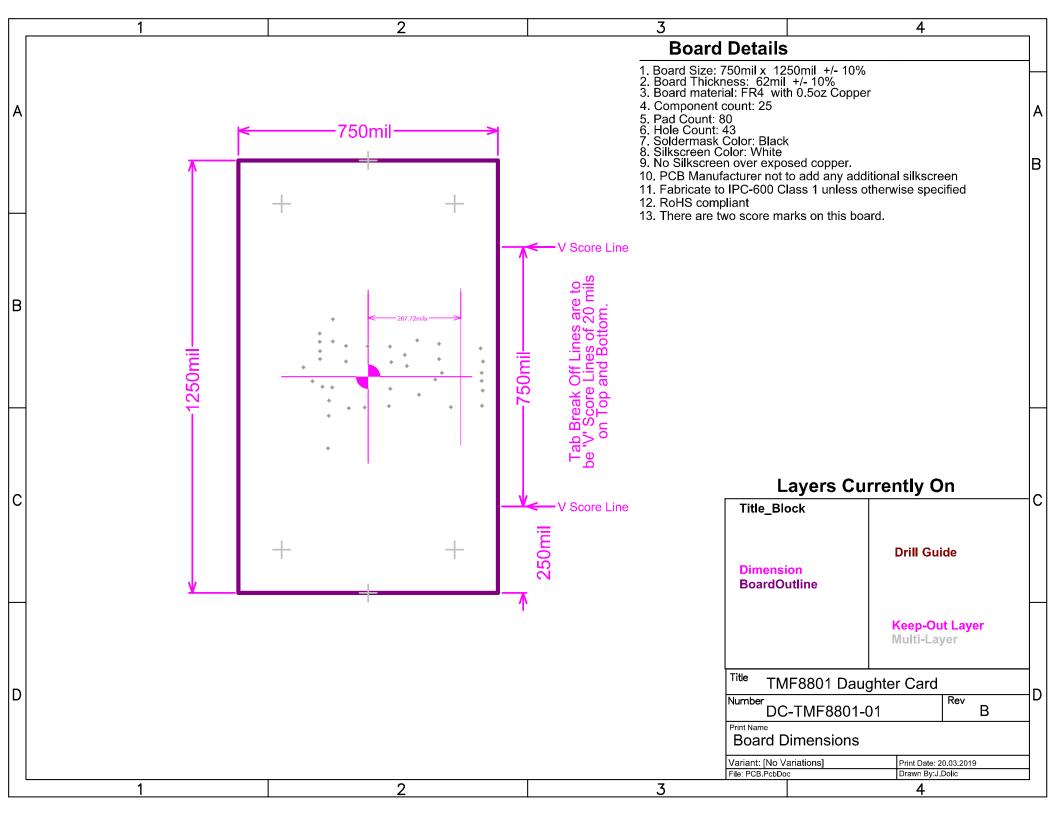


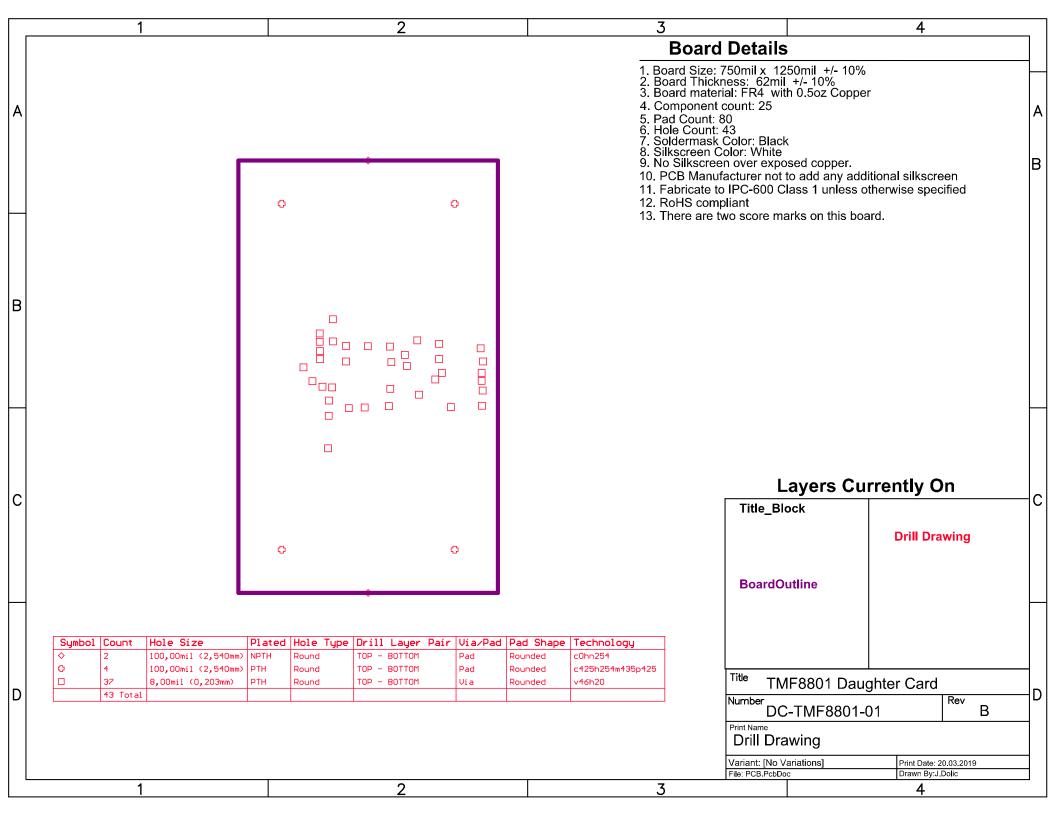


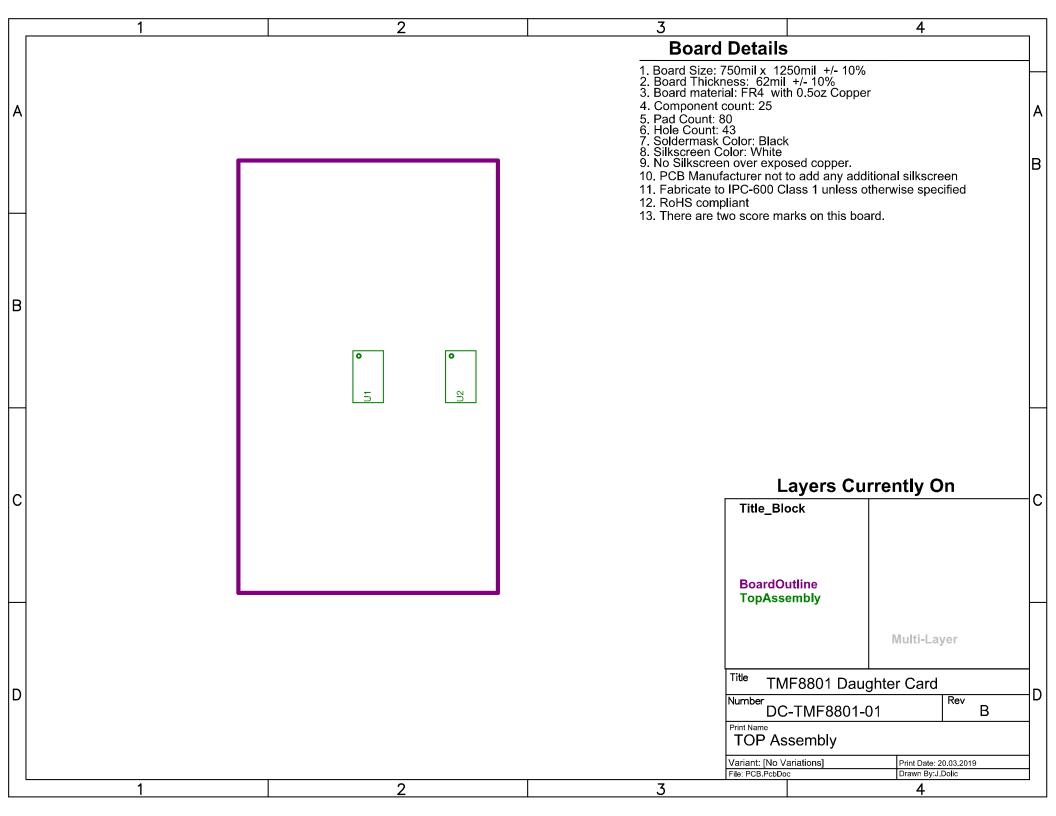


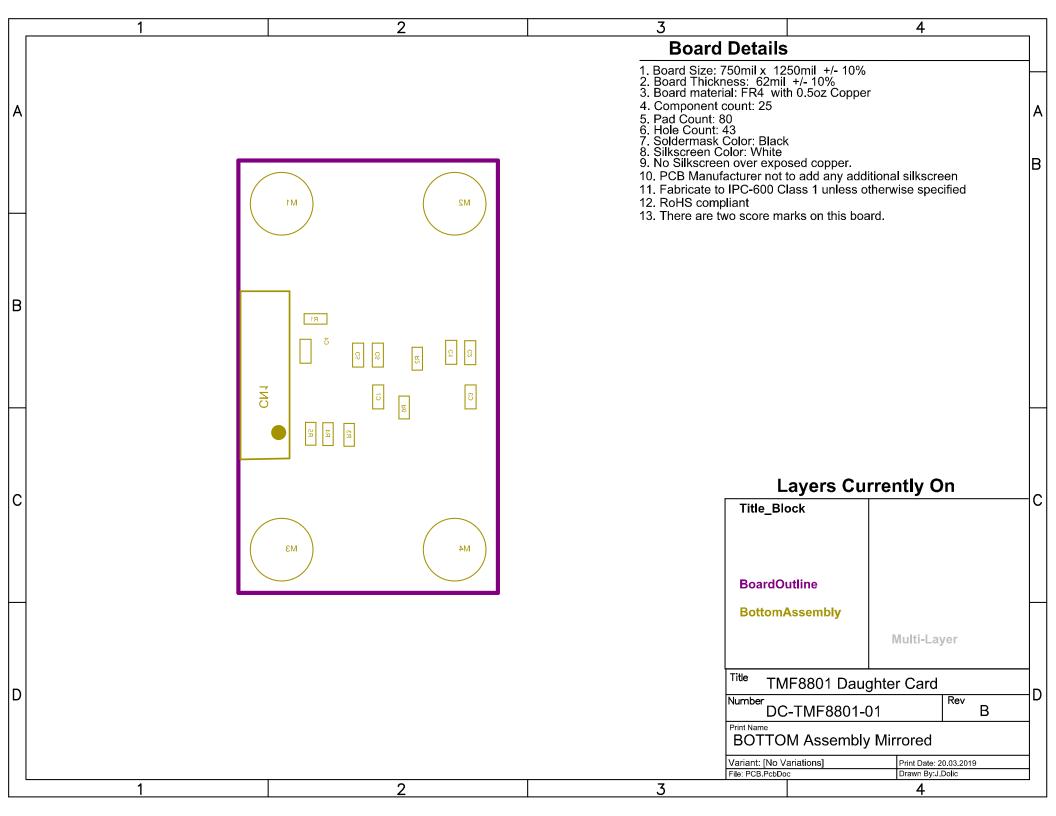












Design Rules Verification ReportFilename: \\fsup04\cnc_prodmgmt\OSL\11_HW_Application_PS\Dahar\Hardware\DC-Dual_T

Warnings 0 Rule Violations 0

Warnings Total 0

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Rule Violations	
Clearance Constraint (Gap=5mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (IsTextInverted),(All)	0
Un-Routed Net Constraint ((All))	0
Width Constraint (Min=4.921mil) (Max=393.701mil) (Preferred=11.811mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=15.748mil) (Conductor Width=5.906mil) (Air Gap=5.906mil)	0
Minimum Annular Ring (Minimum=5mil) (All)	0
Hole Size Constraint (Min=6mil) (Max=232.284mil) (All)	0
Hole To Hole Clearance (Gap=11.811mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Silk To Solder Mask (Clearance=0mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=20mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	0

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Electrical Rules Check Report

Class	Document	Message
Warning	Project Page.SchDoc	Incorrect link between project variant "Default Build" and schematic component Component
		R3 1K5.0402,1%
Warning	Project Page.SchDoc	Incorrect link between project variant "Default Build" and schematic component Component
		R4 1K5,0402,1%
Warning	Project Page.SchDoc	Incorrect link between project variant "Default Build" and schematic component Component
		U1 TOF
Warning	Project Page.SchDoc	Incorrect link between project variant "Default Build" and schematic component Component
	•	U2 TOF

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Bill of Materials

TMF8801 Daughter Card



Source Data From: DC-TMF8801-01.PrjPcb

Project: DC-TMF8801-01.PrjPcb

Variant: None

Creation Date 20.03.2019 14:16:41

Print Date: 20-Mar-19 2:16:52 PM

Designator	Comment	Manufacturer	Manufacturer Part Number	Description	Alternate	Quantity
IC1 C2 C3	/ / /	Murata Electronics North America	GRM155R70J104KA01D	Cap 0.1uF,6V3, 0402, 10%		3
C4	1.0uF,6V3, 0402, 20%	AVX	04026D105MAT2A	Cap 1.0uF,6V3, 0402, 20%	YES	1
CN1	CONN FFC TOP 14POS 0.50MM R/A	Molex	0545501471	CONN FFC TOP 14POS 0.50MM R/A		1
M1, M2, M3, M4	Mounting Hole	PennEngineering	SMTO-M1-1ET	Mounting nut 0.1" Dia M1 thread		4
R1, R2, R5, R6	10K,0402,5%	Vishay Dale	CRCW040210K0JNED	Res, 10K, 0402, 5%		4
U2	TOF	ams AG	TMF8801	TOF		1
						14

Approved

Parts with alternate marked as YES may be replaced by an equivalent with preapproval from AMS.

Parts from ams AG will be consigned